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S1D13706 Embedded Memory LCD Controller

Interfacing to the Freescale MC68030 Microprocessor

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1 Introduction

This application note describes the hardware and software environment required to interface the S1D13706 Embedded Memory LCD Controller and the Freescale MC68030 microprocessor.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Electronics America website at http://www.eea.epson.com for the latest revision of this document before beginning any development.

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2 Freescale MC68030 Bus Interface

2.1 Overview

The MC68030 is a second generation enhanced microprocessor from the Freescale M68000 family of devices. The MC68030 is a 32-bit microprocessor with a 32-bit address bus and a 32-bit data bus. The microprocessor supports both asynchronous and synchronous bus cycles and burst data transfers. The bus also supports dynamic bus sizing which automatically determines device port size on a cycle-by-cycle basis.

2.2 Dynamic Bus Sizing

The MC68030 supports dynamic bus sizing using the following signals.

- SIZ1 and SIZ0 indicate the number of bytes remaining to be transfered for the current bus cycle.

Table 2-1: SIZ Signal Encoding

SIZ1	SIZ0	Bytes Remaining
0	1	1 Byte
1	0	2 Bytes (Word)
1	1	3 Bytes
0	0	4 Bytes (Double Word)

- DSACK1 and DSACK0 (the data transfer size acknowledge signals) indicate the size of the external port and acknowledge the end of the cycle.

Table 2-2: $\overline{DSACK}$ Decoding

$\overline{DSACK1}$	$\overline{DSACK0}$	Result
1	1	Insert Wait States in the Current Bus Cycle
1	0	Complete Cycle - Data Bus Port Size is 8 bits
0	1	Complete Cycle - Data Bus Port Size is 16 bits
0	0	Complete Cycle - Data Bus Port Size is 32 bits

- A0 and A1 determine which portion of the data bus the data is transferred on and whether the address is misaligned.

2.3 Asynchronous / Synchronous Bus Operation

The MC68030 bus can operate asynchronously or synchronously. Asynchronous operation requires $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{AS}$, and $\overline{DS}$ to control transfers. The $\overline{DSACK}$ signals specify the port width and insert wait states in the current bus cycle. $\overline{AS}$ (the address strobe)

signals the start of a bus cycle by indicating a valid address has been placed on the bus. $\overline{DS}$ (the data strobe) is used as a condition for valid data on the data bus. SIZ selects the active portions of the data bus. R/$\overline{W}$ indicates a read or write operation.

Synchronous bus cycles operate much like asynchronous cycles except only 32-bit port sizes are allowed. In this mode the $\overline{DSACK}$ signals are not required. Wait states are inserted with the synchronous signal ($\overline{STERM}$) which signals that the data is to be latched on the next clock when asserted.

3 S1D13706 Host Bus Interface

The S1D13706 directly supports multiple processors. The S1D13706 implements a MC68K #2 Host Bus Interface which directly supports the Freescale MC68030 microprocessor.

The MC68K #2 Host Bus Interface is selected by the S1D13706 on the rising edge of RESET#. After RESET# is released, the bus interface signals assume their selected configuration. For details on the S1D13706 configuration, see Section 4.2, “S1D13706 Hardware Configuration” on page 12.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13706 Pin Names	Freescale MC68030
AB[16:0]	A[16:0]
DB[15:0]	D[31:16]
WE1#	$\overline{DS}$
CS#	External Decode
M/R#	External Decode
CLKI	CLK
BS#	$\overline{AS}$
RD/WR#	R/$\overline{W}$
RD#	External Decode of SIZ1 and SIZ0
WE0#	SIZ0
WAIT#	$\overline{DSACK1}$
RESET#	System $\overline{RESET}$

3.2 Host Bus Interface Signals

The Host Bus Interface requires the following signals.

- CLKI is a clock input which is required by the S1D13706 Host Bus Interface as a source for its internal bus and memory clocks. This clock is typically driven by the host CPU system clock. For this example, CLK from the Freescale MC68030 is used for CLKI.
- The address inputs AB[16:0], and the data bus DB[15:0], connect directly to the MC68030 address (A[16:0) and data bus (D[31:16]), respectively. CNF4 must be set to select big endian mode.
- Chip Select (CS#) must be driven low by the external address decode circuitry whenever the S1D13706 is accessed by the Freescale MC68030.
- M/R# (memory/register) selects between memory or register accesses. This signal is generated by the external address decode circuitry.
- WE0# connects to SIZ0, one of the transfer size signals of the MC68030. Along with SIZ1 this signal indicates how many bytes are to be transferred during the current cycle.
- WE1# connects to $\overline{DS}$ (the data strobe signal from the MC68030) and must be driven low when valid data has been placed on the bus.
- RD# connects to external decode circuitry of SIZ1, one of the transfer size signals of the MC68030. Along with SIZ0 this signal indicates how many bytes are to be transferred during the current cycle.
- RD/WR# is the read or write enable signal and connects to R/$\overline{W}$ of the MC68030. This signal drives low when the MC68030 is writing to the S1D13706 and drives high when the MC68030 is reading from the S1D13706.
- WAIT# connects to $\overline{DSACK1}$ and is a signal which is output from the S1D13706 which indicates the MC68030 must wait until data is ready (read cycle) or accepted (write cycle) on the host bus. Since MC68030 accesses to the S1D13706 may occur asynchronously to the display update, it is possible that contention may occur in accessing the S1D13706 internal registers and/or display buffer. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete.
- BS# connects to AS (the address strobe from the MC68030) and must be driven low when a valid address has been placed on the address bus.

4 MC68030 to S1D13706 Interface

4.1 Hardware Description

The interface between the S1D13706 and the MC68030 requires external glue logic. Address decoding logic is required to provide the chip select (CS#) and memory/register (M/R#) signals to the S1D13706 since the MC68030 does not have a chip select module.

SIZ1 is modified to signal the S1D13706 that 24-bit and 32-bit accesses are to converted into word-byte and word-word accesses, respectively. Misaligned operands for 24-bit and 32-bit cycles are not supported with this external circuitry for SIZ1.RD# must be connected to the following logic circuitry instead of directly to SIZ1.

RD# = ’(SIZ0 & SIZ1’).

The polarity of the WAIT# signal must be selected as active high by connecting CNF5 to NIO V_{DD} (see Table 4-1:, “Summary of Power-On/Reset Configuration Options,” on page 12).

The diagram below shows a typical implementation of the MC68030 to S1D13706 interface.

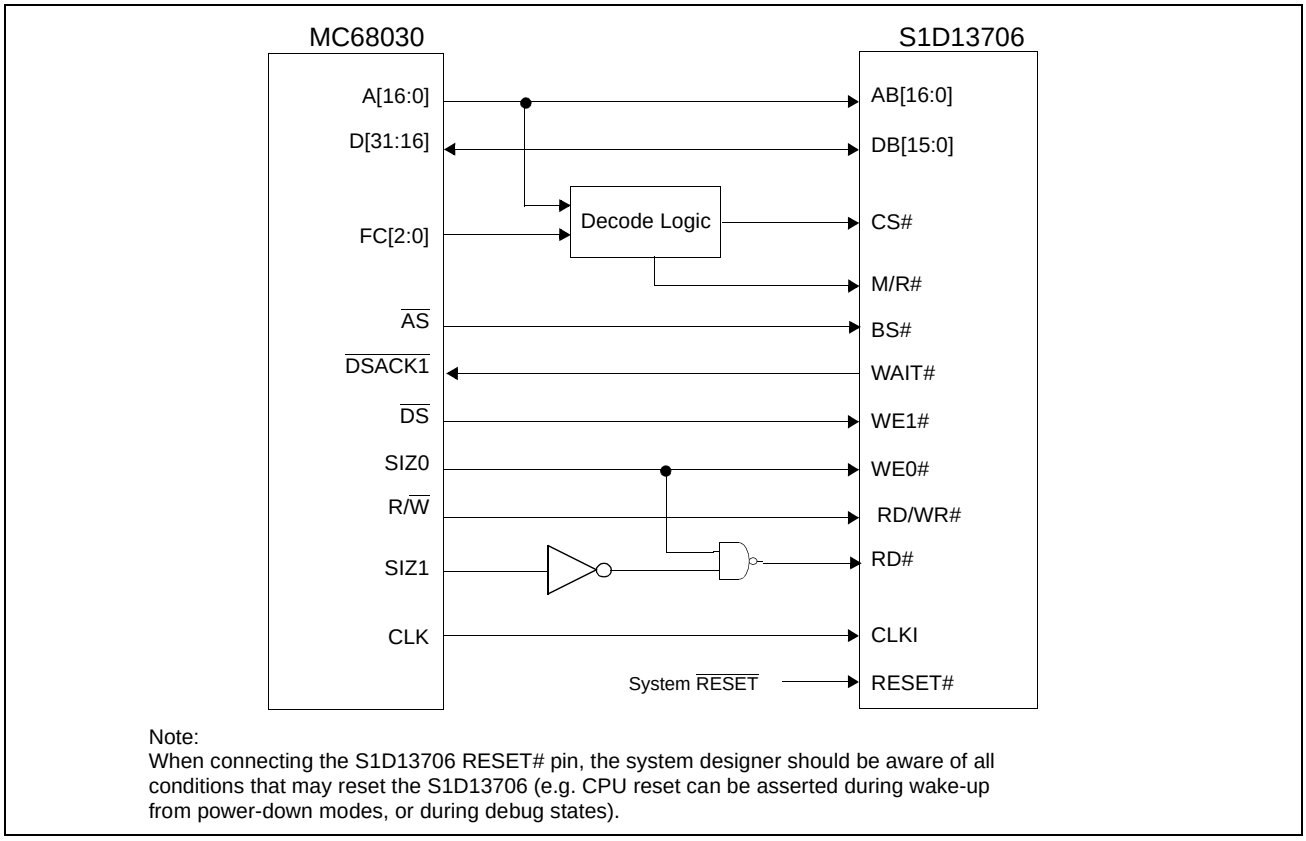

Figure 4-1: Typical Implementation of MC68030 to S1D13706 Interface

Note

The interface was designed using a Freescale MC68030 Integrated Development Platform (IDP).

4.2 S1D13706 Hardware Configuration

The S1D13706 uses CNF7 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

The following table shows the configuration required for this implementation of a S1D13706 to Freescale MC68030 microprocessor.

Table 4-1: Summary of Power-On/Reset Configuration Options

S1D13706 Pin Name	value on this pin at the rising edge of RESET# is used to configure: (1/0)	
	1	0
CNF[2:0]	010 = MC68K #2 Host Bus Interface	
CNF3	GPIO pins as inputs at power on	GPIO pins as HR-TFT / D-TFT outputs
CNF4	Big Endian bus interface	Little Endian bus interface
CNF5	Active high WAIT#	Active low WAIT#
CNF[7:6]	see Table "" for recommended settings	

= configuration for MC68030 microprocessor

Table 4-2: CLKI to BCLK Divide Selection

CNF7	CNF6	CLKI to BCLK Divide
0	0	1:1
0	1	2:1
1	0	3:1
1	1	4:1

= recommended setting for MC68030 microprocessor

4.3 Register/Memory Mapping

The MC68030 IDP board uses the first 256M bytes of address space, therefore the S1D13706 can be mapped anywhere beyond this boundary. The S1D13706 uses two 128K byte blocks which are selected using M/R# from the address decoder. The internal registers occupy the first 128K bytes block and the 80K byte display buffer occupies the second 128K byte block. Registers were located at memory location 10A0 0000h and the display buffer at memory location 10E0 0000h. The address space for the S1D13706 is user dependent.

5 Software

Test utilities and Windows® CE v2.11/2.12 display drivers are available for the S1D13706. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13706CFG, or by directly modifying the source. The Windows CE v2.11/2.12 display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13706 test utilities and Windows CE v2.11/2.12 display drivers are available from your sales support contact or on the internet at http://www.eea.epson.com.

6 References

6.1 Documents

- Freescale Semiconductor, *MC68030 32-bit Enhanced Microprocessor User's Manual*, Freescale Publication no. MC68030UM; available on the Internet at http://www.freescale.com.
- Epson Research and Development, Inc., *S1D13706 Hardware Functional Specification*, Document Number X31B-A-001-xx.
- Epson Research and Development, Inc., *S5U13706B00C Rev. 1.0 Evaluation Board User Manual*, Document Number X31B-G-004-xx.
- Epson Research and Development, Inc., *Programming Notes and Examples*, Document Number X31B-G-003-xx.

6.2 Document Sources

- Freescale Semiconductor Website: www.freescale.com.
- Epson Electronics America website: http://www.eea.epson.com.

7 Technical Support

7.1 EPSON LCD/CRT Controllers (S1D13706)

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway
San Jose, CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

7.2 Freescale MC68030 Processor

- Freescale Semiconductor Website: www.freescale.com.
- Freescale Semiconductor sales office or authorized distributor.