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S1D13706 Embedded Memory LCD Controller

Interfacing to the Motorola RedCap2 DSP With Integrated MCU

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1 Introduction

This application note describes the hardware and software environment required to provide an interface between the S1D13706 Embedded Memory LCD Controller and the Motorola REDCAP2 processor.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Electronics America Website at www.eea.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at techpubs@erd.epson.com.

2 Interfacing to the REDCAP2

2.1 The REDCAP2 System Bus

REDCAP2 integrates a RISC microprocessor (MCU) and a general purpose digital signal processor (DSP) on a single chip. The External Interface Module (EIM) handles the interface to external devices. This section provides an overview of the operation of the REDCAP2 bus in order to establish interface requirements.

2.2 Overview

REDCAP2 uses a 22-bit address bus (A[21:0]) and 16-bit data bus (D[15:0]). All IO is synchronous to a square wave reference clock called CKO. The CKO source can be the DSP clock or the MCU clock and is selected/disabled in the Clock Control Register (CKCTL).

REDCAP2 can generate up to 6 independent chip select outputs. Each chip select has a memory range of 16M bytes and can be independently programmed for wait-states and port size.

Note
REDCAP2 does not provide a wait or termination acknowledge signal to external devices. Therefore, all external devices must guarantee a fixed cycle length.

2.3 Bus Transactions

The chip initiates a data transfer by placing the memory address on address lines A0 through A21. Several control signals are provided with the memory address.

- R/$\overline{W}$ — set high for read cycles and low for write cycles.
- $\overline{EB0}$ — active low signal indicates access to data byte 0 (D[15:8]) during read or write cycles.
- $\overline{EB1}$ — active low signal indicates access to data byte 1 (D[7:0]) during read or write cycles.
- $\overline{OE}$ — active low signal indicates read accesses and enables slave devices to drive the data bus.

Figure 2-1: “REDCAP2 Memory Read Cycle” on page 7 illustrates a typical memory read cycle on the REDCAP2 bus.

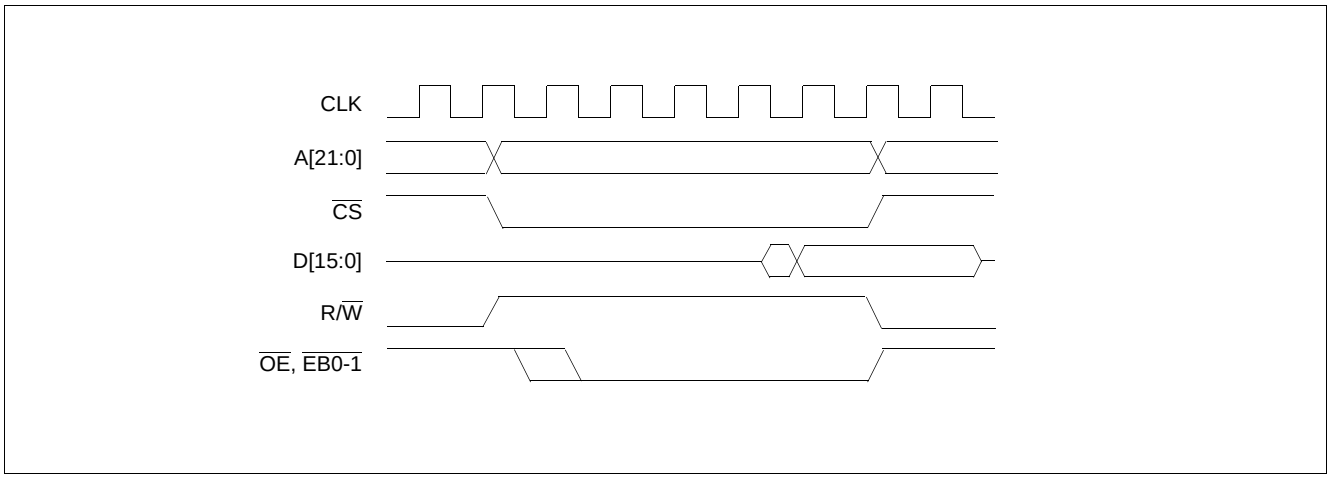

Figure 2-1: REDCAP2 Memory Read Cycle

Figure 2-2: “REDCAP2 Memory Write Cycle” on page 7 illustrates a typical memory write cycle on the REDCAP2 bus.

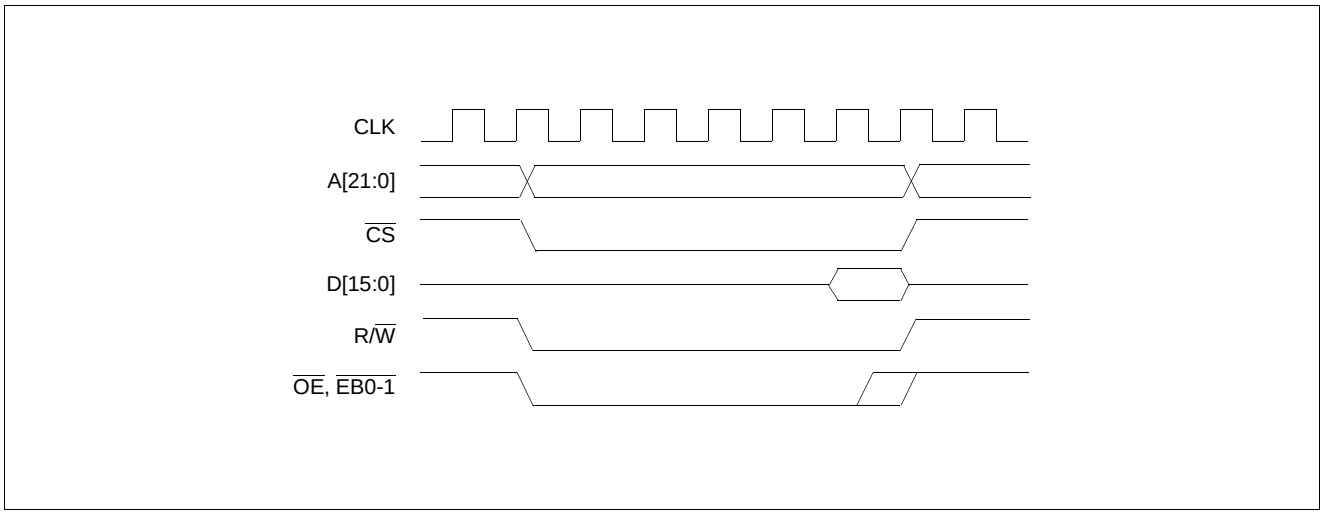

Figure 2-2: REDCAP2 Memory Write Cycle

3 S1D13706 Host Bus Interface

The S1D13706 implements a 16-bit native REDCAP2 host bus interface which is used to interface to the REDCAP2 processor.

The REDCAP2 host bus interface is selected by the S1D13706 on the rising edge of RESET#. After releasing reset, the bus interface signals assume their selected configuration. For details on S1D13706 configuration, see Section 4.3, “S1D13706 Hardware Configuration” on page 13.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13706 Pin Names	REDCAP2
AB[16:0]	A[16:0]
DB[15:0]	D[15:0]
WE1#	$\overline{EB0}$
M/R#	A17
CS#	REDCAP2 Internal Chip Select
CLKI	CKO
BS#	Connected to HIO V_{DD}
RD/WR#	R/$\overline{W}$
RD#	$\overline{OE}$
WE0#	$\overline{EB1}$
WAIT#	N/A
RESET#	$\overline{RST_OUT}$

3.2 Host Bus Interface Signals

The Host Bus Interface requires the following signals:

- CLKI is a clock input which is required by the S1D13706 host bus interface and connects to CKO of the REDCAP2.
- The address inputs AB[16:0], and the data bus DB[15:0], connect directly to the REDCAP2 bus address (A[16:0]) and data bus (D[15:0]), respectively. CNF[2:0] and CNF4 must be set to select the REDCAP2 host bus interface with big endian mode.
- M/R# (memory/register) selects between memory or register access. It may be connected to an address line, allowing REDCAP2 bus address A17 to be connected to the M/R# line.
- CS# (Chip Select) must be driven low whenever the S1D13706 is accessed by the REDCAP2 bus.
- RD/WR# connects to R/$\overline{W}$ which indicates whether a read or a write access is being performed on the S1D13706.
- WE1# and WE0# connect to $\overline{EB0}$ and $\overline{EB1}$ (Enable Byte 0 and 1) for byte steering.
- RD# connects to $\overline{OE}$ (Output Enable). This signal must be driven by the REDCAP2 bus to indicate the bus access is a read and enables slave devices to drive the data bus with read data.
- The BS# and WAIT# signals are not needed for this bus interface, they should be connected to HIO V_{DD}.

4 REDCAP2 to S1D13706 Interface

4.1 Hardware Description

The interface between the S1D13706 and the REDCAP2 requires no external glue logic. The information in this section describes the environment necessary to connect the S5U13706B00C Evaluation Board and the Motorola DSP56654 Application Development Module (ADM). For a list of connections between the pins and signals of the REDCAP2 and the S1D13706 see Table 4-1:,“List of Connections from REDCAP2 ADM to S5U13706B00C” on page 11.

The following figure demonstrates a typical implementation of the S1D13706 to REDCAP2 interface.

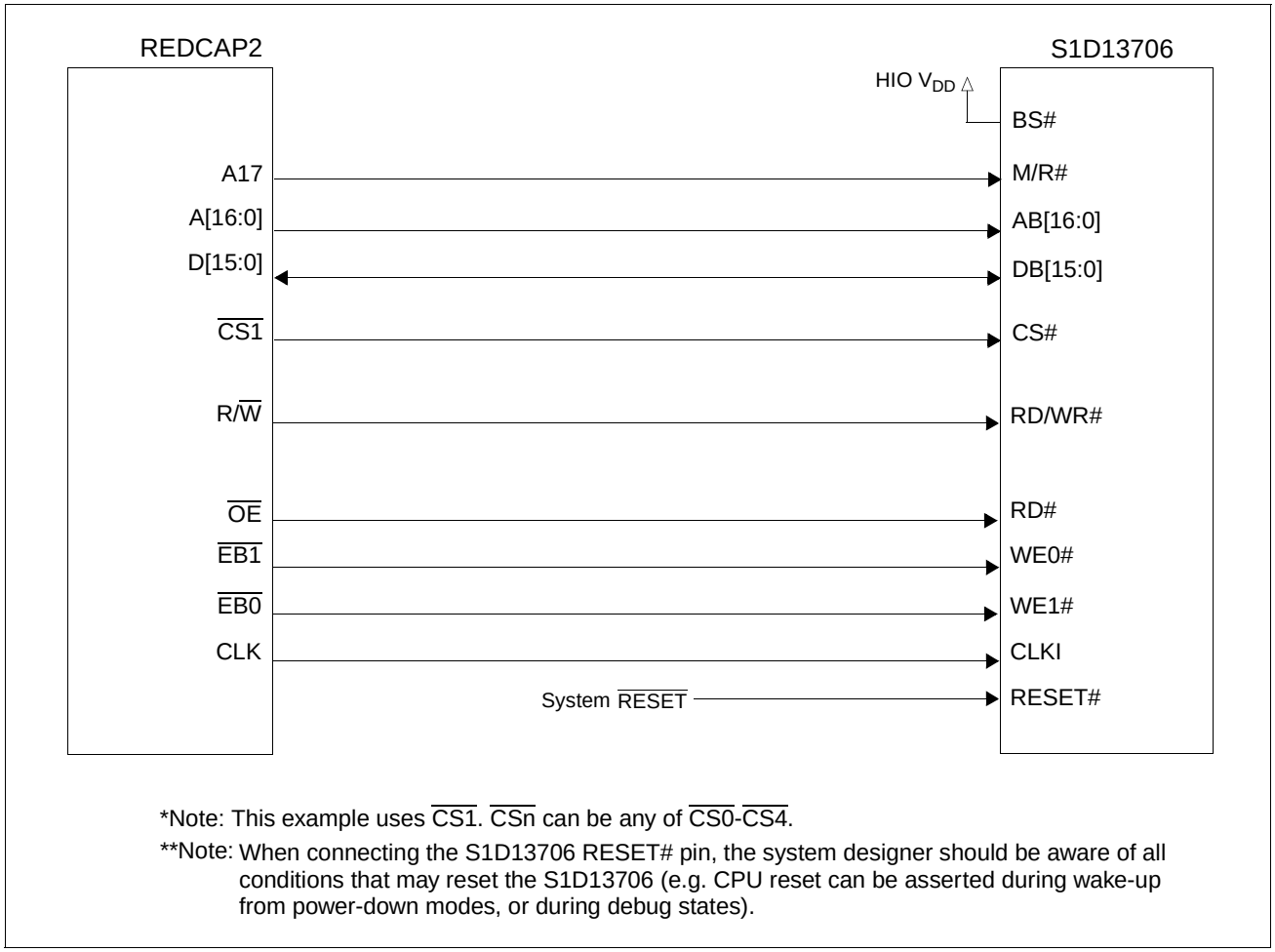

Figure 4-1: Typical Implementation of REDCAP2 to S1D13706 Interface

4.2 Hardware Connections

The following table details the connections between the pins and signals of the REDCAP2 and the S1D13706.

Table 4-1: List of Connections from REDCAP2 ADM to S5U13706B00C

REDCAP2 Signal Name	REDCAP2ADS Connector and Pin Name	S1D13706 Signal Name
A17	P9-34	M/R#
A16	P9-33	AB20
A15	P9-32	AB19
A14	P9-31	AB18
A13	P9-30	AB17
A12	P9-29	AB16
A11	P9-28	AB15
A10	P9-27	AB14
A9	P9-26	AB13
A8	P9-25	AB12
A7	P9-24	AB11
A6	P9-23	AB10
A5	P9-22	AB9
A4	P9-21	AB8
A3	P9-20	AB7
A2	P9-19	AB6
A1	P9-18	AB5
A0	P9-17	AB4
D15	P9-16	DB15
D14	P9-15	DB14
D13	P9-14	DB13
D12	P9-13	DB12
D11	P9-12	DB11
D10	P9-11	DB10
D9	P9-10	DB9
D8	P9-9	DB8
D7	P9-8	DB7
D6	P9-7	DB6
D5	P9-6	DB5
D4	P9-5	DB4
D3	P9-4	DB3
D2	P9-3	DB2
D1	P9-2	DB1
D0	P9-1	DB0
RES_OUT	P24-6	RESET#

Table 4-1: List of Connections from REDCAP2 ADM to S5U13706B00C (Continued)

REDCAP2 Signal Name	REDCAP2ADS Connector and Pin Name	S1D13706 Signal Name
CLK0	P24-3	BUSCLK
$\overline{CS1}$	P9-40	CS#
R/$\overline{W}$	P9-47	RD/WR#
$\overline{OE}$	P9-48	RD#
$\overline{EB1}$	P9-46	WE0#
$\overline{EB0}$	P9-45	WE1#
Gnd	P24-20 / P9-50	Vss

Note

In order for the S5U13706B00C evaluation board to work with the ADM, pin 5 and pin 13 of U28 on the ADM must be connected to $V_{DD.}$ This ensures that the DIR signal of transceivers U17 and U18 is low only during read access, even when EBC in the CS1 Control Register is set to 0.

4.3 S1D13706 Hardware Configuration

The S1D13706 uses CNF7 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

The following table shows the configuration required for this implementation of a S1D13706 to Motorola REDCAP2 microprocessor.

Table 4-2: Summary of Power-On/Reset Options

S1D13706 Pin Name	**state of this pin at rising edge of RESET# is used to configure:**(1/0)	
	1	**0**
CNF[2:0]	101 = REDCAP2 Host Bus Interface	
CNF3	GPIO pins as inputs at power-on	GPIO pins as HR-TFT/ D-TFD outputs
CNF4	Big Endian bus interface	Little Endian bus interface
CNF5	WAIT# is active high	WAIT# is active low
CNF[7:6]	CLKI to BCLK divide select: CNF7 CNF6 CLKI to BCLK Divide Ratio 0 0 1 : 1 0 1 2 : 1 1 0 3 : 1 1 1 4 : 1	

= configuration for REDCAP2 microprocessor

4.4 Register/Memory Mapping

The S1D13706 is a memory mapped device. The S1D13706 uses two 128K byte blocks which are selected using A17 from the REDCAP2 bus (A17 is connected to the S1D13706 M/R# pin). The internal registers occupy the first 128K byte block and the 80K byte display buffer occupies the second 128K byte block. In this example, the S1D13706 internal registers are accessed starting at address 4100 0000h and the display buffer is accessed starting at address 4102 0000h.

Each Chip Select on the REDCAP2 is allocated a 16M byte block. However, the S1D13706 only needs a 256K byte block of memory to accommodate its register set and 80K byte display buffer. For this reason, only address bits A[17:0] are used while A[21:18] are ignored. The S1D13706's memory and register are aliased every 256K bytes in the 16M byte CS1 address space.

Note
If aliasing is not desirable, the upper addresses must be fully decoded.

4.5 REDCAP2 Chip Select Configuration

In this example, Chip Select 1 controls the S1D13706. The following options are selected in the CS1 Control Register.

- CSEN = 1 — Chip Select function enabled.
- WP = 0 — writes allowed.
- SP = 0 — user mode access allowed.
- DSZ = 10 — 16-bit Port.
- EBC = 0 — assert $\overline{\text{EB0-1}}$ for both reads and writes.
- WEN = 1 — $\overline{\text{EB0-1}}$ negated half a clock earlier during write cycle.
- OEA = 1 — $\overline{\text{OE}}$ asserted half a clock later during a read cycle.
- CSA = 0 — Chip Select asserted as early as possible. No idle cycle inserted between back-to-back external transfers.
- EDC = 1 — an idle cycle is inserted after a read cycle for back-to-back external transfers, unless the next cycle is a read cycle to the same $\overline{\text{CS}}$ bank.
- WWS = 0 — same length for reads and writes.

5 Software

Test utilities and Windows® CE v2.11/2.12 display drivers are available for the S1D13706. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13706CFG, or by directly modifying the source. The Windows CE v2.11/2.12 display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13706 test utilities and Windows CE v2.11/2.12 display drivers are available from your sales support contact or on the internet at www.eea.epson.com.

6 References

6.1 Documents

- Motorola Inc., *REDCAP2 Digital Signal Processor Integrated With MCU Product Specifications Rev. 1.2ext*.
- Epson Research and Development, Inc., *S1D13706 Hardware Functional Specification*, Document Number X31B-A-001-xx.
- Epson Research and Development, Inc., *S5U13706B00C Rev. 1.0 Evaluation Board User Manual*, Document Number X31B-G-004-xx.
- Epson Research and Development, Inc., *S1D13706 Programming Notes and Examples*, Document Number X31B-G-003-xx.

6.2 Document Sources

- Motorola Literature Distribution Center: (800) 441-2447.
- Epson Electronics America Website: www.eea.epson.com.

7 Technical Support

7.1 EPSON LCD/CRT Controllers (S1D13706)

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