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S1D13706 Embedded Memory LCD Controller

Interfacing to 8-bit Processors

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1 Introduction

This application note describes the hardware and software environment required to interface the S1D13706 Embedded Memory LCD Controller and 8-bit processors. This document is not intended to cover all possible implementation, but provides a generic example of how such an interface can be accomplished.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Electronics America website at http://www.eea.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Interfacing to an 8-bit Processor

2.1 The Generic 8-bit Processor System Bus

Although the S1D13706 does not directly support an 8-bit CPU, an 8-bit interface can be achieved with minimal external logic.

Typically, the bus of an 8-bit microprocessor is straight forward with minimal CPU and system control signals. To connect a memory mapped device such as the S1D13706, only the write, read, and wait control signals, plus the data and address lines, need to be interfaced. Since the S1D13706 is a 16-bit device, some external logic is required.

3 S1D13706 Host Bus Interface

The S1D13706 directly supports multiple processors. The S1D13706 implements a 16-bit Generic #2 Host Bus Interface which can be adapted for use with an 8-bit processor.

The Generic #2 Host Bus Interface is selected by the S1D13706 on the rising edge of RESET#. After RESET# is released, the bus interface signals assume their selected configuration. For details on the S1D13706 configuration, see Section 4.2, “S1D13706 Hardware Configuration” on page 10.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13706 Pin Names	Generic #2	Comments
AB[16:0]	A[16:0]	—
DB[15:0]	D[15:0]	—
WE1#	Byte High Enable (BHE#)	External decode required
CS#	Chip Select	External decode required
M/R#	Memory/Register Select	External decode required
CLKI	BUSCLK	—
BS#	connect to HIO V_{DD}	—
RD/WR#	connect to HIO V_{DD}	—
RD#	RD#	—
WE0#	WE#	—
WAIT#	WAIT#	—
RESET#	Inverted RESET	—

3.2 Host Bus Interface Signals

The S1D13706 Generic #2 Host Bus Interface requires the following signals from an 8-bit processor.

- CLKI is a clock input which is required by the S1D13706 Host Bus Interface as a source for its internal bus and memory clocks. This clock is typically driven by the host CPU system clock.
- The address inputs AB[16:0] connect directly to the 8-bit processor address lines (A[16:0). If the specific 8-bit processor cannot implement all 17 address lines required by the S1D13706, only a portion of the 80K byte S1D13706 display buffer is accessible. For example, if only AB[15:0] are supported, only the first 64K byte of the display buffer is available.
- The data bus DB[15:0] must be connected so that the 8-bit processor data lines (D[7:0]) are connected to both DB[15:8] and DB[7:0] of the S1D13706. CNF4 must be set to select little endian mode.
- Chip Select (CS#) is driven by decoding the high-order address lines to select the proper register and memory address space.
- M/R# (memory/register) selects between memory or register accesses. This signal may be connected to an address line, allowing system address A17 to be connected to the M/R# line.

  Note
  If A17 is unavailable on the 8-bit processor, an external decode must be used to generate the M/R# signal.

- BHE# is the high byte enable for both read and write cycles and connects to the high byte chip select signal.

  Note
  In an 8-bit environment, this signal is driven by inverting address line A0 thus indicating that odd addresses are to be read/write on the high byte of the data bus.

- WE# connects to WE# (the write enable signal) and must be driven low when the 8-bit processor is writing data to the S1D13706.
- RD# connects to RD# (the read enable signal) and must be driven low when the 8-bit processor is reading data from the S1D13706.
- WAIT# is a signal output from the S1D13706 that indicates the 8-bit processor must wait until data is ready (read cycle) or accepted (write cycle) on the host bus. Since host CPU bus accesses to the S1D13706 may occur asynchronously to the display update, it is possible that contention may occur in accessing the 13706 internal registers and/or display buffer. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete. This signal is active low and may need to be inverted if the host CPU wait state signal is active high.
- The Bus Status (BS#) and Read/Write (RD/WR#) signals are not used in this implementation of a generic 8-bit processor using the Generic #2 Host Bus Interface. These pins must be tied high (connected to HIO V_{DD}).

4 8-Bit Processor to S1D13706 Interface

4.1 Hardware Connections

The interface between the S1D13706 and an 8-bit processor requires minimal glue logic. A decoder is used to generate the chip select for the S1D13706 based on where the S1D13706 is mapped into memory. Alternatively, if the processor supports a chip select module, it can be programmed to generate a chip select for the S1D13706 without the need of an address decoder.

An inverter inverts A0 to generate the BHE# signal for the S1D13706. If the 8-bit host interface has an active high WAIT signal, it must be inverted as well.

BS# (bus start) and RD/WR# are not used by the Generic #2 Host Bus Interface and should be tied high (connected to HIO V_{DD}).

In order to support an 8-bit processor with a 16-bit peripheral, the low and high order bytes of the data bus must be connected together. The following diagram shows a typical implementation of an 8-bit processor to S1D13706 interface.

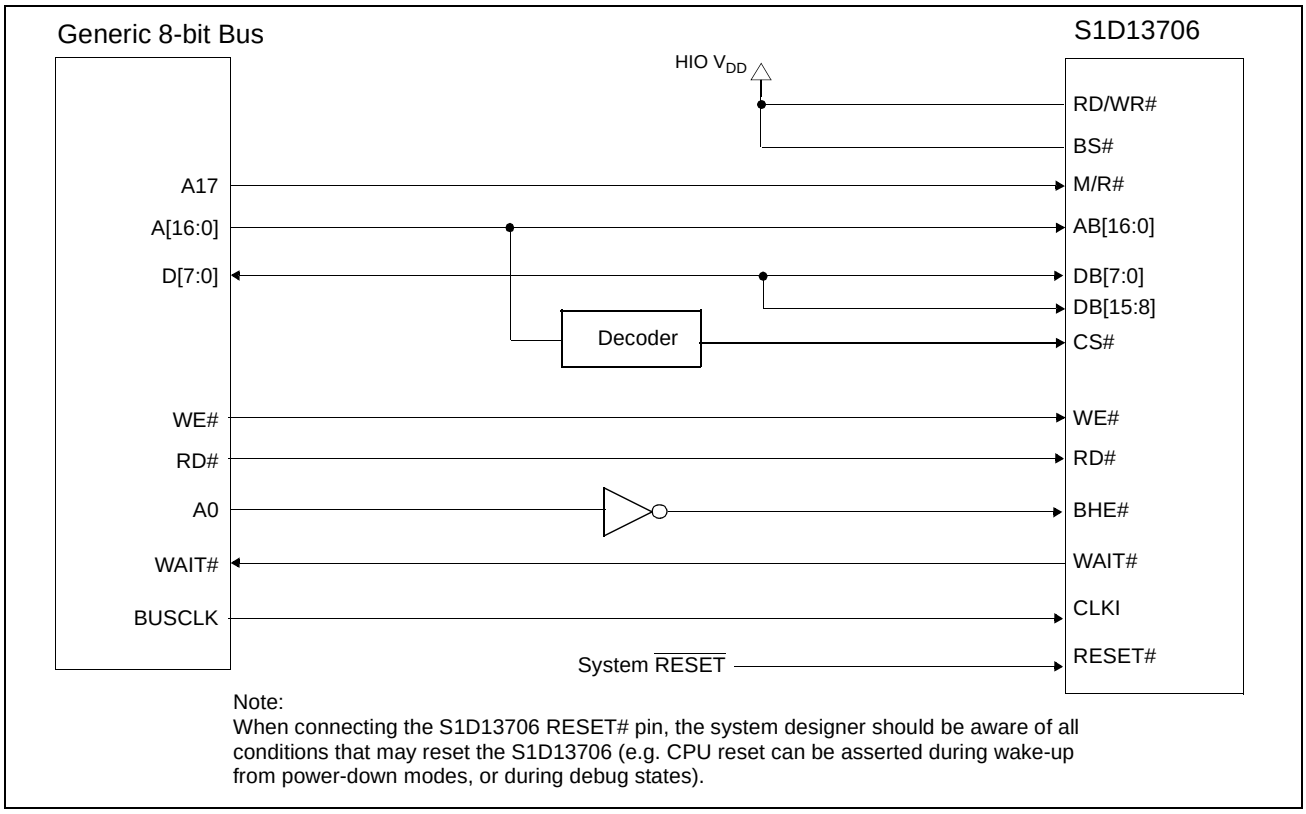

Figure 4-1: Typical Implementation of 8-bit Processor to S1D13706 Interface

4.2 S1D13706 Hardware Configuration

The S1D13706 uses CNF7 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

The following table shows the configuration required for this implementation of a S1D13706 to generic 8-bit processor.

Table 4-1: Summary of Power-On/Reset Configuration Options

S1D13706 Pin Name	value on this pin at the rising edge of RESET# is used to configure: (1/0)	
	1	0
CNF[2:0]	100 = Generic #2 Host Bus Interface	
CNF3	GPIO pins as inputs at power on	GPIO pins as HR-TFT / D-TFT outputs
CNF4	Big Endian bus interface	Little Endian bus interface
CNF5	Active high WAIT#	Active low WAIT#
CNF[7:6]	see Table 4-2: “CLKI to BCLK Divide Selection” for recommended setting	

= configuration for generic 8-bit processor

Table 4-2: CLKI to BCLK Divide Selection

CNF7	CNF6	CLKI to BCLK Divide
0	0	1:1
0	1	2:1
1	0	3:1
1	1	4:1

= recommended setting for generic 8-bit processor

4.3 Register/Memory Mapping

The S1D13706 is a memory mapped device. The S1D13706 uses two 128K byte blocks which are selected using A17 from the 8-bit processor (A17 is connected to the S1D13706 M/R# pin). The internal registers occupy the first 128K byte block and the 80K byte display buffer occupies the second 128K byte block.

An external decoder can be used to decode the address lines and generate a chip select for the S1D13706 whenever the selected 128k byte memory block is accessed. If the processor supports a general chip select module, its internal registers can be programmed to generate a chip select for the S1D13706 whenever the S1D13706 memory block is accessed.

5 Software

Test utilities and Windows® CE v2.11/2.12 display drivers are available for the S1D13706. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13706CFG, or by directly modifying the source. The Windows CE v2.11/2.12 display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13706 test utilities and Windows CE v2.11/2.12 display drivers are available from your sales support contact or on the internet at http://www.eea.epson.com.

6 References

6.1 Documents

- Epson Research and Development, Inc., *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.
- Epson Research and Development, Inc., *S5U13706B00C Rev. 1.0 Evaluation Board User Manual*, document number X31B-G-004-xx.
- Epson Research and Development, Inc., *S1D13706 Programming Notes and Examples*, Document Number X31B-G-003-xx.

6.2 Document Sources

- Epson Research and Development website: http://www.erd.epson.com

7 Technical Support

7.1 EPSON LCD Controllers (S1D13706)

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway
San Jose, CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117