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S1D13706 Embedded Memory LCD Controller

13706CFG Configuration Program

Document Number: X31B-B-001-03

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13706CFG

13706CFG is an interactive Windows® 9x/ME/NT/2000 program that calculates register values for a user defined S1D13706 configuration. The configuration information can be used to directly alter the operating characteristics of the S1D13706 utilities or any program built with the Hardware Abstraction Layer (HAL) library. Alternatively, the configuration information can be saved in a variety of text file formats for use in other applications.

S1D13706 Supported Evaluation Platforms

13706CFG runs on PC system running Windows 9x/ME/NT/2000 and can modify the executable files for the following evaluation platforms:

- PC system with an Intel 80x86 processor.
- M68EC000IDP (Integrated Development Platform) board, revision 3.0, with a Motorola M68EC000 processor.
- MC68030IDP (Integrated Development Platform) board, revision 3.0, with a Motorola MC68030 processor.
- SH3-LCEVB board, revision B, with an Hitachi SH-3 HD6417780 processor.
- MPC821ADS (Applications Development System) board, revision B, with a Motorola MPC821 processor.

Installation

Create a directory for **13706cfg.exe** and the S1D13706 utilities. Copy the files **13706cfg.exe** and **panels.def** to that directory. **Panels.def** contains configuration information for a number of panels and must reside in the same directory as **13706cfg.exe**.

Usage

13706CFG can be started from the Windows desktop or from a Windows command prompt.

To start 13706CFG from the Windows desktop, double click the program icon or the link icon if one was created during installation.

To start 13706CFG from a Windows command prompt, change to the directory **13706cfg.exe** was installed to and type the command **13706cfg**.

The basic procedure for using 13706CFG is:

1. Start 13706CFG as described above.
2. Open an existing file to serve as a starting reference point (this step is optional).
3. Modify the configuration. For specific information on editing the configuration, see “13706CFG Configuration Tabs” on page 7.
4. Save the new configuration. The configuration information can be saved in two ways; as an ASCII text file or by modifying the executable image on disk.

   Several ASCII text file formats are supported. Most are formatted C header files used to build display drivers or standalone applications.

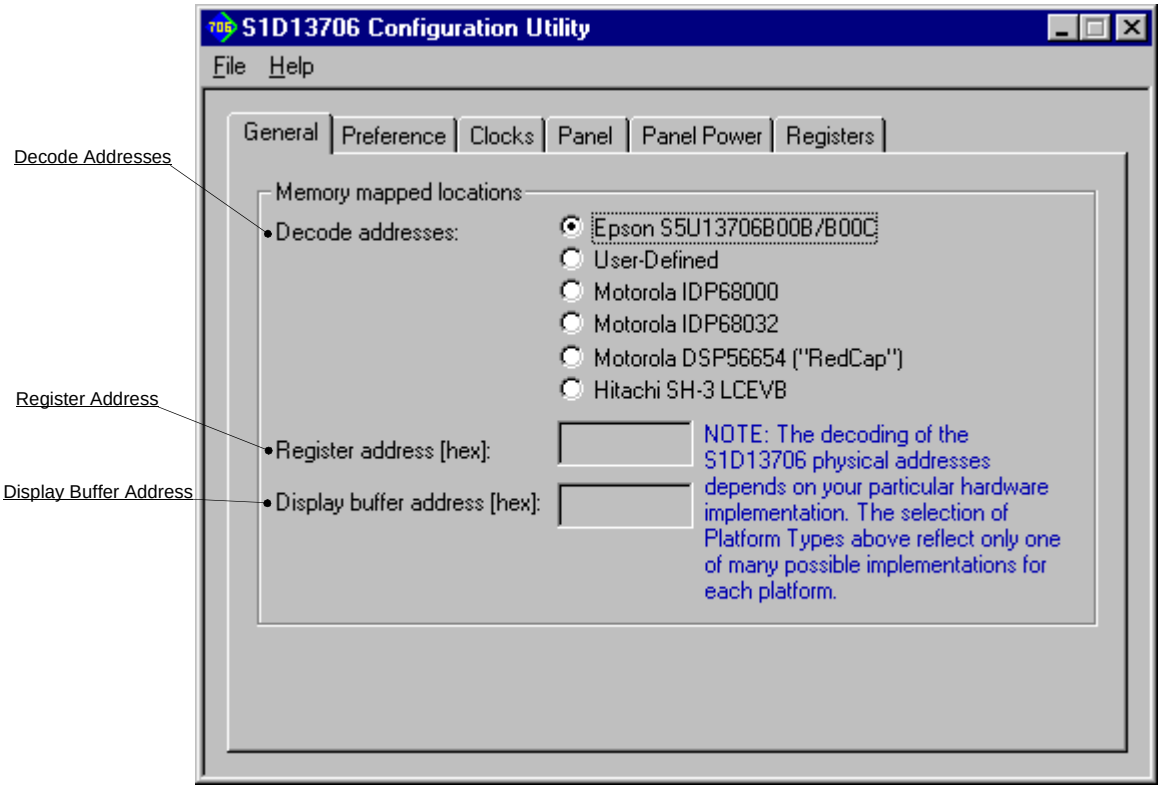
   Utility files based on the Hardware Abstraction Layer (HAL) can be modified directly by 13706CFG.

13706CFG Configuration Tabs

13706CFG provides a series of tabs which can be selected at the top of the main window. Each tab allows the configuration of a specific aspect of S1D13706 operation.

The tabs are labeled “General”, “Preference”, “Clocks”, “Panel”, “Panel Power”, and “Registers”. The following sections describe the purpose and use of each of the tabs.

General Tab



The General tab contains S1D13706 evaluation board specific information. The values presented are used for configuring HAL based executable utilities. The settings on this tab specify where in CPU address space the registers and display buffer are located.

Decode Addresses

Selecting one of the listed evaluation platforms changes the values for the “Register address” and “Display buffer address” fields. The values used for each evaluation platform are examples of possible implementations as used by the Epson S1D13706 evaluation board. If your hardware implementation differs from the addresses used, select the User-Defined option and enter the correct addresses for “Register address” and “Display buffer address”.

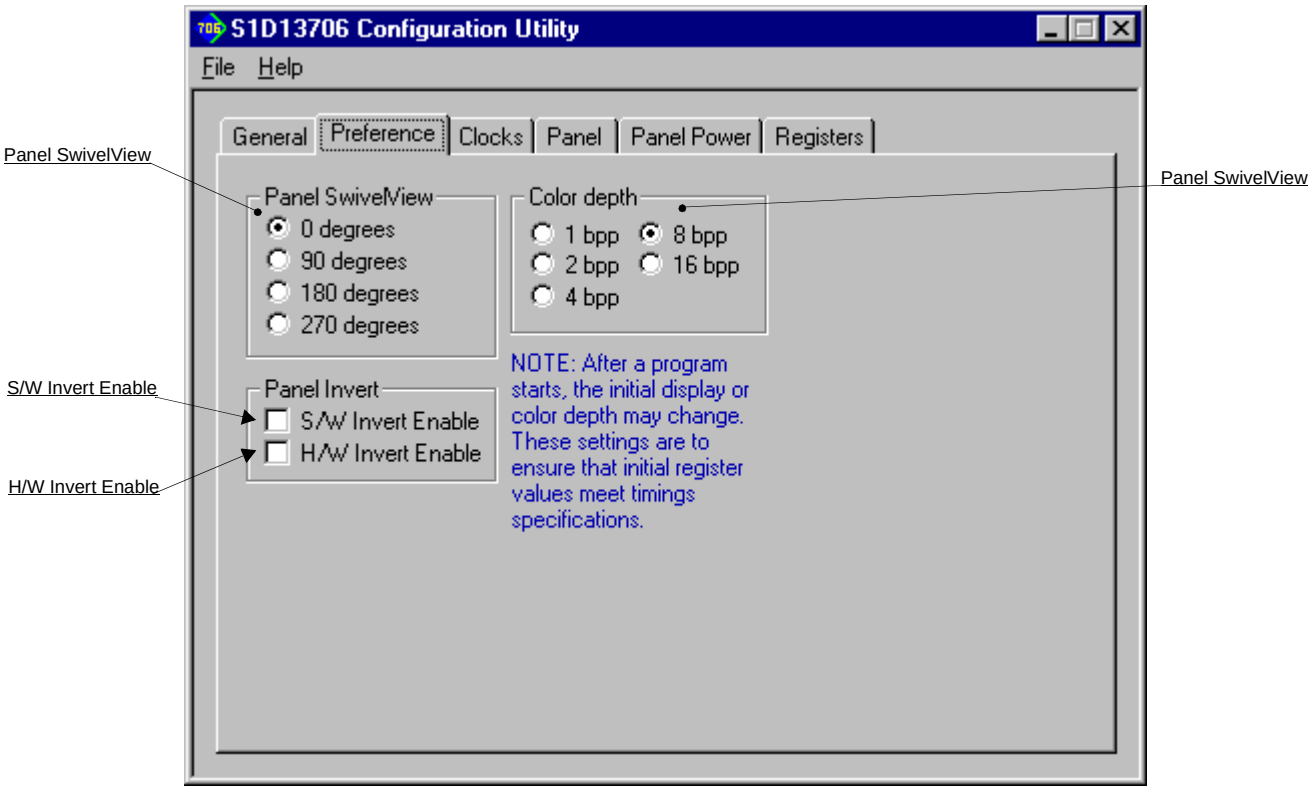
Register Address	The physical address of the start of register decode space (in hexadecimal). This field is automatically set according to the Decode Address unless the “User-Defined” decode address is selected.
Display Buffer Address	The physical address of the start of display buffer decode space (in hexadecimal). This field is automatically set according to the Decode Address unless the “User-Defined” decode address is selected.

Note

When “Epson S5U13706B00B/B00C Evaluation Board” is selected, the register and display buffer addresses are blanked because the evaluation board uses the PCI interface and the decode addresses are determined by the system BIOS during boot-up.

If using the S1D13706 Evaluation Board on a PCI based platform, both Windows and the **S1D13XXX** device driver must be installed. For further information on the S1D13xxx device driver, see the *S1D13XXX 32-bit Windows Device Driver Installation Guide*, document number X00A-E-003-xx.

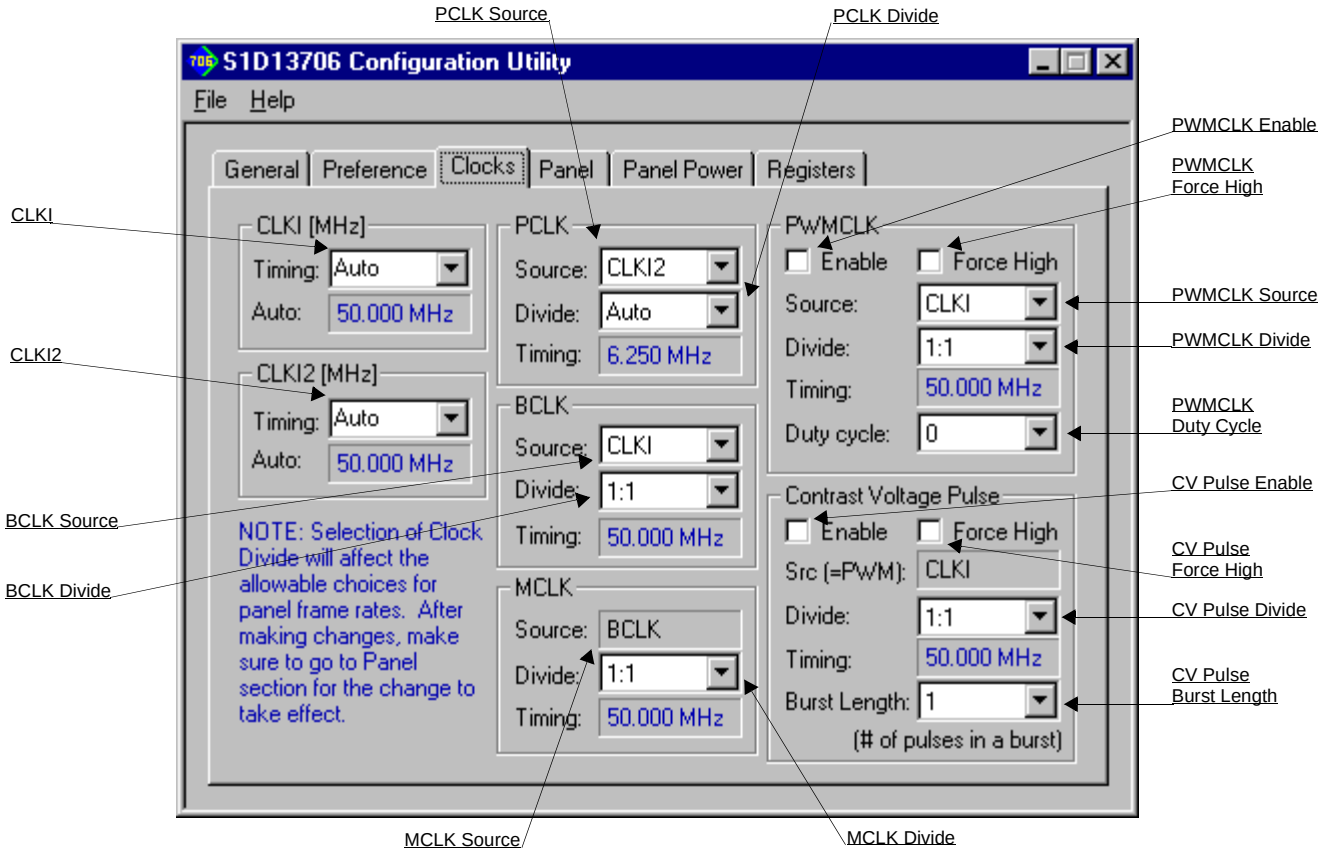
Preferences Tab



The Preference tab contains settings pertaining to the initial display state. During runtime these settings may be changed.

Panel SwivelView	The S1D13706 SwivelView feature is capable of rotating the image displayed on an LCD panel 90°, 180°, or 270° in a counter-clockwise direction. This sets the initial orientation of the panel.
Panel Invert	The S1D13706 can invert the display data going to the LCD panel. The display data is inverted after the Look-Up Table.
S/W Invert Enable	The Video Invert feature can be controlled by software using REG[70h] bit 4. When this box is checked, the Software Video Invert bit is set to one and video data is inverted. If the box is unchecked, the bit is set to zero and video data remains normal.
H/W Invert Enable	The Video Invert feature can be controlled by hardware if the GPIO0 is available. Hardware control is not possible if a HR-TFT or D-TFD panel is used as both panels use GPIO0 as an LCD control signal.
Panel Color Depth	Sets the initial color depth on the LCD panel.

Clocks Tab



The Clocks tab is intended to simplify the selection of input clock frequencies and the source of internal clocking signals. For further information regarding clocking and clock sources, refer to the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx.

In automatic mode the values for CLKI and CLKI2 are calculated based on selections made for LCD timings from the Panel tab. In this mode, the required frequencies for the input clocks are displayed in blue in the “Auto” section of each group. It is the responsibility of the system designer to ensure that the correct CLKI frequencies are supplied to the S1D13706.

Making a selection other than “Auto” indicates that the values for CLKI or CLKI2 are known and are fixed by the system design. Options for LCD frame rates are limited to ranges determined by the clock values.

Note

Changing clock values may modify or invalidate Panel settings. Confirm all settings on the Panel tab after modifying any clock settings.

The S1D13706 may use as many as two input clocks or as few as one. The more clocks used the greater the flexibility of choice in display type and memory speed.

CLKI

This setting determines the frequency of CLKI.

Select “Auto” to have the CLKI frequency determined automatically based on settings made on other configuration tabs. After completing the other configurations, the required CLKI frequency will be displayed in blue in the Auto section.

If the system design requires the CLKI frequency to be fixed at a particular rate, set this value by selecting a preset frequency from the drop down list or entering the desired frequency in MHz.

CLKI2

This setting determines the frequency of CLKI2.

Select “Auto” to have the CLKI2 frequency determined automatically based on settings made on other configuration tabs. After completing the other configurations, the required CLKI2 frequency will be displayed in blue in the Auto section.

If the system design requires the CLKI2 frequency to be fixed at a particular rate, set this value by selecting a preset frequency from the drop down list or entering the desired frequency in MHz.

PCLK

These settings select the clock signal source and divisor for the pixel clock (PCLK).

Source

Selects the PCLK source. Possible sources include CLKI, CLKI2, BCLK or MCLK.

Divide

Specifies the divide ratio for the clock source signal. The divide ratio is applied to the PCLK source to derive PCLK.

Selecting “Auto” for the divisor allows the configuration program to calculate the best clock divisor. Unless a very specific clocking is being specified, it is best to leave this setting on “Auto”.

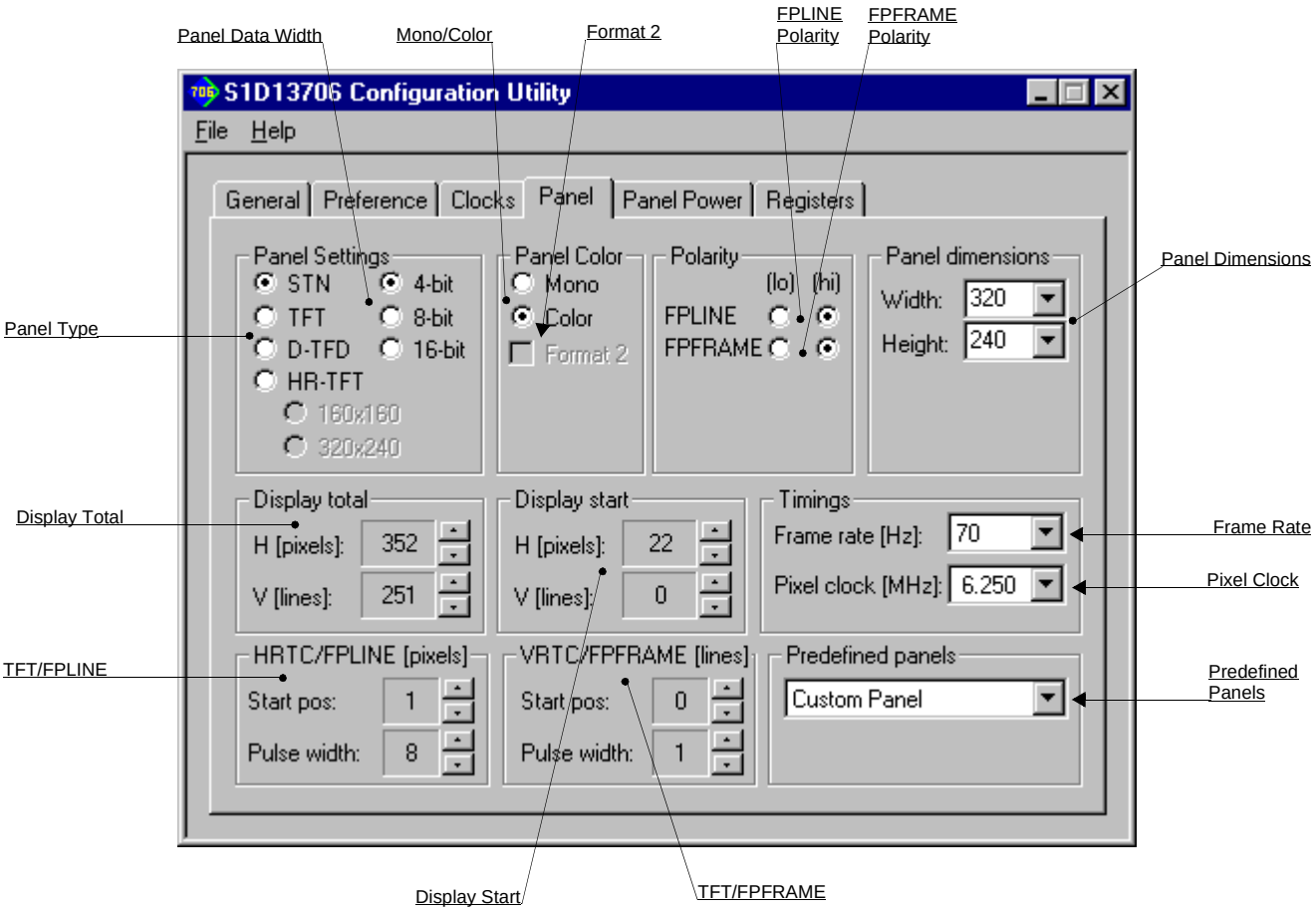
Timing

This field shows the actual PCLK used by the configuration process.

BCLK	These settings select the clock signal source and divisor for the bus interface clock (BCLK).
Source	The BCLK source is CLKI.
Divide	Specifies the divide ratio for the clock source signal. The divide ratio is applied to the BCLK source to derive BCLK.
Timing	This field shows the actual BCLK frequency used by the configuration process.
MCLK	These settings select the clock signal source and input clock divisor for the memory clock (MCLK). MCLK should be set as close to the maximum (50 MHz) as possible.
Source	The MCLK source is BCLK.
Divide	Specifies the divide ratio for the clock source signal. The divide ratio is applied to the MCLK source to derive MCLK. This divide ratio should be left at 1:1 unless the resultant MCLK is greater that 50MHz.
Timing	This field shows the actual MCLK frequency used by the configuration process.

PWMCLK	These controls configure various PWMCLK settings. The PWMCLK is the internal clock used by the Pulse Width Modulator for output to the panel.
Enable	When this box is checked, the PWMCLK circuitry is enabled.
Force High	The signal PWMOUT is forced high when this box is checked. PWMOUT is forced low when this box is not checked and Enable is not checked
Source	Selects the PWMCLK source. Possible sources include CLKI and CLKI2.
Divide	Specifies the divide ratio for the clock source signal. The divide ratio is applied to the PWMCLK source to derive PWMCLK.
Timing	This field shows the actual PWMCLK frequency used by the configuration process.
Duty Cycle	Selects the number of cycles that PWMOUT is high out of 256 clock periods.
Contrast Voltage Pulse	These controls configure various Contrast Voltage (CV) Pulse settings. The CV Pulse is provided for panels which support the contrast voltage function.
Enable	When this box is checked, the CV Pulse circuitry is enabled.
Force High	The signal CVOUT is forced high when this box is checked. CVOUT is forced low when this box is not checked and CVOUT is not enabled.
Source	The CV Pulse uses the same source clock as the PWMCLK.
Divide	Specifies the divide ratio for the clock source signal. The divide ratio is applied to the CVOUT Pulse clock source to derive the CV Pulse clock frequency.
Timing	This field shows the actual CV Pulse frequency used by the configuration process.
Burst Length	The number of pulses generated in a single CV Pulse burst.

Panel Tab



The S1D13706 supports many panel types. This tab allows configuration of most panel settings such as panel dimensions, type and timings.

Panel Type

Selects between passive (STN) and active (TFT/D-TFD/HR-TFT) panel types.

Several options may change or become unavailable when the STN/TFT setting is switched. Therefore, confirm all settings on this tab after the Panel Type is changed.

Panel Data Width

Selects the panel data width. Panel data width is the number of bits of data transferred to the LCD panel on each clock cycle and shouldn't be confused with color depth which determines the number of displayed colors.

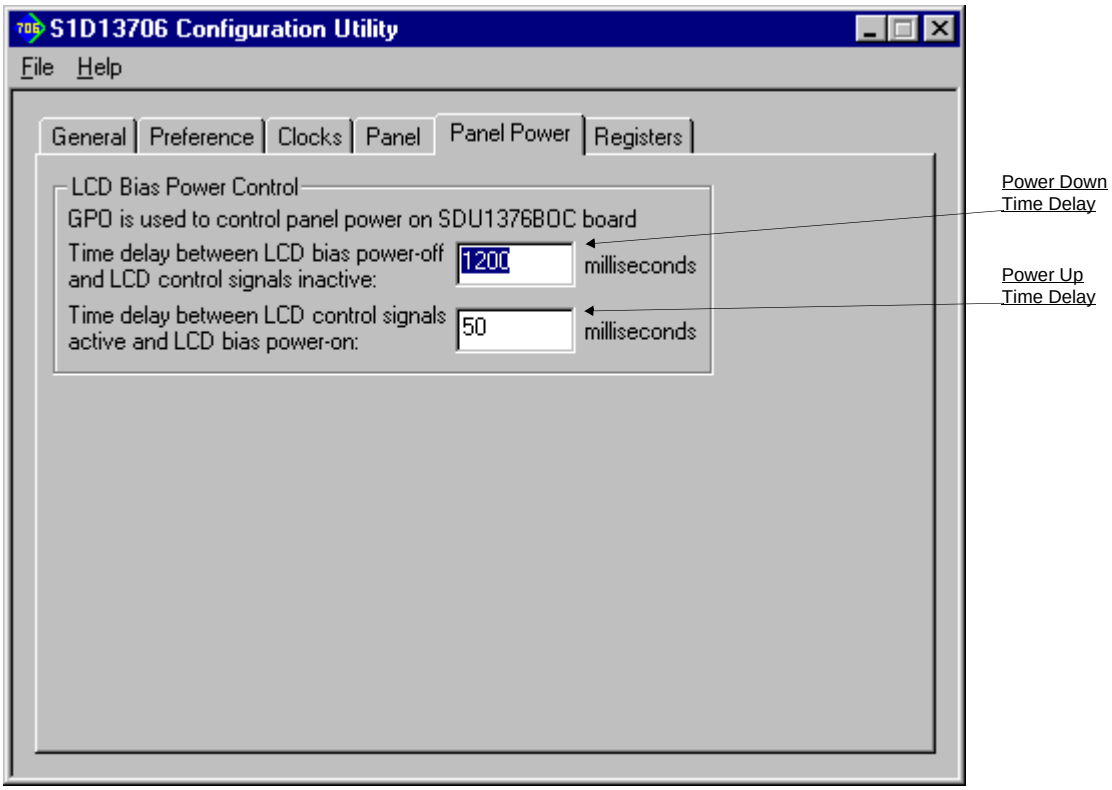
When the panel type is STN, the available options are 4, 8, and 16 bit. When an active panel type is selected the available options are 9, 12, and 18 bit.

Mono / Color	Selects between a monochrome or color panel.
Format 2	Selects color STN panel format 2. This option is specifically for configuring 8-bit color STN panels. See the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx, for description of format 1 / format 2 data formats. Most new panels use the format 2 data format.
FPLINE Polarity	Selects the polarity of the FPLINE pulse. Refer to the panel specification for the correct polarity of the FPLINE pulse.
FPFRAME Polarity	Selects the polarity of the FPFRAME pulse. Refer to the panel specification for the correct polarity of the FPFRAME pulse.
Panel Dimensions	These fields specify the panel width and height. A number of common widths and height are available in the selection boxes. If the width/height of your panel is not listed, enter the actual panel dimensions into the edit field. For passive panels, manually entered pixel widths must be a minimum of 32 pixels and can be increased by multiples of 16. For TFT panels, manually entered pixel widths must be a minimum of 16 pixels and can be increased by multiples of 8. If a value is entered that does not match these requirements, a notification box appears and 13706CFG rounds up the value to the next allowable width.
Display Total	It is recommended that these automatically generated Display Total values be used without adjustment. However, manual adjustment may be useful in fine tuning the horizontal and vertical display totals. The display total equals the display period plus the non-display period.
Display Start	It is recommended that these automatically generated Display Start values be used without adjustment. However, manual adjustment may be useful in fine tuning the horizontal and vertical display start positions. For passive panels these values must always be 0.

Frame Rate	Select the desired frame rate (in Hz) from the drop-down list. The values in the list are the range of possible frame rates using the currently selected pixel clock. To change the range of frame rates, select a different Pixel Clock rate (in MHz). Panel dimensions are fixed therefore frame rate can only be adjusted by changing either PCLK or non-display period values. Higher frame rates correspond to smaller horizontal and vertical non-display values, or higher frequencies.
Pixel Clock	Select the desired Pixel Clock (in MHz) from the drop-down list. The range of frequencies displayed is dependent on settings selected on the Clocks tab. For example: If CLKI is chosen to be Auto and PCLK is sourced from CLKI on the Clocks tab, then the range for Pixel Clock will range from 1.5 MHz to 80 MHz. Selecting a fixed PCLK on the Clocks tab, say 25.175 MHz, will result in only four selections: 6.293, 8.392, 12.587, and 25.175 MHz. (these frequencies represent the four possible frequencies from a fixed 25.175 MHz input clock divided by the PCLK divider).
TFT/FPLINE (pixels)	These settings allow fine tuning of the TFT line pulse parameters and are only available when the selected panel type is TFT/D-TFD/HR-TFT. Refer to *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx for a complete description of the FPLINE pulse settings. Start pos - Specifies the delay (in pixels) from the start of the horizontal non-display period to the leading edge of the FPLINE pulse. Pulse Width - Specifies the delay (in pixels) from the start of the horizontal non-display period to the leading edge of the FPLINE pulse.

TFT/FPFRAME (lines)	These settings allow fine tuning of the TFT frame pulse parameters and are only available when the selected panel type is TFT/D-TFD/HR-TFT. Refer to *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx, for a complete description of the FPFRAME pulse settings. Start pos - Specify the delay (in lines) from the start of the vertical non-display period to the leading edge of the FPFRAME pulse. Pulse width - Specifies the pulse width (in lines) of the FPFRAME output signal.
Predefined Panels	13706CFG uses a file (**panels.def**) which lists various panel manufacturers recommended settings. If the file **panels.def** is present in the same directory as **13706cfg.exe**, the settings for a number of predefined panels are available in the drop-down list. If a panel is selected from the list, 13706CFG loads the predefined settings contained in the file.

Panel Power Tab



The S5U13706B00C evaluation board is designed to use the GPO signal to control the LCD bias power. The following settings allow configuration of the necessary delays.

Power Down Time Delay

This setting controls the time delay between when the LCD panel is powered-off and when the S1D13706 control signals are turned off. This setting must be configured according to the specification for the panel being used.

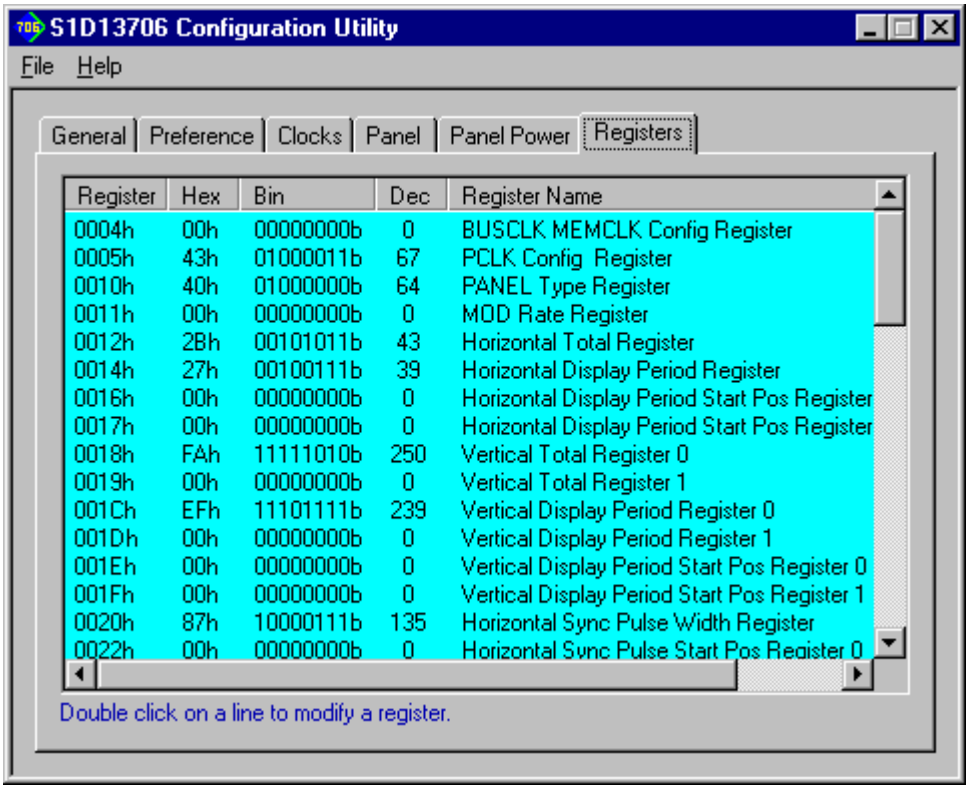
This value is only used by Epson evaluation software designed for the S5U13706B00C evaluation board.

Power Up Time Delay

This setting controls the time delay between when the S1D13706 control signals are turned on and the LCD panel is powered-on. This setting must be configured according to the specification for the panel being used.

This value is only used by Epson evaluation software designed for the S5U13706B00C evaluation board.

Registers Tab



Register	Hex	Bin	Dec	Register Name
0004h	00h	00000000b	0	BUSCLK MEMCLK Config Register
0005h	43h	01000011b	67	PCLK Config Register
0010h	40h	01000000b	64	PANEL Type Register
0011h	00h	00000000b	0	MOD Rate Register
0012h	2Bh	00101011b	43	Horizontal Total Register
0014h	27h	00100111b	39	Horizontal Display Period Register
0016h	00h	00000000b	0	Horizontal Display Period Start Pos Register
0017h	00h	00000000b	0	Horizontal Display Period Start Pos Register
0018h	FAh	11111010b	250	Vertical Total Register 0
0019h	00h	00000000b	0	Vertical Total Register 1
001Ch	EFh	11101111b	239	Vertical Display Period Register 0
001Dh	00h	00000000b	0	Vertical Display Period Register 1
001Eh	00h	00000000b	0	Vertical Display Period Start Pos Register 0
001Fh	00h	00000000b	0	Vertical Display Period Start Pos Register 1
0020h	87h	10000111b	135	Horizontal Sync Pulse Width Register
0022h	00h	00000000b	0	Horizontal Sync Pulse Start Pos Register 0

The Registers tab allows viewing and direct editing the S1D13706 register values.

Scroll up and down the list of registers and view their configured value based on the settings the previous tabs. Individual register settings may be changed by double-clicking on the register in the listing. **Manual changes to the registers are not checked for errors, so caution is warranted when directly editing these values.** It is strongly recommended that the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx be referred to before making an manual register settings.

Manually entered values may be changed by 13706CFG if further configuration changes are made on the other tabs. In this case, the user is notified.

Note

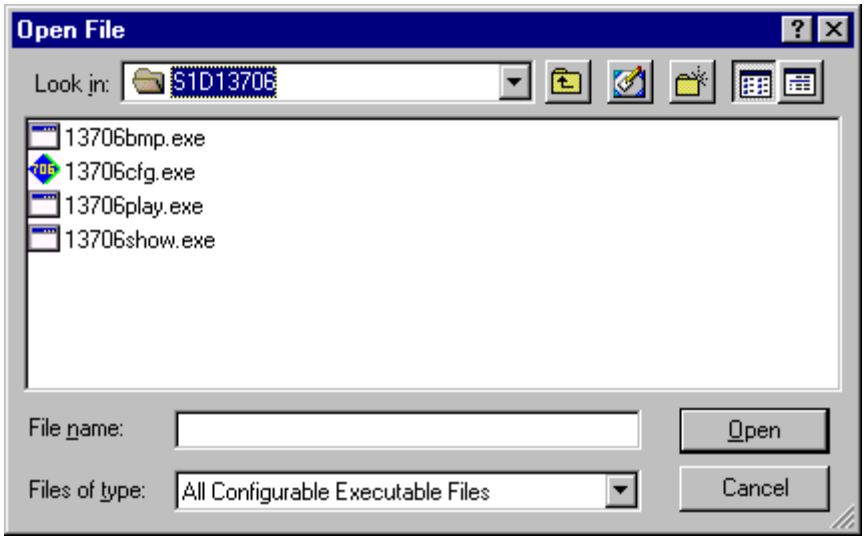
Manual changes to the registers may have unpredictable results if incorrect values are entered.

13706CFG Menus

The following sections describe each of the options in the File and Help menus.

Open...

From the Menu Bar, select “File”, then “Open...” to display the Open File Dialog Box.



The Open option allows 13706CFG to open files containing HAL configuration information. When 13706CFG opens a file it scans the file for an identification string, and if found, reads the configuration information. This may be used to quickly arrive at a starting point for register configuration. The only requirement is that the file being opened must contain a valid S1D13706 HAL library information block.

13706CFG supports a variety of executable file formats. Select the file type(s) 13706CFG should display in the Files of Type drop-down list and then select the filename from the list and click on the Open button.

Note

13706CFG is designed to work with utilities programmed using a given version of the HAL. If the configuration structure contained in the executable file differs from the version 13706CFG expects the Open will fail and an error message is displayed. This may happen if the version of 13706CFG is substantially older, or newer, than the file being opened.

Save

From the Menu Bar, select “File”, then “Save” to initiate the save action. The Save menu option allows a fast save of the configuration information to a file that was opened with the Open menu option.

Note

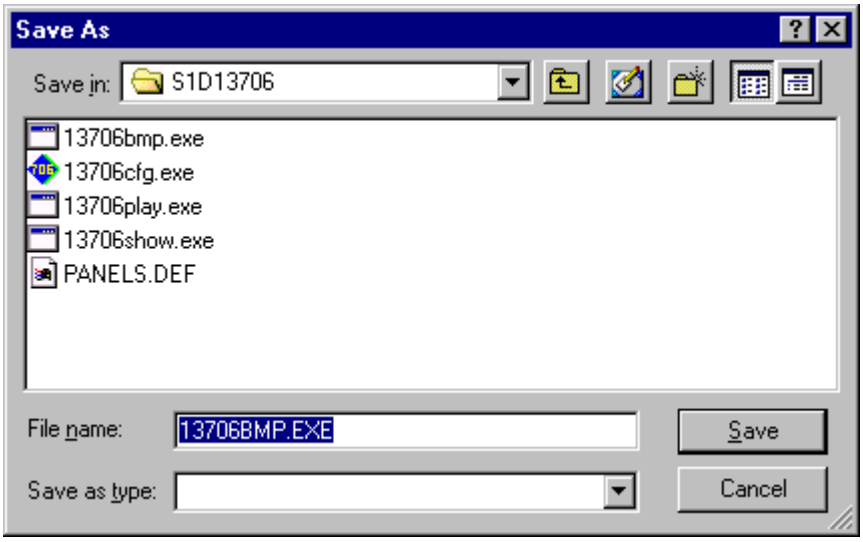
This option is only available once a file has been opened.

Note

13706cfg.exe can be configured by making a copy of the file 13706cfg.exe and configuring the copy. It is not possible to configure the original while it is running.

Save As...

From the Menu Bar, select “File”, then “Save As...” to display the Save As Dialog Box.



“Save as” is very similar to Save except a dialog box is displayed allowing the user to name the file before saving.

Using this technique a tester can configure a number of files differing only in configuration information and name (e.g. BMP60Hz.EXE, BMP72Hz.EXE, BMP75Hz.EXE where only the frame rate changes in each of these files).

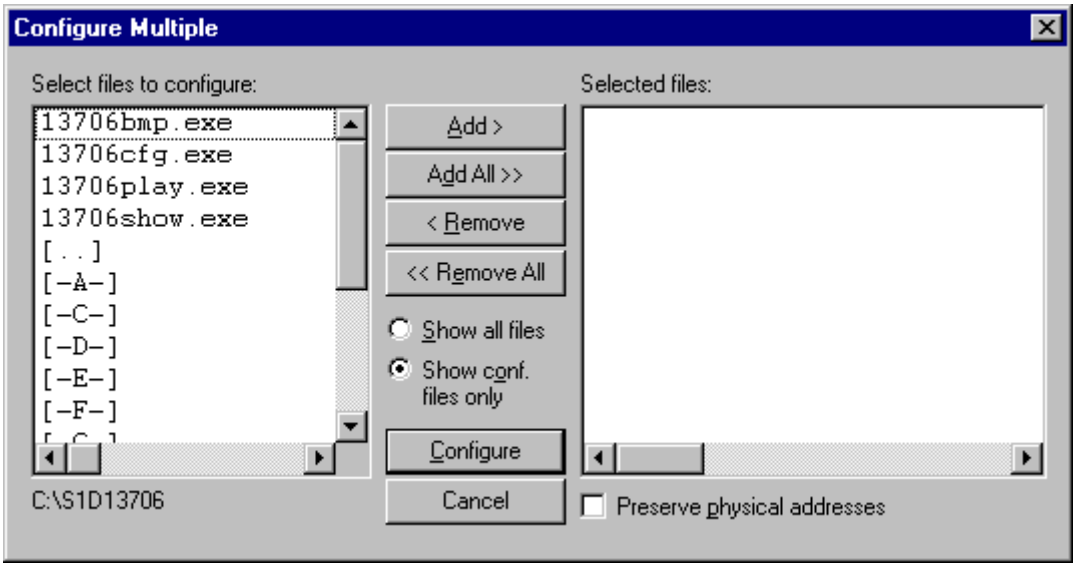
Note

When “Save As” is selected then an exact duplicate of the file as opened by the “Open” option is created containing the new configuration information.

Configure Multiple

After determining the desired configuration, “Configure Multiple” allows the information to be saved into one or more executable files built with the HAL library.

From the Menu Bar, select “File”, then “Configure Multiple” to display the Configure Multiple Dialog Box.This dialog box is also displayed when a file(s) is dragged onto the 13706CFG window.



The left pane lists files available for configuration; the right pane lists files that have been selected for configuration. Files can be selected by clicking the “Add” or “Add All” buttons, double clicking any file in the left pane, or by dragging the file(s) from Windows Explorer.

Selecting “Show all files” displays all files in the selected directory, whereas selecting “Show conf. files only” will display only files that can be configured using 13706CFG (i.e. .exe, .s9, .elf).

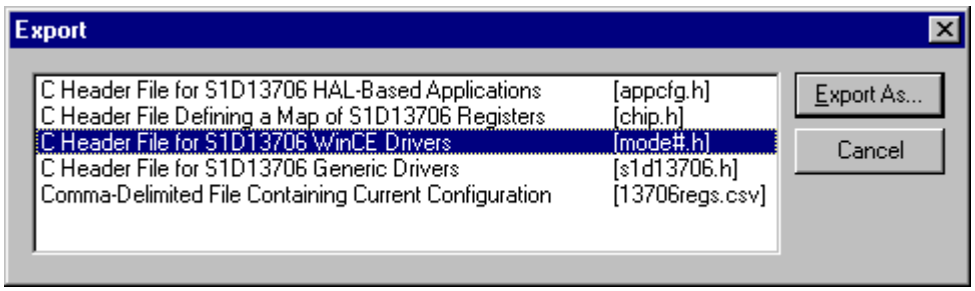
The configuration values can be saved to a specific EXE file for Intel platforms, or to a specific S9 or ELF file for non-Intel platforms. The file must have been compiled using the 13706 HAL library.

Checking “Preserve Physical Addresses” instructs 13706CFG to use the register and display buffer address values the files were previously configured with. Addresses specified in the General Tab are discarded. This is useful when configuring several programs for various hardware platforms at the same time. For example, if configuring PCI, MPC and IDP based programs at the same time for a new panel type, the physical addresses for each are retained. This feature is primarily intended for the test lab where multiple hardware configurations exist and are being tested.

Export

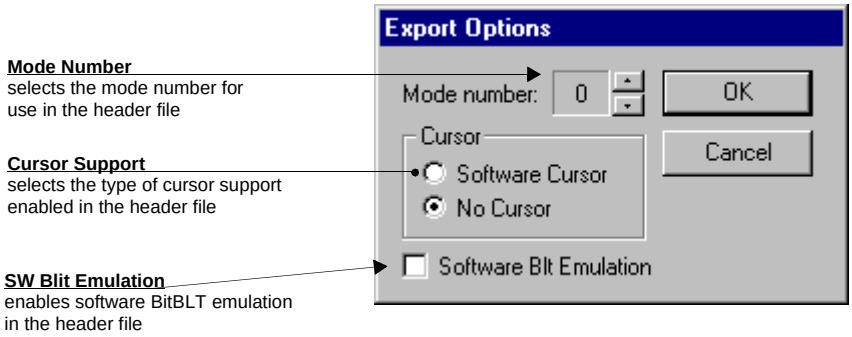
After determining the desired configuration, “Export” permits the user to save the register information as a variety of ASCII text file formats. The following is a list and description of the currently supported output formats:

- a C header file for use in writing HAL library based applications.
- a C header file which lists each register and the value it should be set to.
- a C header file for use in developing Window CE display drivers.
- a C header file for use in developing display drivers for other operating systems such as Linux, QNX, and VxWorks UGL or WindML.
- a comma delimited text file containing an offset, a value, and a description for each S1D13706 register.



After selecting the file format, click the “Export As..." button to display the file dialog box which allows the user to enter a filename before saving. Before saving the configuration file, clicking the “Preview” button starts Notepad with a copy of the configuration file about to be saved.

When the **C Header File for S1D13706 WinCE Drivers** option is selected as the export type, additional options are available and can be selected by clicking on the Options button. The options dialog appears as:



Enable Tooltips

Tooltips provide useful information about many of the items on the configuration tabs. Placing the mouse pointer over nearly any item on any tab generates a popup window containing helpful advice and hints.

To enable/disable tooltips check/uncheck the “Tooltips” option form the “Help” menu.

Note

Tooltips are enabled by default.

ERD on the Web

This “Help” menu item is actually a hotlink to the Epson Research and Development website. Selecting “Help” then “ERD on the Web” starts the default web browser and points it to the ERD product web site.

The latest software, drivers, and documentation for the S1D13706 is available at this website.

About 13706CFG

Selecting the “About 13706CFG” option from the “Help” menu displays the about dialog box for 13706CFG. The about dialog box contains version information and the copyright notice for 13706CFG.

Comments

- On any tab particular options may be grayed out if selecting them would violate the operational specification of the S1D13706 (i.e. Selecting TFT or STN on the Panel tab enables/disables options specific to the panel type).
- The file **panels.def** is a text file containing operational specifications for several supported, and tested, panels. This file can be edited with any text editor.
- 13706CFG allows manually altering register values. The manual changes may violate memory and LCD timings as specified in the *S1D13706 Hardware Functional Specification*, document number X31B-A-001-xx. If this is done, unpredictable results may occur. Epson Research and Development, Inc. does not assume liability for any damage done to the display device as a result of configuration errors.