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S1D13A04 LCD/USB Companion Chip

Interfacing to the Toshiba MIPS TMPR3905/3912 Microprocessors

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1 Introduction

This application note describes the hardware and software environment necessary to provide an interface between the S1D13A04 USB/LCD Companion Chip and the Toshiba MIPS TMPR3905/3912 processors.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Research and Development website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Interfacing to the TMPR3905/12

2.1 The Toshiba TMPR3905/12 System Bus

The TMPR39XX family of processors features a high-speed system bus typical of modern MIPS RISC microprocessors. This section provides an overview of the operation of the CPU bus in order to establish interface requirements.

2.1.1 Overview

The TMPR3905/12 is a highly integrated controller developed for handheld products. The microprocessor is based on the R3900 MIPS RISC processor core. The TMPR3905/12 implements an external 26-bit address bus and a 32-bit data bus allowing it to communicate with its many peripheral units. The address bus is multiplexed (A[12:0]) using an address latch signal (ALE) which controls the driving of the address onto the address bus. The full 26-bit address bus (A[25:0]) is generated to devices not capable of receiving a multiplexed address, using external latches (controlled by ALE).

The TMPR3905/12 provides two, revision 2.01 compliant, PC Card slots. The 16-bit PC Card slots provide a 26-bit multiplexed address and additional control signals which allow access to three 64M byte address ranges: IO, memory, and attribute space. The signal CARDREG* selects memory space when high and attribute or IO space when low. Memory and attribute space are accessed using the write and read enable signals (WE* and RD*). When CARDREG* is low, card IO space is accessed using separate write (CARDIOWR*) and read (CARDIORD*) control signals.

2.1.2 Card Access Cycles

A data transfer is initiated when the address is placed on the PC Card bus and one, or both, of the card enable signals (CARD1CSL* and CARD1CSH*) are driven low. CARDREG* is inactive for memory and IO cycles. If only CARD1CSL* is driven low, 8-bit data transfers are enabled and A0 specifies whether the even or odd data byte appears on the PC Card data bus lines D[7:0]. If only CARD1CSH* is driven low, an odd byte transfer occurs on PC Card data lines D[15:8]. If both CARD1CSL* and CARD1CSH* are driven low, a 16-bit word transfer takes place on D[15:0].

During a read cycle, either RD* or CARDIORD* is driven low depending on whether a memory or IO cycle is specified. A write cycle is specified by driving WE* (memory cycle) or CARDIOWR* (IO cycle) low. The cycle can be lengthened by driving CARD1WAIT* low for the time required to complete the cycle.

Figure 2-1: “Toshiba 3905/12 PC Card Memory/Attribute Cycle,” illustrates a typical memory/attribute cycle on the Toshiba 3905/12 PC Card bus.

Figure 2-1: Toshiba 3905/12 PC Card Memory/Attribute Cycle

Figure 2-2: “Toshiba 3905/12 PC Card IO Cycle,” illustrates a typical IO cycle on the Toshiba 3905/12 PC Card bus.

Figure 2-2: Toshiba 3905/12 PC Card IO Cycle

3 S1D13A04 Host Bus Interface

The S1D13A04 directly supports multiple processors. The S1D13A04 implements a 16-bit Generic #2 Host Bus Interface which is most suitable for connection to the Toshiba TMPR3905/12 microprocessor.

The Generic #2 Host Bus Interface is selected by the S1D13A04 on the rising edge of RESET#. After releasing reset the bus interface signals assume their selected configuration. For details on the S1D13A04 configuration, see Section 4.2, “S1D13A04 Hardware Configuration” on page 14.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13A04 Pin Names	Toshiba TMPR3905/12
AB[17:0]	External Decode
DB[15:8]	D[23:16]
DB[7:0]	D[31:24]
WE1#	External Decode
CS#	External Decode
M/R#	External Decode
CLKI	DCLKOUT
BS#	Connect to IO_{VDD} from the S1D13A04
RD/WR#	Connect to IO_{VDD} from the S1D13A04
RD#	CARDIORD*
WE0#	CARDIOWR*
WAIT#	CARD1WAIT*
RESET#	system $\overline{RESET}$

3.2 Host Bus Interface Signals

The Host Bus Interface requires the following signals.

- CLKI is a clock input required by the S1D13A04 Host Bus Interface as a source for its internal bus and memory clocks. This clock is typically driven by the host CPU system clock. For example, DCLKOUT from the Toshiba TMPR3905/12.
- The address inputs AB[12:0] are connected directly to the TMPR3905/12 address bus. Since the TMPR3905/12 has a multiplexed address bus, the other address inputs A[17:13] must be generated using an external latch controlled by the address latch enable signal (ALE). The low data byte on the TMPR3905/12 data bus for 16-bit ports is D[31:24] and connects to the S1D13A04 low data byte, D[7:0]. The high data byte on the TMPR3905/12 data bus for 16-bit ports is D[23:16] and connects to the S1D13A04 high data byte, D[15:0]. The hardware engineer must ensure that CNF4 selects the proper endian mode upon reset.
- Chip Select (CS#) is driven by external decoding circuitry to select the S1D13A04.
- M/R# (memory/register) selects between memory or register accesses. This signal is generated by the external address decode circuitry. For this example, M/R# is connected to address line A18, allowing system address A18 to select between memory or register accesses.
- WE1# is connected to CARD1CSH* and is the high byte enable for both read and write cycles.
- WE0# is connected to CARDIOWR* (the write enable signal) and must be driven low when the Toshiba TMPR3905/12 is writing data to the S1D13A04.
- RD# is connected to CARDIORD* (the read enable signal) and must be driven low when the Toshiba TMPR3905/12 is reading data from the S1D13A04.
- WAIT# connects to CARD1WAIT* and is a signal which is output from the S1D13A04 to the TMPR3905/12 that indicates when data is ready (read cycle) or accepted (write cycle) on the host bus. Since host CPU accesses to the S1D13A04 may occur asynchronously to the display update, it is possible that contention may occur in accessing the S1D13A04 internal registers and/or display buffer. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete.
- The Bus Status (BS#) and Read/Write (RD/WR#) signals are not used in this implementation of the Toshiba TMPR3905/12 using the Generic #2 Host Bus Interface. These pins must be tied high (connected to IO V_{DD}).

4 Toshiba TMPR3905/12 to S1D13A04 Interface

4.1 Hardware Description

In this implementation, the S1D13A04 occupies the TMPR3905/12 PC Card slot #1 IO address space. IO address space closely matches the timing parameters for the S1D13A04 Generic #2 Host Bus Interface.

The address bus of the TMPR3905/12 PC Card interface is multiplexed and must be demultiplexed using an advanced CMOS latch (e.g., 74AHC373).

BS# (bus start) and RD/WR# are not used in this implementation and should be tied high (connected to IO V_{DD}).

A pull-up resistor is attached to WAIT# to speed up its rise time when terminating a cycle.

The following diagram demonstrates a typical implementation of the TMPR3905/12 to S1D13A04 interface.

Figure 4-1: S1D13A04 to TMPR3905/12 Direct Connection

The Generic #2 Host Bus Interface control signals of the S1D13A04 are asynchronous with respect to the S1D13A04 bus clock. This gives the system designer full flexibility to choose the appropriate source (or sources) for CLKI and CLKI2. The choice of whether both clocks should be the same, and whether to use DCLKOUT (divided) as clock source, should be based on the desired:

- pixel and frame rates.
- power budget.
- part count.
- maximum S1D13A04 clock frequencies.

The S1D13A04 also has internal clock dividers providing additional flexibility.

4.2 S1D13A04 Hardware Configuration

The S1D13A04 latches CNF6 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.

The table below shows the configuration settings important to the Generic #2 host bus interface used by the Toshiba TMPR3905/12.

Table 4-1: Summary of Power-On/Reset Options

S1D13A04 Configuration Input	Power-On/Reset State	
	1 (connected to IO V_{DD})	**0 (connected to V_{SS})**
CNF4, CNF[2:0]	Select host bus interface as follows: **CNF4** 0 **CNF2** 1 **CNF1** 0 **CNF0** 0 — **Host Bus** Generic #2, Little Endian	
CNF3	Reserved. Must be set to 1.	
CNF5	WAIT# is active high	WAIT# is active low
CNF6	CLKI to BCLK divide ratio 2:1	CLKI to BCLK divide ratio 1:1

	configuration for Toshiba TMPR3905/3912 microprocessor

4.3 Memory Mapping and Aliasing

In this implementation the TMPR3905/12 control signal CARDREG* is ignored. This means that the S1D13A04 takes up the entire PC Card slot 1.

The S1D13A04 is a memory mapped device and uses two 256K byte blocks which are selected using A18 from the TMPR3905/12 (A18 is connected to the S1D13A04 M/R# pin). The internal registers occupy the first 256K byte block and the 160K byte display buffer occupies the second 256K byte block.

The registers occupy the range 0h through 3FFFFh while the on-chip display memory occupies the range 40000h through 68000h. Demultiplexed address lines A[25:19] are ignored. Therefore, the S1D13A04 is aliased at 256K byte intervals over the 64M byte PC Card slot #1 memory space.

Note
If aliasing is undesirable, additional decoding circuitry must be added.

5 Software

Test utilities and display drivers are available for the S1D13A04. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13A04CFG (see document number X37A-B-001-xx), or by directly modifying the source. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13A04 test utilities and display drivers are available from your sales support contact (see Section 7, *"Sales and Technical Support"*) or www.erd.epson.com.

6 References

6.1 Documents

- Toshiba America Electrical Components, Inc., *TMPR3905/12 Specification*.
- Epson Research and Development, Inc., *S1D13A04 Hardware Functional Specification*, Document Number X37A-A-001-xx.
- Epson Research and Development, Inc., *S5U13A04B00C Rev. 1.0 ISA Bus Evaluation Board User Manual,* Document Number X37A-G-004-xx.
- Epson Research and Development, Inc., *S1D13A04 Programming Notes and Examples*, Document Number X37A-G-003-xx.

6.2 Document Sources

- Toshiba America Electrical Components Website: www.toshiba.com/taec.
- Epson Research and Development Website: www.erd.epson.com.

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7.2 Toshiba MIPS TMPR3905/12 Processor

http://www.toshiba.com/taec/nonflash/indexproducts.html