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S1D13A04 LCD/USB Companion Chip

Interfacing to the PC Card Bus

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1 Introduction

This application note describes the hardware and software environment required to interface the S1D13A04 LCD/USB Companion Chip and the PC Card (PCMCIA) bus.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Research and Development website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Interfacing to the PC Card Bus

2.1 The PC Card System Bus

PC Card technology has gained wide acceptance in the mobile computing field as well as in other markets due to its portability and ruggedness. This section is an overview of the operation of the 16-bit PC Card interface conforming to the PCMCIA 2.0/JEIDA 4.1 Standard (or later).

2.1.1 PC Card Overview

The 16-bit PC Card provides a 26-bit address bus and additional control lines which allow access to three 64M byte address ranges. These ranges are used for common memory space, IO space, and attribute memory space. Common memory may be accessed by a host system for memory read and write operations. Attribute memory is used for defining card specific information such as configuration registers, card capabilities, and card use. IO space maintains software and hardware compatibility with hosts such as the Intel x86 architecture, which address peripherals independently from memory space.

Bit notation follows the convention used by most microprocessors, the high bit is the most significant. Therefore, signals A25 and D15 are the most significant bits for the address and data bus respectively.

Support is provided for on-chip DMA controllers. To find further information on these topics, refer to Section 6, *"References"* on page 13.

PC Card bus signals are asynchronous to the host CPU bus signals. Bus cycles are started with the assertion of either the -CE1 and/or the -CE2 card enable signals. The cycle ends once these signals are de-asserted. Bus cycles can be lengthened using the -WAIT signal.

Note

The PCMCIA 2.0/JEIDA 4.1 (and later) PC Card Standard support the two signals -WAIT and RESET which are not supported in earlier versions of the standard. The -WAIT signal allows for asynchronous data transfers for memory, attribute, and IO access cycles. The RESET signal allows resetting of the card configuration by the reset line of the host CPU.

2.1.2 Memory Access Cycles

A data transfer is initiated when the memory address is placed on the PC Card bus and one, or both, of the card enable signals (-CE1 and -CE2) are driven low. -REG must be kept inactive. If only -CE1 is driven low, 8-bit data transfers are enabled and A0 specifies whether the even or odd data byte appears on data bus lines D[7:0]. If both -CE1 and -CE2 are driven low, a 16-bit word transfer takes place. If only -CE2 is driven low, an odd byte transfer occurs on data lines D[15:8].

During a read cycle, -OE (output enable) is driven low. A write cycle is specified by driving -OE high and driving the write enable signal (-WE) low. The cycle can be lengthened by driving -WAIT low for the time needed to complete the cycle.

Figure 2-1: illustrates a typical memory access read cycle on the PC Card bus.

Figure 2-1: PC Card Read Cycle

Figure 2-2: illustrates a typical memory access write cycle on the PC Card bus.

Figure 2-2: PC Card Write Cycle

3 S1D13A04 Host Bus Interface

The S1D13A04 directly supports multiple processors. The S1D13A04 implements a 16-bit Generic #2 Host Bus Interface which is most suitable for direct connection to the PC Card bus. Generic #2 supports an external Chip Select, shared Read/Write Enable for high byte, and individual Read/Write Enable for low byte.

The Generic #2 Host Bus Interface is selected by the S1D13A04 on the rising edge of RESET#. After RESET# is released, the bus interface signals assume their selected configuration. For details on the S1D13A04 configuration, see Section 4.2, “S1D13A04 Hardware Configuration” on page 11.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13A04 Pin Names	PC Card (PCMCIA)
AB[17:0]	A[17:0]
DB[15:0]	D[15:0]
WE1#	-CE2
CS#	External Decode
M/R#	A18
CLKI	see note
BS#	Connect to IO_{VDD} from the S1D13A04
RD/WR#	Connect to IO_{VDD} from the S1D13A04
RD#	-OE
WE0#	-WE
WAIT#	-WAIT
RESET#	Inverted RESET

Note

Although a clock is not directly supplied by the PC Card interface, one is required by the S1D13A04 Generic #2 Host Bus Interface. For an example of how this can be accomplished see the discussion on CLKI in Section 3.2, “Host Bus Interface Signals” on page 9.

3.2 Host Bus Interface Signals

The S1D13A04 Generic #2 Host Bus Interface requires the following signals from the PC Card bus.

- CLKI is a clock input which is required by the S1D13A04 Host Bus Interface as a source for its internal bus and memory clocks. This clock is typically driven by the host CPU system clock. Since the PC Card signalling is independent of any clock, CLKI can come from any oscillator already implemented. For example, the source for the CLKI2 input of the S1D13A04 may be used.
- The address inputs AB[17:0], and the data bus DB[15:0], connect directly to the PC Card address (A[17:0]) and data bus (D[15:0]), respectively. CNF4 must be set to select little endian mode.
- Chip Select (CS#) is driven by decoding the high-order address lines to select the proper register and memory address space.
- M/R# (memory/register) selects between memory or register accesses. This signal is generated by the external address decode circuitry. For this example, M/R# is connected to address line A18, allowing system address A18 to select between memory or register accesses.
- WE1# connects to -CE2 (the high byte chip select signal from the PC Card interface) which in conjunction with address bit 0 allows byte steering of read and write operations.
- WE0# connects to -WE (the write enable signal form the PC Card bus) and must be driven low when the PC Card bus is writing data to the S1D13A04.
- RD# connects to -OE (the read enable signal from the PC Card bus) and must be driven low when the PC Card bus is reading data from the S1D13A04.
- WAIT# is a signal output from the S1D13A04 that indicates the PC Card bus must wait until data is ready (read cycle) or accepted (write cycle) on the host bus. Since PC Card bus accesses to the S1D13A04 may occur asynchronously to the display update, it is possible that contention may occur in accessing the S1D13A04 internal registers and/or display buffer. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete.
- The Bus Status (BS#) and Read/Write (RD/WR#) signals are not used in this implementation of the PC Card bus using the Generic #2 Host Bus Interface. These pins must be tied high (connected to IO V_{DD}).
- The RESET# (active low) input of the S1D13A04 may be connected to the PC Card RESET (active high) using an inverter.

4 PC Card to S1D13A04 Interface

4.1 Hardware Connections

The S1D13A04 is interfaced to the PC Card bus with a minimal amount of glue logic. In this implementation, the address inputs (AB[17:0]) and data bus (DB[15:0] connect directly to the CPU address (A[17:0]) and data bus (D[15:0]).

The PC Card interface does not provide a bus clock, so one must be supplied for the S1D13A04. Since the bus clock frequency is not critical, nor does it have to be synchronous to the bus signals, it may be the same as CLKI2.

BS# (bus start) and RD/WR# are not used by the Generic #2 Host Bus Interface and should be tied high (connected to IO V_{DD}).

The following diagram shows a typical implementation of the PC Card to S1D13A04 interface.

Figure 4-1: Typical Implementation of PC Card to S1D13A04 Interface

4.2 S1D13A04 Hardware Configuration

The S1D13A04 uses CNF6 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.

The following table shows the configuration required for this implementation of a S1D13A04 to PC Card bus interface.

Table 4-1: Summary of Power-On/Reset Options

S1D13A04 Configuration Input	Power-On/Reset State	
	1 (connected to IO V_{DD})	0 (connected to V_{SS})
CNF4, CNF[2:0]	Select host bus interface as follows: **CNF4** 0 **CNF2** 1 **CNF1** 0 **CNF0** 0 — **Host Bus** Generic #2, Little Endian	
CNF3	Reserved. Must be set to 1.	
CNF5	WAIT# is active high	WAIT# is active low
CNF6	CLKI to BCLK divide ratio 2:1	CLKI to BCLK divide ratio 1:1

configuration for PC Card bus

4.3 Register/Memory Mapping

The S1D13A04 is a memory mapped device. The S1D13A04 uses two 256K byte blocks which are selected using A18 from the PC Card bus (A18 is connected to the S1D13A04 M/R# pin). The internal registers occupy the first 256K byte block and the 160K byte display buffer occupies the second 256K byte block.

The PC Card socket provides 64M bytes of memory address space. However, the S1D13A04 only needs a 512K byte block of memory to accommodate its 160K byte display buffer and register set. For this reason, only address bits A[18:0] are used while A[25:19] are ignored. The S1D13A04's memory and registers are aliased every 512K bytes in the 64M byte PC Card memory address space.

Note
If aliasing is not desirable, the upper addresses must be fully decoded.

5 Software

Test utilities and display drivers are available for the S1D13A04. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13A04CFG (see document number X37A-B-001-xx), or by directly modifying the source. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13A04 test utilities and display drivers are available from your sales support contact (see Section 7, *"Sales and Technical Support"*) or www.erd.epson.com.

6 References

6.1 Documents

- PC Card (PCMCIA) Standard March 1997.
- Epson Research and Development, Inc., *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.
- Epson Research and Development, Inc., *S5U13A04B00C Rev. 1.0 Evaluation Board User Manual,* document number X37A-G-004-xx.
- Epson Research and Development, Inc., *S1D13A04 Programming Notes and Examples*, Document Number X37A-G-003-xx.

6.2 Document Sources

- PC Card Website: www.pc-card.com.
- Epson Research and Development Website: www.erd.epson.com.

7 Sales and Technical Support

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7.2 PC Card Standard

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