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## S1D13A04 LCD/USB Companion Chip

# Connecting to the Sharp HR-TFT Panels

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# 1 Introduction

This application note describes the hardware and software environment required to connect to the Sharp HR-TFT panels directly supported by the S1D13A04. These panels are:

- Sharp LQ031B1DDXX 160 x 160 HR-TFT panel.
- Sharp LQ039Q2DS01 320 x 240 HR-TFT panel.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Research and Development website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

# 2 Connecting to the Sharp LQ039Q2DS01 HR-TFT

## 2.1 External Power Supplies

The S1D13A04 provides all necessary data and control signals to connect to the Sharp LQ039Q2DS01 320 x 240 HR-TFT panel. However, it does not provide any of the voltages required for gray scaling, gate driving, or for the digital and analog supplies. Therefore, external supplies must be designed for any device utilizing the LQ039Q2DS01.

### 2.1.1 Gray Scale Voltages for Gamma Correction

The standard gray scale voltages can be generated using a precise resistor divider network that supplies two sets (A and B) of nine reference voltages to a National Semiconductor 9-Channel Buffer Amplifier (LMC6009). The LMC6009 buffers these nine reference voltages and outputs them to the panel column drivers. The A/B inputs allow the two sets of reference voltages to be alternated, compensating for asymmetrical gamma characteristics during row inversion. This input is controlled by the S1D13A04 output signal REV which toggles every time a horizontal sync signal is sent to the panel.

The REV signal is also used to generate the highest gray scale voltage (V0 or black) by buffering REV and shifting its maximum level to the maximum gray scale voltage (CON_POWER). CON_POWER is supplied by a National Semiconductor micropower Voltage Regulator (LP2951). Figure 2-1: “Sharp LQ039Q2DS01 Gray Scale Voltage (V0-V9) Generation” shows the schematic for gray scale voltage generation.

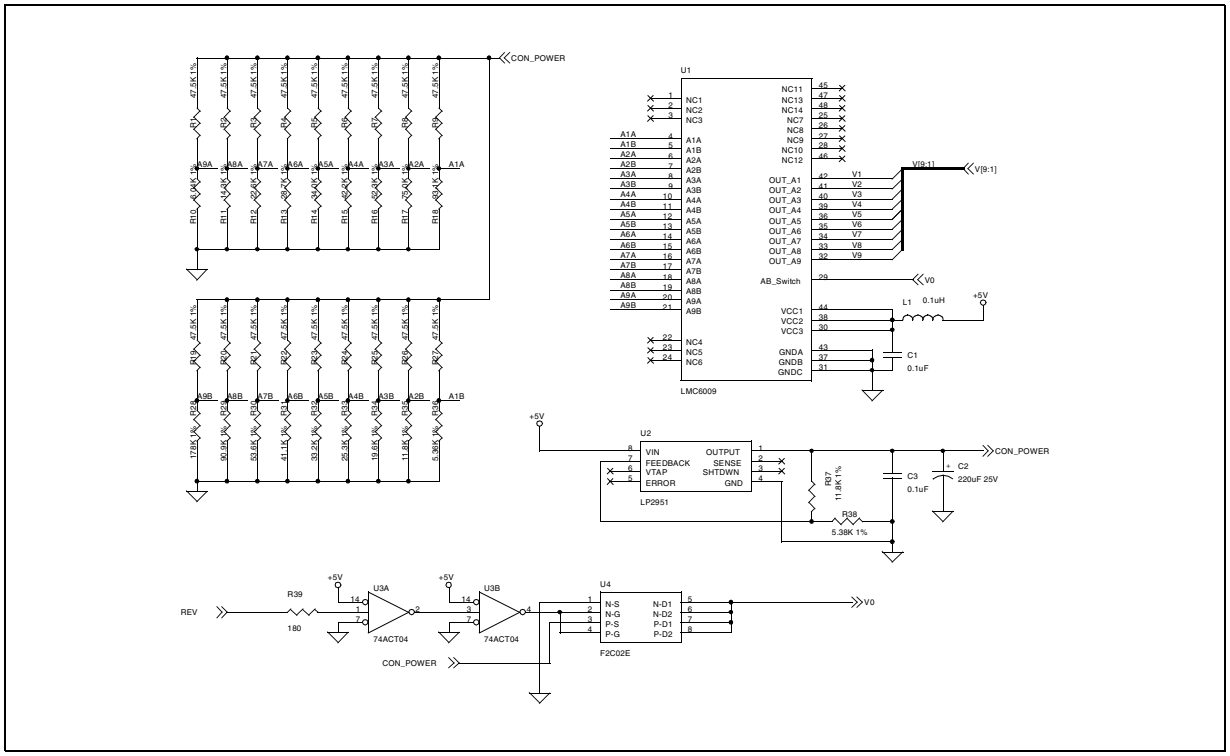



*Figure 2-1: Sharp LQ039Q2DS01 Gray Scale Voltage (V0-V9) Generation*

### 2.1.2 Digital/Analog Power Supplies

The digital power supply (VSHD) must be connected to a 3.3V supply. The analog power supply (VSHA) must be connected to a 5.0V supply.

### 2.1.3 DC Gate Driver Power Supplies

The gate driver high level power supply ($V_{DD}$) and the gate driver logic low power supply ($V_{SS}$) have typical values of +15V and -15V respectively. These power supplies can be provided by a Linear Technology high efficiency switching regulator (LT1172). The two power supplies can be adjusted through their allowable ranges using the potentiometer VR1.

The gate driver logic high power supply ($V_{CC}$) is defined as $V_{SS}$ + VSHD. The typical $V_{CC}$ voltage of -11.7V can be supplied from $V_{SS}$ using a 3.3V zener diode which provides the necessary voltage change.

Figure 2-2: "Panel Gate Driver DC Power Supplies" shows the schematic for $V_{SS}$, $V_{DD}$ and $V_{CC}$.

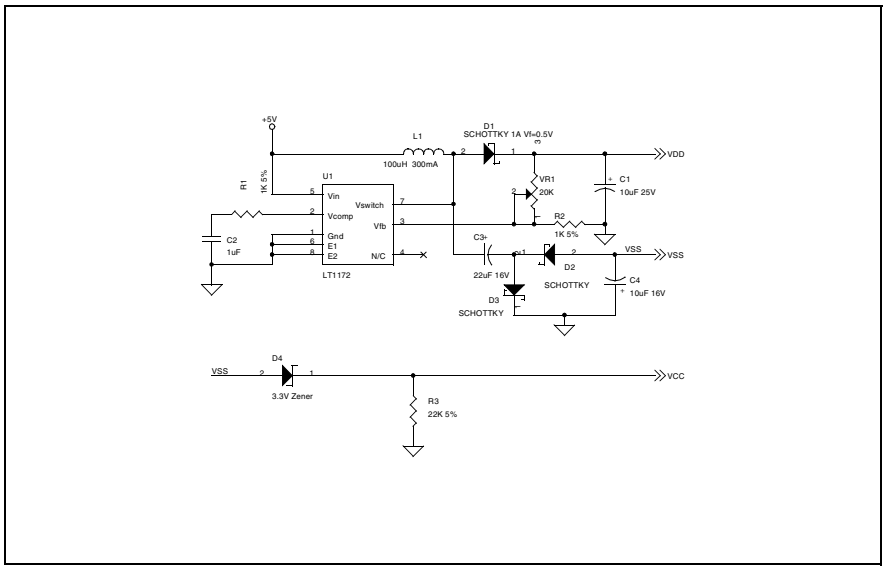



*Figure 2-2: Panel Gate Driver DC Power Supplies*

### 2.1.4 AC Gate Driver Power Supplies

The gate drive low level power supply ($V_{EE}$) is an AC power supply with a DC offset voltage (offset typically -9.0V). The AC component is the common electrode driving signal ($V_{COM}$) which has a voltage of ±2.5V. $V_{COM}$ must be alternated every horizontal period and every vertical period. The S1D13A04 output signal REV accomplishes this function and generates the alternating $V_{COM}$ signal which is superimposed onto $V_{EE}$. Figure 2-3: "Panel Gate Driver AC Power Supplies," on page 8 shows the schematic for generating $V_{COM}$ and $V_{EE}$.

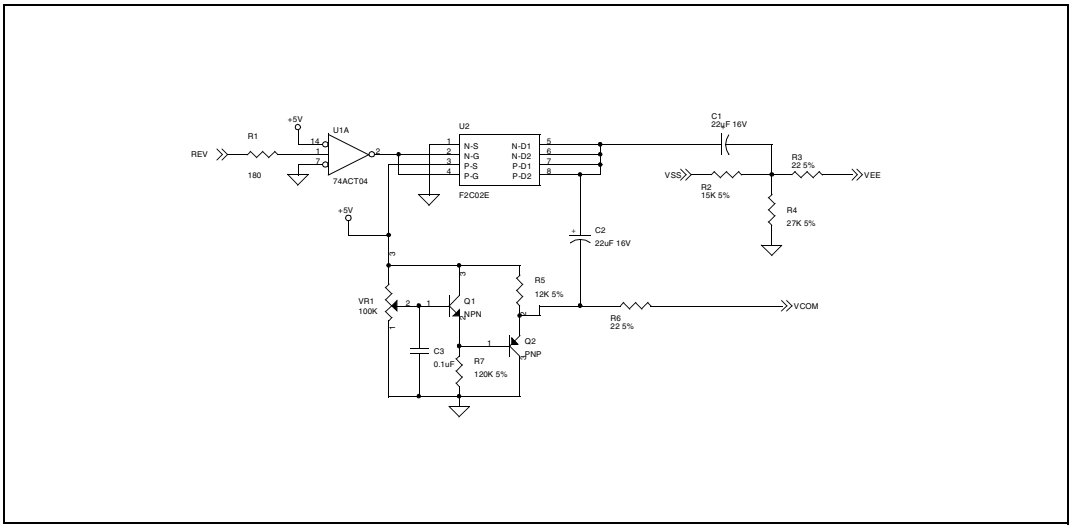
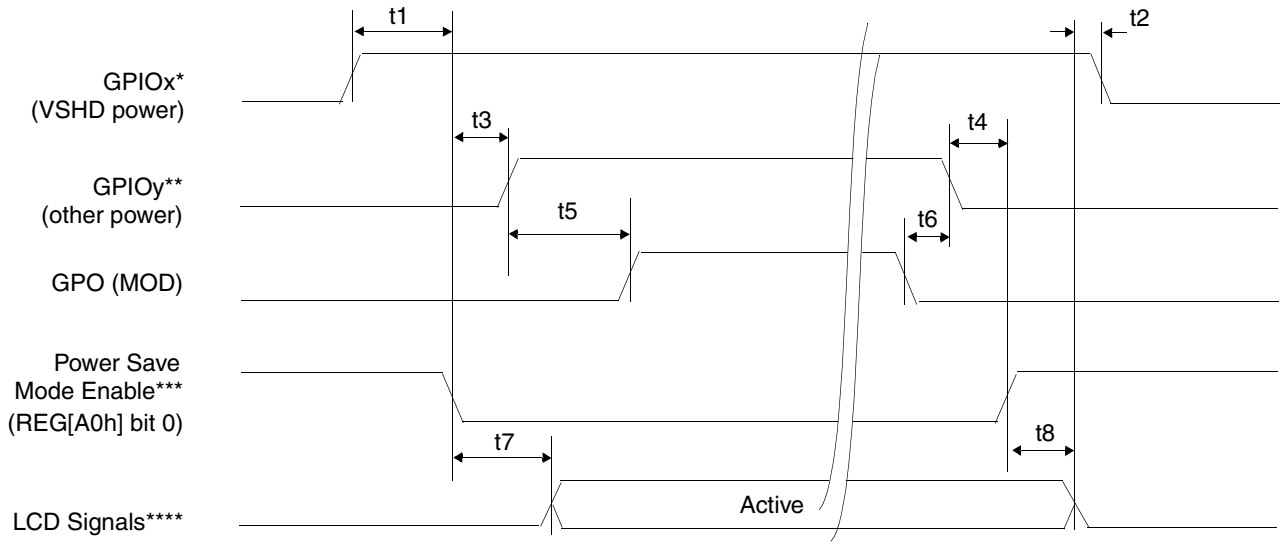



*Figure 2-3: Panel Gate Driver AC Power Supplies*

## 2.2 HR-TFT MOD Signal

The HR-TFT panel uses an input signal (MOD) to control the power-on sequencing of the panel. This HR-TFT signal should not be confused with the S1D13A04 signal DRDY (referred to as MOD for passive panels).

To power-on the HR-TFT panel, MOD must be held low until the power supply has been turned on for more than two FRAMES. To power-off the HR-TFT panel, MOD must be forced low before the power supply is turned off. This sequencing requires two software controlled GPIO pins from the S1D13A04 (see Figure 2-4: “HR-TFT Power-On/Off Sequence Timing” ).




*It is recommended to use one of the general purpose IO pins GPIO[6:4] to control the digital power supply VSHD.
**It is recommended to use one of the general purpose IO pins GPIO[6:4] to control the other power supplies required by the HR-TFT panel.
***The S1D13A04 LCD power-on/off sequence is activated by programming the Power Save Mode Enable bit (REG[A0h] bit 0
****LCD Signals include: FPDAT[17:0], FPSHIFT, FPLINE, FPFRAME, and GPIO[3:0].

*Figure 2-4: HR-TFT Power-On/Off Sequence Timing*

*Table 2-1: HR-TFT Power-On/Off Sequence Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| t1 | LCD Power (VSHD) active to Power Save Mode disabled | 0 | | ns |
| t2 | LCD signals low to LCD Power (VSHD) inactive | 0 | | ns |
| t3 | Power Save Mode disabled to LCD Power (other) active | 0 | | ns |
| t4 | LCD Power (other) inactive to Power Save Mode enabled | 0 | | ns |
| t5 | LCD Power (other) active to MOD active | 2 | | FRAME |
| t6 | MOD inactive to LCD Power (other) inactive | 0 | | ns |
| t7 | Power Save Mode disabled to LCD signals active | | 20 | ns |
| t8 | Power Save Mode enabled to LCD signals low | | 20 | ns |

## 2.3 S1D13A04 to LQ039Q2DS01 Pin Mapping

*Table 2-2: S1D13A04 to LQ039Q2DS01 Pin Mapping*

| LCD Pin No. | LCD Pin Name | S1D13A04 Pin Name | Description | Remarks |
|---|---|---|---|---|
| 1 | VDD | - | Power supply of gate driver (high level) | See Section 2.1, “External Power Supplies” on page 6 |
| 2 | VCC | - | Power supply of gate driver (logic high) | See Section 2.1, “External Power Supplies” on page 6 |
| 3 | MOD | - | Control signal of gate driver | See Section 2.2, “HR-TFT MOD Signal” on page 9 |
| 4 | MOD | - | Control signal of gate driver | See Section 2.2, “HR-TFT MOD Signal” on page 9 |
| 5 | U/L | - | Selection for vertical scanning direction | Connect to VSHD (top / bottom scanning) |
| 6 | SPS | FPFRAME | Start signal of gate driver | |
| 7 | CLS | GPIO1 | Clock signal of gate driver | |
| 8 | VSS | - | Power supply of gate driver (logic low) | See Section 2.1, “External Power Supplies” on page 6 |
| 9 | VEE | - | Power supply of gate driver (low level) | See Section 2.1, “External Power Supplies” on page 6 |
| 10 | VEE | - | Power supply of gate driver (low level) | See Section 2.1, “External Power Supplies” on page 6 |
| 11 | VCOM | - | Common electrode driving signal | See Section 2.1, “External Power Supplies” on page 6 |
| 12 | VCOM | - | Common electrode driving signal | See Section 2.1, “External Power Supplies” on page 6 |
| 13 | SPL | GPIO3 | Sampling start signal for left / right scanning | |
| 14 | R0 | FPDAT11 | Red data signal (LSB) | |
| 15 | R1 | FPDAT10 | Red data signal | |
| 16 | R2 | FPDAT9 | Red data signal | |
| 17 | R3 | FPDAT2 | Red data signal | |
| 18 | R4 | FPDAT1 | Red data signal | |
| 19 | R5 | FPDAT0 | Red data signal (MSB) | |
| 20 | G0 | FPDAT14 | Green data signal (LSB) | |
| 21 | G1 | FPDAT13 | Green data signal | |
| 22 | G2 | FPDAT12 | Green data signal | |
| 23 | G3 | FPDAT5 | Green data signal | |
| 24 | G4 | FPDAT4 | Green data signal | |
| 25 | G5 | FPDAT3 | Green data signal (MSB) | |

*Table 2-2: S1D13A04 to LQ039Q2DS01 Pin Mapping (Continued)*

| LCD Pin No. | LCD Pin Name | S1D13A04 Pin Name | Description | Remarks |
|---|---|---|---|---|
| 26 | B0 | FPDAT17 | Blue data signal (LSB) | |
| 27 | B1 | FPDAT16 | Blue data signal | |
| 28 | B2 | FPDAT15 | Blue data signal | |
| 29 | B3 | FPDAT8 | Blue data signal | |
| 30 | B4 | FPDAT7 | Blue data signal | |
| 31 | B5 | FPDAT6 | Blue data signal (MSB) | |
| 32 | VSHD | - | Digital power supply | See Section 2.1, “External Power Supplies” on page 6 |
| 33 | DGND | $V_{SS}$ | Digital ground | Ground pin of S1D13A04 |
| 34 | PS | GPIO0 | Power save signal | |
| 35 | LP | FPLINE | Data latch signal of source driver | |
| 36 | DCLK | FPSHIFT | Data sampling clock signal | |
| 37 | LBR | - | Selection for horizontal scanning direction | Connect to VSHD (left / right scanning) |
| 38 | SPR | - | Sampling start signal for right / left scanning | Right to left scanning not supported |
| 39 | VSHA | - | Analog power supply | See Section 2.1, “External Power Supplies” on page 6 |
| 40 | V0 | - | Standard gray scale voltage (black) | See Section 2.1, “External Power Supplies” on page 6 |
| 41 | V1 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 42 | V2 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 43 | V3 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 44 | V4 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 45 | V5 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 46 | V6 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 47 | V7 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 48 | V8 | - | Standard gray scale voltage | See Section 2.1, “External Power Supplies” on page 6 |
| 49 | V9 | - | Standard gray scale voltage (white) | See Section 2.1, “External Power Supplies” on page 6 |
| 50 | AGND | $V_{SS}$ | Analog ground | Ground pin of S1D13A04 |

# 3 Connecting to the Sharp LQ031B1DDxx HR-TFT

## 3.1 External Power Supplies

The S1D13A04 provides all necessary data and control signals to connect to the Sharp LQ031B1DDxx 160x160 HR-TFT panel(s). However, it does not provide any of the voltages required for the backlight, gray scaling, gate driving, or for the digital and analog supplies. Therefore, external supplies must be designed for any device utilizing the LQ031B1DDxx.

The LQ031B1DDxx (160x160) has the same voltage requirements as the LQ039Q2DS01 (320x240). All the circuits used to generate the various voltages for the LQ039Q2DS01 panel also apply to the LQ031B1DDxx panel. This section provides additional circuits for generating some of these voltages.

### 3.1.1 Gray Scale Voltages for Gamma Correction

The standard gray scale voltages can be generated using a precise resistor divider network as described in Section 2.1.1, “Gray Scale Voltages for Gamma Correction” on page 6. Alternately, they can be generated using a Sharp gray scale IC. The Sharp IR3E203 eliminates the large resistor network used to provide the 10 gray scale voltages and combines their function into a single IC.

The S1D13A04 output signal REV is used to alternate the gray scale voltages and connects to the SW input of the IR3E203 IC. The COM signal is used in generating the gate driver panel AC voltage, $V_{COM}$ and is explained in Section 3.1.4, “AC Gate Driver Power Supplies” on page 13. Figure 3-1: “Sharp LQ031B1DDxx Gray Scale Voltage (V0-V9) Generation” shows the circuit that generates the gray scale voltages using the Sharp IR3E203 IC.

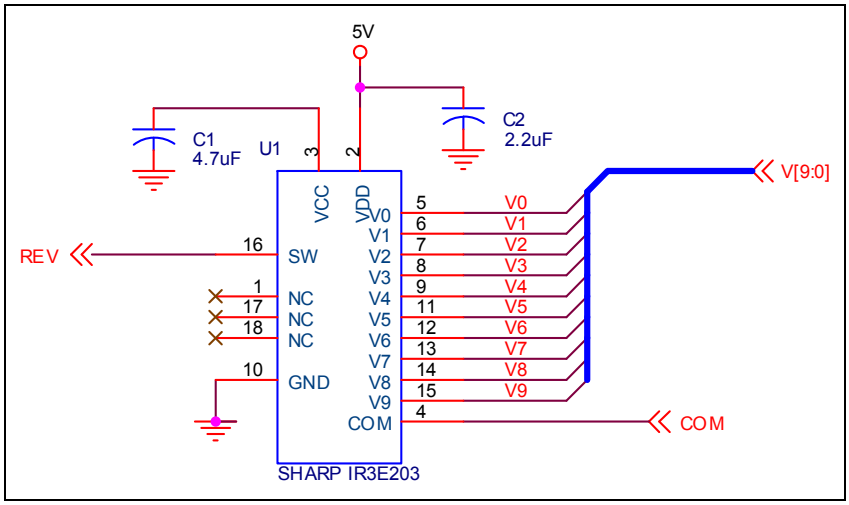



*Figure 3-1: Sharp LQ031B1DDxx Gray Scale Voltage (V0-V9) Generation*

### 3.1.2 Digital/Analog Power Supplies

The digital power supply (VSHD) must be connected to a 3.3V supply. The analog power supply (VSHA) must be connected to a 5.0V supply.

### 3.1.3 DC Gate Driver Power Supplies

See Section 2.1.3, "DC Gate Driver Power Supplies" on page 7 and Figure 2-2: "Panel Gate Driver DC Power Supplies," on page 7 for details on generating $V_{SS}$, $V_{DD}$, and $V_{CC}$.

### 3.1.4 AC Gate Driver Power Supplies

See Section 2.1.4, "AC Gate Driver Power Supplies" on page 8 and Figure 2-3: "Panel Gate Driver AC Power Supplies," on page 8 for details on generating $V_{EE}$ and $V_{COM}$. If the Sharp IR3E203 is used to generate the gray scale voltages, the COM signal can be connected to the input of the F2C02E MOSFET instead of the buffered REV signal.

## 3.2 HR-TFT MOD Signal

See Section 2.2, "HR-TFT MOD Signal" on page 9 for details on controlling the MOD signal through software.

## 3.3 S1D13A04 to LQ031B1DDxx Pin Mapping

*Table 3-1: S1D13A04 to LQ031B1DDxx Pin Mapping*

| LCD Pin No. | LCD Pin Name | S1D13A04 Pin Name | Description | Remarks |
|---|---|---|---|---|
| 1 | VDD | - | Power supply of gate driver (high level) | See Section 3.1, “External Power Supplies” on page 12 |
| 2 | VCC | - | Power supply of gate driver (logic high) | See Section 3.1, “External Power Supplies” on page 12 |
| 3 | MOD | - | Control signal of gate driver | See Section 3.2, “HR-TFT MOD Signal” on page 13 |
| 4 | MOD | - | Control signal of gate driver | See Section 3.2, “HR-TFT MOD Signal” on page 13 |
| 5 | U/L | - | Selection for vertical scanning direction | Connect to VSHD (top / bottom scanning) |
| 6 | SPS | FPFRAME | Start signal of gate driver | |
| 7 | CLS | GPIO1 | Clock signal of gate driver | |
| 8 | VSS | - | Power supply of gate driver (logic low) | See Section 3.1, “External Power Supplies” on page 12 |
| 9 | VEE | - | Power supply of gate driver (low level) | See Section 3.1, “External Power Supplies” on page 12 |
| 10 | VEE | - | Power supply of gate driver (low level) | See Section 3.1, “External Power Supplies” on page 12 |
| 11 | VCOM | - | Common electrode driving signal | See Section 3.1, “External Power Supplies” on page 12 |
| 12 | VCOM | - | Common electrode driving signal | See Section 3.1, “External Power Supplies” on page 12 |
| 13 | SPL | GPIO3 | Sampling start signal for left / right scanning | |
| 14 | R0 | FPDAT11 | Red data signal (LSB) | |
| 15 | R1 | FPDAT10 | Red data signal | |
| 16 | R2 | FPDAT9 | Red data signal | |
| 17 | R3 | FPDAT2 | Red data signal | |
| 18 | R4 | FPDAT1 | Red data signal | |
| 19 | R5 | FPDAT0 | Red data signal (MSB) | |
| 20 | G0 | FPDAT14 | Green data signal (LSB) | |
| 21 | G1 | FPDAT13 | Green data signal | |
| 22 | G2 | FPDAT12 | Green data signal | |
| 23 | G3 | FPDAT5 | Green data signal | |
| 24 | G4 | FPDAT4 | Green data signal | |
| 25 | G5 | FPDAT3 | Green data signal (MSB) | |

*Table 3-1: S1D13A04 to LQ031B1DDxx Pin Mapping (Continued)*

| LCD Pin No. | LCD Pin Name | S1D13A04 Pin Name | Description | Remarks |
|---|---|---|---|---|
| 26 | B0 | FPDAT17 | Blue data signal (LSB) | |
| 27 | B1 | FPDAT16 | Blue data signal | |
| 28 | B2 | FPDAT15 | Blue data signal | |
| 29 | B3 | FPDAT8 | Blue data signal | |
| 30 | B4 | FPDAT7 | Blue data signal | |
| 31 | B5 | FPDAT6 | Blue data signal (MSB) | |
| 32 | VSHD | - | Digital power supply | See Section 3.1, “External Power Supplies” on page 12 |
| 33 | DGND | $V_{SS}$ | Digital ground | Ground pin of S1D13A04 |
| 34 | PS | GPIO0 | Power save signal | |
| 35 | LP | FPLINE | Data latch signal of source driver | |
| 36 | DCLK | FPSHIFT | Data sampling clock signal | |
| 37 | LBR | - | Selection for horizontal scanning direction | Connect to VSHD (left / right scanning) |
| 38 | SPR | - | Sampling start signal for right / left scanning | Right to left scanning not supported |
| 39 | VSHA | - | Analog power supply | See Section 3.1, “External Power Supplies” on page 12 |
| 40 | V0 | - | Standard gray scale voltage (black) | See Section 3.1, “External Power Supplies” on page 12 |
| 41 | V1 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 42 | V2 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 43 | V3 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 44 | V4 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 45 | V5 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 46 | V6 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 47 | V7 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 48 | V8 | - | Standard gray scale voltage | See Section 3.1, “External Power Supplies” on page 12 |
| 49 | V9 | - | Standard gray scale voltage (white) | See Section 3.1, “External Power Supplies” on page 12 |
| 50 | AGND | $V_{SS}$ | Analog ground | Ground pin of S1D13A04 |

# 4 Test Software

Test utilities and display drivers are available for the S1D13A04. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13A04CFG (see document number X37A-B-001-xx), or by directly modifying the source. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13A04 test utilities and display drivers are available from your sales support contact (see Section 6, *"Sales &Technical Support"*) or at www.erd.epson.com.

# 5 References

## 5.1 Documents

- Sharp Electronics Corporation, *LQ039Q2DS01 Specification*.
- Sharp Electronics Corporation, *LQ031B1DDxx Specification*.
- Epson Research and Development, Inc., *S1D13A04 Hardware Functional Specification*, Document Number X37A-A-001-xx.
- Epson Research and Development, Inc., *S1D13A04 Programming Notes and Examples*, Document Number X37A-G-003-xx.
- Epson Research and Development, Inc., *S5U13A04B00C Rev. 1.0 ISA Bus Evaluation Board User Manual*, Document Number X37A-G-004-xx.

## 5.2 Document Sources

- Sharp Electronics Corporation Website: www.sharpmeg.com.
- Epson Research and Development Website: www.erd.epson.com.

# 6 Sales &Technical Support

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## 6.2 Sharp HR-TFT Panel

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