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S1D13A04 LCD/USB Companion Chip

Interfacing to the Freescale MCF5307 "ColdFire" Microprocessor

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1 Introduction

This application note describes the hardware and software environment required to interface the S1D13A04 LCD/USB Companion Chip and the Freescale MCF5307 “Coldfire” Processor.

The designs described in this document are presented only as examples of how such interfaces might be implemented. This application note is updated as appropriate. Please check the Epson Research and Development website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Interfacing to the MCF5307

2.1 The MCF5307 System Bus

The MCF5200/5300 family of processors feature a high-speed synchronous system bus typical of modern microprocessors. This section is an overview of the operation of the CPU bus in order to establish interface requirements.

2.1.1 Overview

The MCF5307 microprocessor family uses a synchronous address and data bus, very similar in architecture to the MC68040 and MPC8xx. All outputs and inputs are timed with respect to a square-wave reference clock called BCLK0 (Master Clock). This clock runs at a software-selectable divisor rate from the machine cycle speed of the CPU core (typically 20 to 33 MHz). Both the address and the data bus are 32 bits in width. All IO accesses are memory-mapped; there is no separate IO space in the Coldfire architecture.

The bus can support two types of cycles, normal and burst. Burst memory cycles are used to fill on-chip cache memories, and for certain on-chip DMA operations. Normal cycles are used for all other data transfers.

2.1.2 Normal (Non-Burst) Bus Transactions

A data transfer is initiated by the bus master by placing the memory address on address lines A31 through A0 and driving $\overline{TS}$ (Transfer Start) low for one clock cycle. Several control signals are also provided with the memory address:

- SIZ[1:0] (Transfer Size) — indicates whether the bus cycle is 8, 16, or 32-bit.
- R/$\overline{W}$ — set high for read cycles and low for write cycles.
- TT[1:0] (Transfer Type Signals) — provides more detail on the type of transfer being attempted.
- $\overline{TIP}$ (Transfer In Progress) — asserts whenever a bus cycle is active.

When the peripheral device being accessed has completed the bus transfer, it asserts $\overline{TA}$ (Transfer Acknowledge) for one clock cycle to complete the bus transaction. Once $\overline{TA}$ has been asserted, the MCF5307 will not start another bus cycle until $\overline{TA}$ has been de-asserted. The minimum length of a bus transaction is two bus clocks.

Figure 2-1: “MCF5307 Memory Read Cycle,” illustrates a typical memory read cycle on the MCF5307 system bus.

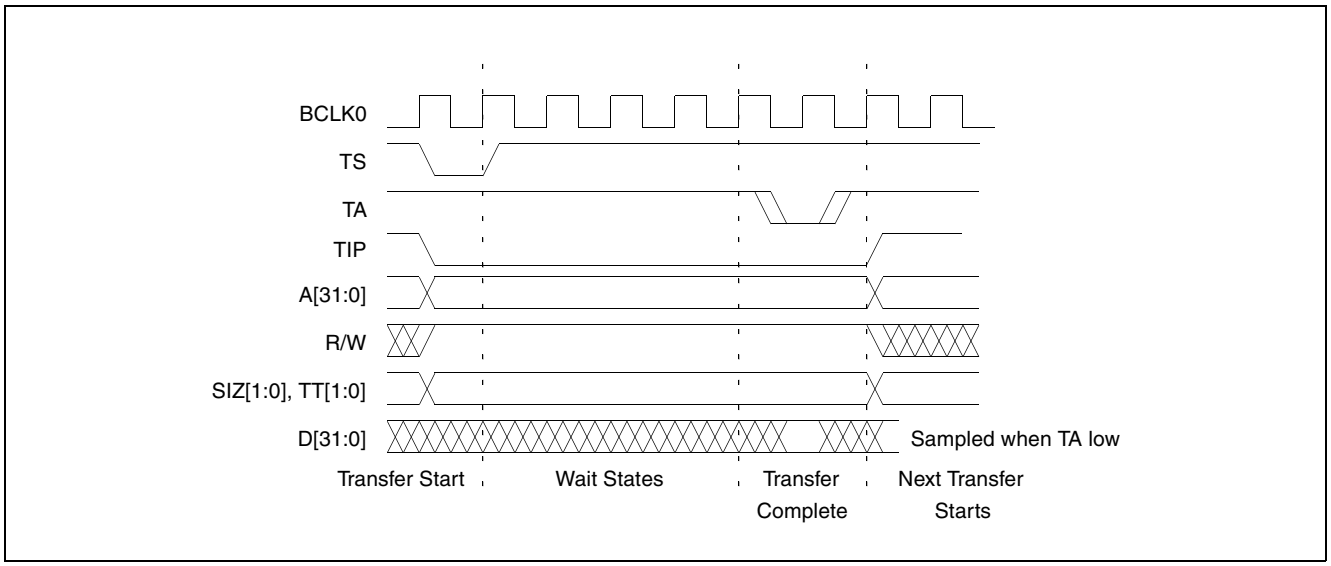


Figure 2-1: MCF5307 Memory Read Cycle

Figure 2-2: “MCF5307 Memory Write Cycle,” illustrates a typical memory write cycle on the MCF5307 system bus.

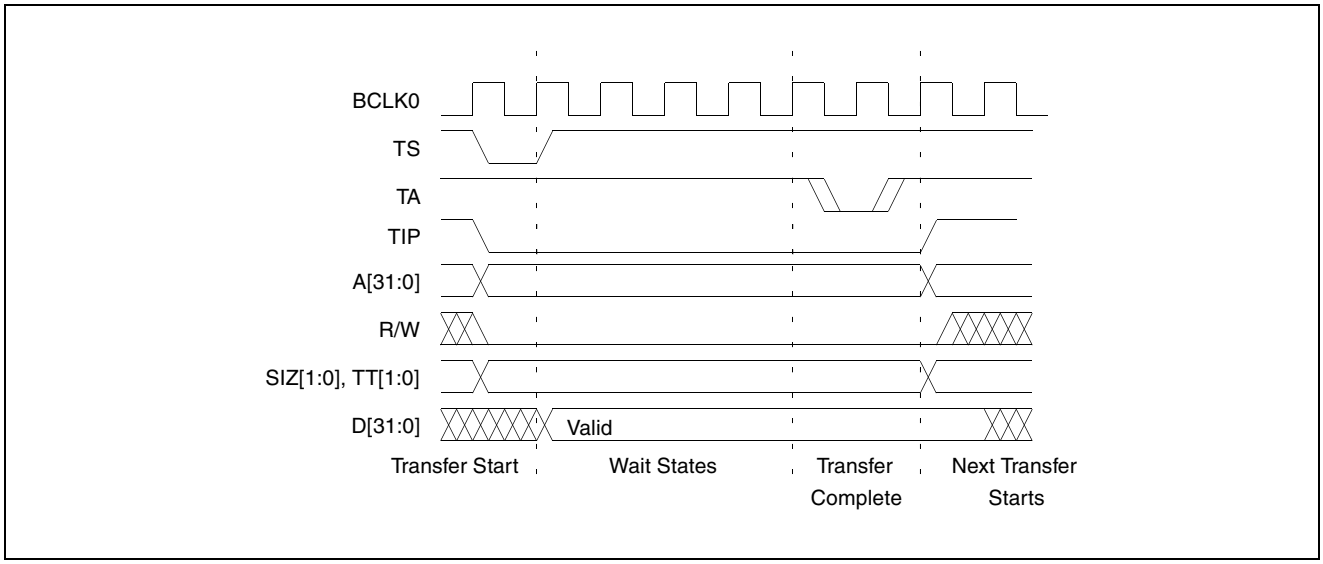


Figure 2-2: MCF5307 Memory Write Cycle

2.1.3 Burst Cycles

Burst cycles are very similar to normal cycles, except that they occur as a series of four back-to-back, 32-bit memory reads or writes. The $\overline{\text{TIP}}$ (Transfer In Progress) output is asserted continuously through the burst. Burst memory cycles are mainly intended to fill

caches from program or data memory. They are typically not used for transfers to or from IO peripheral devices such as the S1D13A04. The MCF5307 chip selects provide a mechanism to disable burst accesses for peripheral devices which are not burst capable.

2.2 Chip-Select Module

In addition to generating eight independent chip-select outputs, the MCF5307 Chip Select Module can generate active-low Output Enable ($\overline{OE}$) and Write Enable ($\overline{BWE}$) signals compatible with most memory and x86-style peripherals. The MCF5307 bus controller also provides a Read/Write (R/$\overline{W}$) signal which is compatible with most 68K peripherals.

Chip selects 0 and 1 can be programmed independently to respond to any base address and block size. Chip select 0 can be active immediately after reset, and is typically used to control a boot ROM. Chip select 1 is likewise typically used to control a large static or dynamic RAM block.

Chip selects 2 through 7 have fixed block sizes of 2M bytes each. Each has a unique, fixed offset from a common, programmable starting address. These chip selects are well-suited to typical IO addressing requirements.

Each chip select may be individually programmed for:

- port size (8/16/32-bit).
- up to 15 wait states or external acknowledge.
- address space type.
- burst or non-burst cycle support.
- write protect.

Figure 2-3: “Chip Select Module Outputs Timing” illustrates a typical cycle for a memory mapped device using the GPCM of the Power PC.

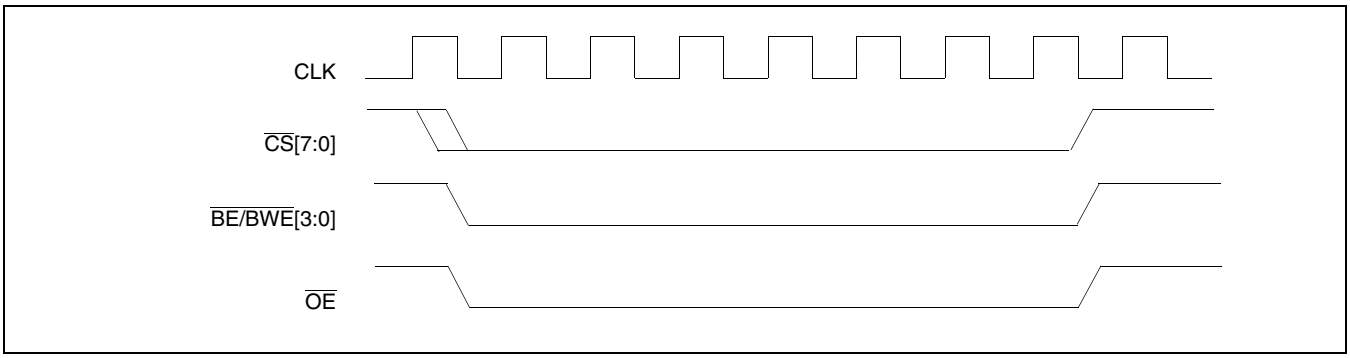


Figure 2-3: Chip Select Module Outputs Timing

3 S1D13A04 Host Bus Interface

The S1D13A04 directly supports multiple processors. The S1D13A04 implements a 16-bit Generic #1 Host Bus Interface which is most suitable for direct connection to the Freescale MFC5307 microprocessor. Generic #1 supports a Chip Select and an individual Read Enable/Write Enable for each byte.

The Generic #1 Host Bus Interface is selected by the S1D13A04 on the rising edge of RESET#. After RESET# is released, the bus interface signals assume their selected configuration. For details on the S1D13A04 configuration, see Section 4.2, “S1D13A04 Hardware Configuration” on page 12.

3.1 Host Bus Interface Pin Mapping

The following table shows the functions of each Host Bus Interface signal.

Table 3-1: Host Bus Interface Pin Mapping

S1D13A04 Pin Names	Freescale MCF5307
AB[17:0]	A[17:0]
DB[15:0]	D[31:16]
WE1#	$\overline{BWE1}$
CS#	$\overline{CS4}$
M/R#	A18
CLKI	BCLK0
BS#	Connect to IO_{VDD} from the S1D13A04
RD/WR#	$\overline{OE}$
RD#	$\overline{OE}$
WE0#	$\overline{BWE0}$
WAIT#	$\overline{TA}$
RESET#	system $\overline{RESET}$

3.2 Host Bus Interface Signals

The Host Bus Interface requires the following signals.

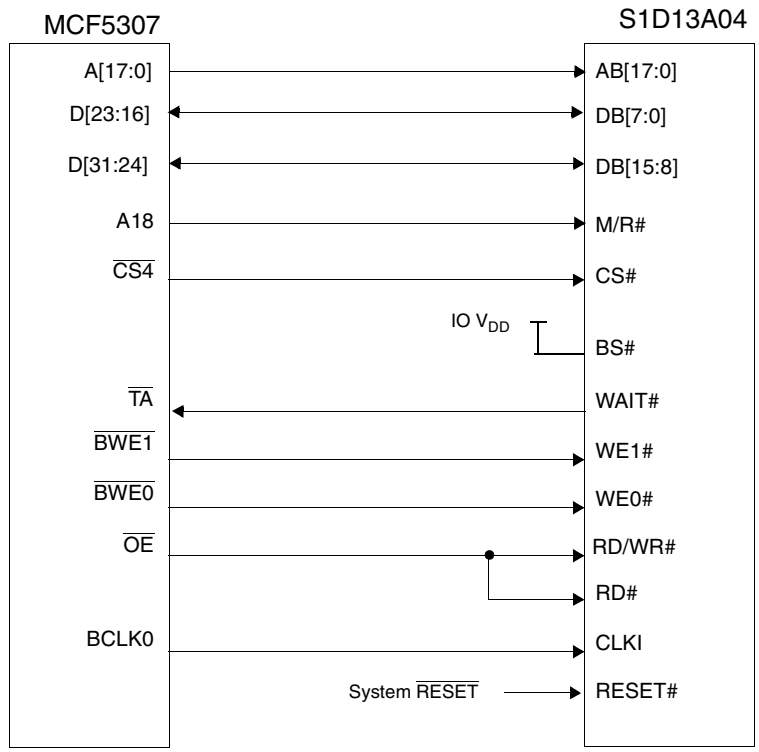
- CLKI is a clock input which is required by the S1D13A04 Host Bus Interface as a source for its internal bus and memory clocks. This clock is typically driven by the host CPU system clock. For this example, BCLK0 from the Freescale MCF5307 is used for CLKI.
- The address inputs AB[17:0] connect directly to the MCF5307 address bus (A[17:0]).
- DB[7:0] connects D[23:16] (the MCF5307 low order byte). DB[15:8] connects to D[31:24] (the MCF5307 high order byte). CNF4 must be set to select big endian mode.
- Chip Select (CS#) must be driven low by $\overline{CS4}$ whenever the S1D13A04 is accessed by the Freescale MCF5307.
- M/R# (memory/register) selects between memory or register accesses. This signal is generated by the external address decode circuitry. For this example, M/R# is connected to address line A18, allowing system address A18 to select between memory or register accesses.
- WE0# connects to $\overline{BWE0}$ (the low byte enable signal from the MCF5307) and must be driven low when the MCF5307 is writing the low byte to the S1D13A04.
- WE1# connects to $\overline{BWE1}$ (the high byte enable signal from the MCF5307) and must be driven low when the MCF5307 is writing the high byte to the S1D13A04.
- RD# and RD/WR# are read enables for the low-order and high-order bytes, respectively. Both signals are driven low by $\overline{OE}$ when the Freescale MCF5307 is reading data from the S1D13A04.
- WAIT# connects to $\overline{TA}$ and is a signal which is output from the S1D13A04 that indicates the host CPU must wait until data is ready (read cycle) or accepted (write cycle) on the host bus. Since host CPU accesses to the S1D13A04 may occur asynchronously to the display update, it is possible that contention may occur in accessing the S1D13A04 internal registers and/or refresh memory. The WAIT# line resolves these contentions by forcing the host to wait until the resource arbitration is complete. This signal is active low and may need to be inverted if the host CPU wait state signal is active high.
- The Bus Status (BS#) signal is not used in the bus interface for Generic #1 mode and must be tied high to IO V_{DD}.

4 MCF5307 To S1D13A04 Interface

4.1 Hardware Description

The interface between the S1D13A04 and the MCF5307 requires no external glue logic. The polarity of the WAIT# signal must be selected as active high by connecting CNF5 to IO V_{DD} (see Table 4-1:, "Summary of Power-On/Reset Options," on page 12).

The following diagram shows a typical implementation of the MCF5307 to S1D13A04 interface.



Note:
When connecting the S1D13A04 RESET# pin, the system designer should be aware of all conditions that may reset the S1D13A04 (e.g. CPU reset can be asserted during wake-up from power-down modes, or during debug states).

Figure 4-1: Typical Implementation of MCF5307 to S1D13A04 Interface

4.2 S1D13A04 Hardware Configuration

The S1D13A04 uses CNF6 through CNF0 to allow selection of the bus mode and other configuration data on the rising edge of RESET#. For details on configuration, refer to the *S1D13A04 Hardware Functional Specification*, document number X37A-A-001-xx.

The following table shows the configuration required for this implementation of a S1D13A04 to Freescale MFC5307 microprocessor.

Table 4-1: Summary of Power-On/Reset Options

S1D13A04 Configuration Input	**Power-On/Reset State**	
	1 (connected to IO V_{DD})	**0 (connected to V_{SS})**
CNF4, CNF[2:0]	Select host bus interface as follows: **CNF4** 1, **CNF2** 0, **CNF1** 1, **CNF0** 1 — **Host Bus**: Generic #1, Big Endian	
CNF3	Reserved. Must be set to 1.	
CNF5	WAIT# is active high	WAIT# is active low
CNF6	CLKI to BCLK divide ratio 2:1	CLKI to BCLK divide ratio 1:1

	configuration for Freescale MFC5307 microprocessor

4.3 Register/Memory Mapping

The S1D13A04 uses two 256K byte blocks which are selected using A18 from the MCF5307 (A18 is connected to the S1D13A04 M/R# pin). The internal registers occupy the first 256K bytes block and the 160K byte display buffer occupies the second 256K byte block. These two blocks of memory are aliased over the entire 2M byte space.

Note
If aliasing is not desirable, the upper addresses must be fully decoded.

4.4 MCF5307 Chip Select Configuration

Chip Selects 0 and 1 have programmable block sizes from 64K bytes through 2G bytes. However, these chip selects would normally be needed to control system RAM and ROM. Therefore, one of the IO chip selects CS2 through CS7 is required to address the entire address space of the S1D13A04. These IO chip selects have a fixed, 2M byte block size. In the example interface, chip select 4 is used to control the S1D13A04. The CSBAR register should be set to the upper 8 bits of the desired base address.

The following options should be selected in the chip select mask registers (CSMR4/5).

- WP = 0 – disable write protect
- AM = 0 - enable alternate bus master access to the S1D13A04
- C/I = 1 - disable CPU space access to the S1D13A04
- SC = 1 - disable Supervisor Code space access to the S1D13A04
- SD = 0 - enable Supervisor Data space access to the S1D13A04
- UC = 1 - disable User Code space access to the S1D13A04
- UD = 0 - enable User Data space access to the S1D13A04
- V = 1 - global enable (“Valid”) for the chip select

The following options should be selected in the chip select control registers (CSCR4/5).

- WS0-3 = 0 - no internal wait state setting
- AA = 0 - no automatic acknowledgment
- PS (1:0) = 1:0 – memory port size is 16 bits
- BEM = 0 – Byte enable/write enable active on writes only
- BSTR = 0 – disable burst reads
- BSTW = 0 – disable burst writes

5 Software

Test utilities and display drivers are available for the S1D13A04. Full source code is available for both the test utilities and the drivers.

The test utilities are configurable for different panel types using a program called 13A04CFG (see document number X37A-B-001-xx), or by directly modifying the source. The display drivers can be customized by the OEM for different panel types, resolutions and color depths only by modifying the source.

The S1D13A04 test utilities and display drivers are available from your sales support contact (see Section 7, *"Sales and Technical Support"*) or www.erd.epson.com.

6 References

6.1 Documents

- Freescale Semiconductor, *MCF5307 ColdFire® Integrated Microprocessor User's Manual*, Freescale Publication no. MCF5307UM; available on the Internet at http://www.freescale.com.
- Epson Research and Development, Inc., *S1D13A04 Hardware Functional Specification,* document number X37A-A-001-xx.
- Epson Research and Development, Inc., *S5U13A04B00C Rev. 1.0 Evaluation Board User Manual,* document number X37A-G-004-xx.
- Epson Research and Development, Inc., *S1D13A04 Programming Notes and Examples*, document number X37A-G-003-xx.

6.2 Document Sources

- Freescale Semiconductor Website: www.freescale.com.
- Epson Research and Development Website: www.erd.epson.com.

7 Sales and Technical Support

7.1 EPSON LCD/USB Companion Chips (S1D13A04)

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway
San Jose, CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

7.2 Freescale MCF5307 Processor

- Freescale Semiconductor Website: www.freescale.com.
- Freescale Semiconductor sales office or authorized distributor.