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## S1D13A05 LCD/USB Companion Chip

# 13A05CFG Configuration Program

**Document Number: X40A-B-001-01**

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# Table of Contents

**13A05CFG . . . . . 5**
S1D13A05 Supported Evaluation Platforms . . . . . 5
Installation . . . . . 6
Usage . . . . . 6
13A05CFG Configuration Tabs . . . . . 7
General Tab . . . . . 7
Preferences Tab . . . . . 9
Clocks Tab . . . . . 11
Panel Tab . . . . . 15
Panel Power Tab . . . . . 23
Registers Tab . . . . . 25
Direct Tab . . . . . 26
13A05CFG Menus . . . . . 28
Open... . . . . 28
Save . . . . . 29
Save As... . . . . 29
Configure Multiple . . . . . 30
Export . . . . . 31
Enable Tooltips . . . . . 32
Tooltip Delay . . . . . 32
ERD on the Web . . . . . 32
Update Common Controls . . . . . 32
About 13A05CFG . . . . . 32
Comments . . . . . 33

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# 13A05CFG

13A05CFG is an interactive Windows® program that calculates register values for a user-defined S1D13A05 configuration. The configuration information can be used to directly alter the operating characteristics of the S1D13A05 utilities or any program built with the Hardware Abstraction Layer (HAL) library. Alternatively, the configuration information can be saved in a variety of text file formats for use in other applications.

**Note**

This program is a Windows desktop application suitable for configuring software for a given implementation of an Epson LCD controller. However, it is not a display driver for any Windows desktop operating system. Epson does not provide display drivers for any of the Windows desktop operating systems.

## S1D13A05 Supported Evaluation Platforms

13A05CFG runs on PC system running Windows 9x/ME/XP/NT/2000 and can modify Win32 .exe files and .s9 format files.

## Installation

Create a directory for **13a05cfg.exe** and copy the files **13a05cfg.exe** and **panels.def** to that directory. **Panels.def** contains configuration information for a number of panels and must reside in the same directory as **13a05cfg.exe**.

## Usage

To start 13A05CFG from the Windows desktop, double-click on the My Computer icon and run the program **13a05cfg.exe** from the installed directory.

To start 13A05CFG from a Windows command prompt, change to the directory **13a05cfg.exe** was installed to and type the command **13A05cfg**.

The basic procedure for using 13A05CFG is:

1. Start 13A05CFG as described above.
2. Open an existing file to serve as a starting reference point (this step is optional).
3. Modify the configuration. For specific information on editing the configuration, see "13A05CFG Configuration Tabs" on page 7.
4. Save the new configuration. The configuration information can be saved in two ways; as an ASCII text file or by modifying an executable image on disk.

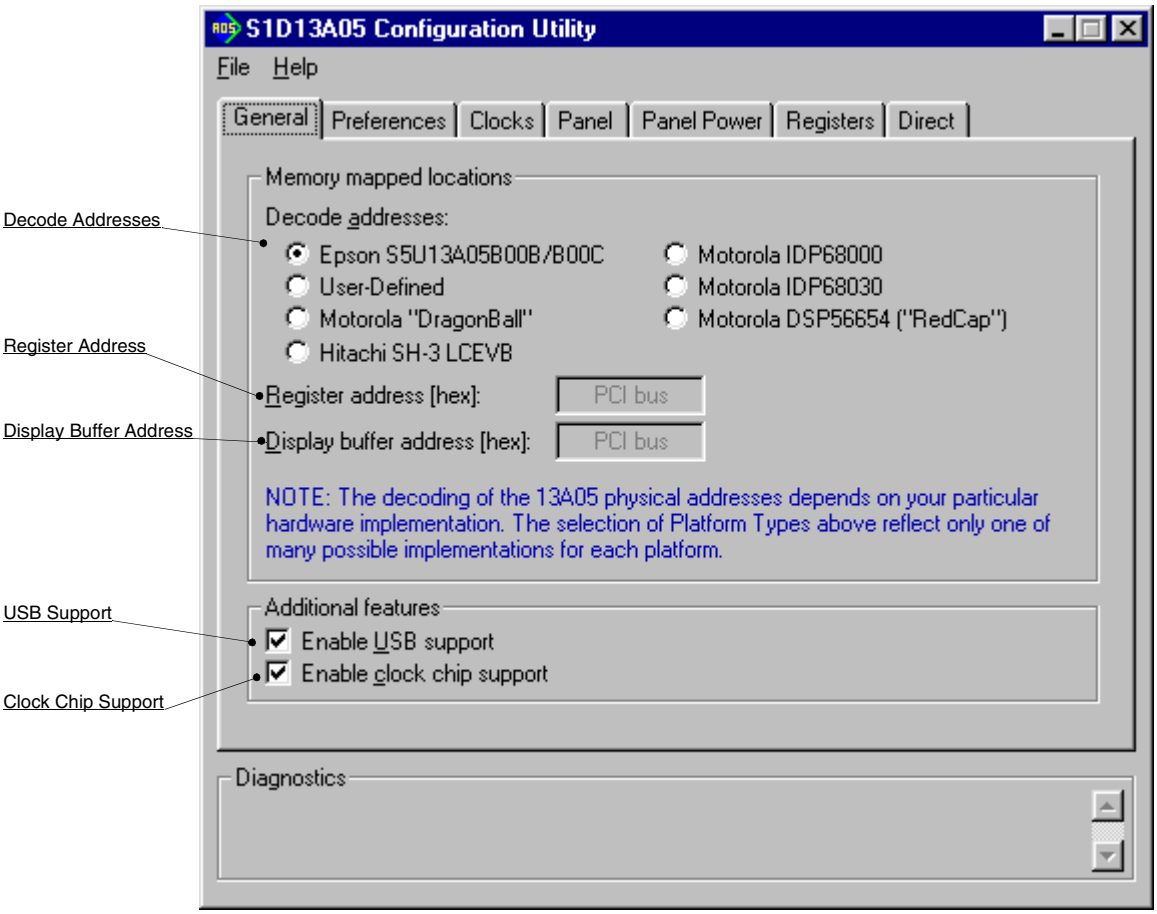
   Several ASCII text file formats are supported. Most are formatted C header files used to build display drivers or standalone applications.

   Utility files based on the Hardware Abstraction Layer (HAL) can be modified directly by 13A05CFG.

# 13A05CFG Configuration Tabs

13A05CFG displays a series of tabs which can be selected at the top of the main window. Each tab allows the configuration of a specific aspect of S1D13A05 operation. The following sections describe the purpose and use of each of the tabs.

## General Tab




The General tab contains settings that define the S1D13A05 operating environment.

Decode Addresses

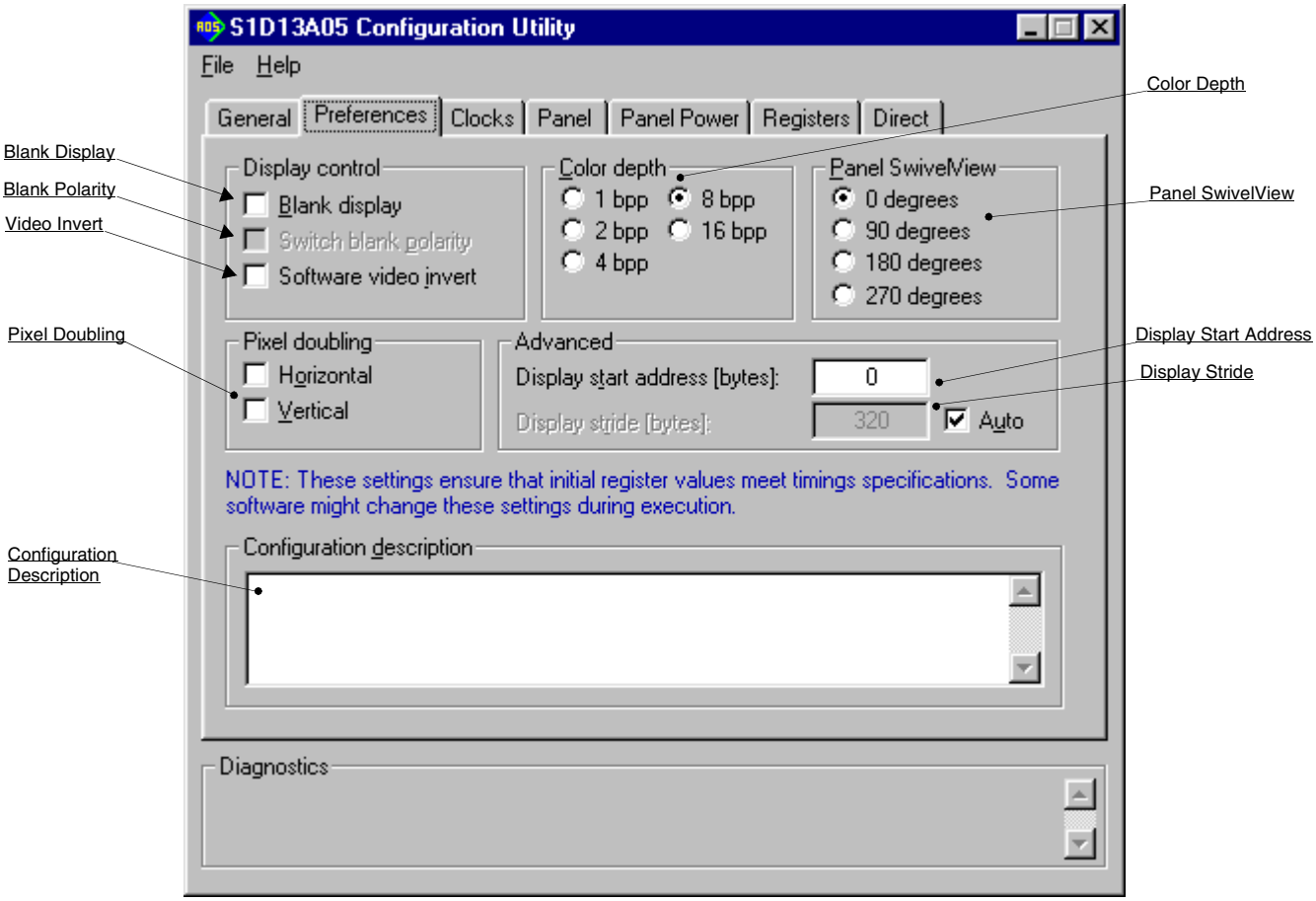
Selecting one of the listed evaluation platforms changes the values for the “Register address” and “Display buffer address” fields. The values used for each evaluation platform are examples of possible implementations as used by the Epson evaluation board. If your hardware implementation differs from the addresses used, select the User-Defined option and enter the correct values for “Register address” and “Display buffer address”.

**Note**

When "Epson S5U13A05B00B/B00C Evaluation Board" is selected, the register and display buffer addresses are blanked because the evaluation board uses the PCI interface and the decode addresses are determined by the system BIOS during boot-up.

| | |
|---|---|
| Register Address | The physical address of the start of register decode space (in hexadecimal).<br><br>This field is automatically set according to the Decode Address unless the "User-Defined" decode address is selected. |
| Display Buffer Address | The physical address of the start of display buffer decode space (in hexadecimal).<br><br>This field is automatically set according to the Decode Address unless the "User-Defined" decode address is selected. |
| USB Support | The S1D13A05 contains a USB client controller. If this box is checked, chip initialization configures GPIO[7:4] for use by the USB controller. For further information on the S1D13A05 USB implementation, see the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx. |
| Clock Chip Support | The S1D13A05 evaluation board implements a Cypress ICD2061A Clock Synthesizer which can be used to generate CLKI and CLKI2. When this box is checked, GPIO[3:1] are reserved for Clock Synthesizer support. Selecting a HR-TFT, Type 2 TFT, Type 3 TFT, or Casio TFT panel will disable this feature as the HR-TFT requires GPIO[3:0].<br><br>**This feature is only available when using the S1D13A05 evaluation board.** |

## Preferences Tab

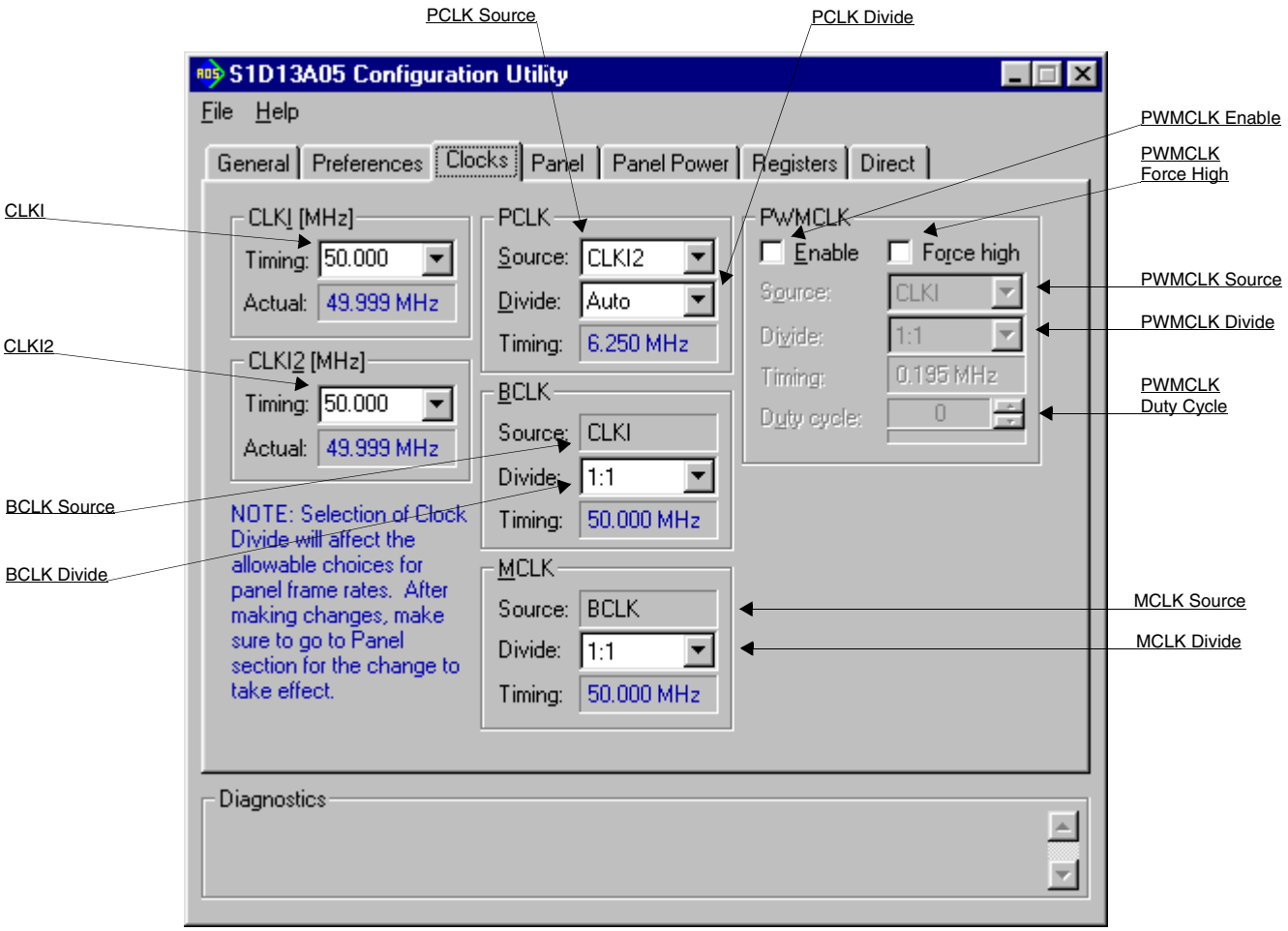



The Preference tab contains settings pertaining to the initial display state. During runtime these settings may be changed.

| | |
|---|---|
| Blank Display | The S1D13A05 can blank the LCD display by forcing all FPDAT lines used by the panel to either zeros or ones (as selected by the Switch Blank Polarity option). When this box is checked the display is blanked. |
| Blank Polarity | When this box is checked the FPDAT lines are forced to ones instead of zeros when the LCD display is blanked. When the box remains un-checked the FPDAT lines are forced to zeros when the LCD display is blanked. This option only has an effect when Blank Display is enabled. |
| Video Invert | The S1D13A05 can invert the display data going to the LCD panel. When this box is checked, video data is inverted. Display data is inverted after the Look-Up Table, which means colors are truly inverted. |

| | |
|---|---|
| Pixel Doubling | These settings allow the Pixel Doubling feature to be configured independently in the horizontal and vertical dimensions. Pixel doubling causes each pixel of display data to be extended to two pixels. This feature can be useful for using existing software on larger panels. |
| Horizontal | When this box is checked, pixel doubling in the horizontal direction is enabled. **Note that the S1D13A05 does not support horizontal pixel doubling for SwivelView 90° or 270° modes.** |
| Vertical | When this box is checked, pixel doubling in the vertical direction is enabled. **Note that the S1D13A05 does not support vertical pixel doubling for SwivelView 90° or 270° modes.** |
| Configuration Description | This field allows the user to enter a description for a particular configuration. This field is saved in the HAL information and is displayed when a HAL-based utility is run. |
| Color Depth | Sets the initial color depth on the LCD panel. If there is insufficient display buffer for the selected width and height then a warning is displayed in the diagnostic area. |
| Panel SwivelView | The S1D13A05 SwivelView feature is capable of rotating the image displayed on an LCD panel 90°, 180°, or 270° in a counter-clockwise direction. This setting determines the initial orientation of the panel. |
| Advanced | These settings allow fine tuning of the start address and stride. The start address defines the offset into the display buffer (video memory) of the pixel which will be displayed in the top left corner of the panel. Stride defines the number of bytes required to step from the first pixel on one row to the first pixel on the next row (i.e. 160 pixel wide display at 16 bpp requires 320 bytes per horizontal row). |
| Display Start Address | This option sets the start address for the main window of the panel. Typically the start address is set to zero. |
| Display Stride | This option sets the stride for the main window of the panel. To set the stride equal to the size of the display, select the “auto” box. To increase the stride, uncheck the “auto” box and enter the desired stride.<br>**Note**<br>The stride value must be greater than or equal to the number of bytes required by one line of display memory. |

## Clocks Tab




The Clocks tab simplifies the selection of input clock frequencies and the sources of internal clocking signals. For further information regarding clocking and clock sources, refer to the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx.

The CLKI and CLKI2 frequencies represent clock values the system provides to the S1D13A05. It is the responsibility of the system designer to ensure that the correct clock frequencies are supplied to the S1D13A05. The S1D13A05 may use one or two clock sources. Two clock sources allow greater flexibility in the selection of display type and memory speed.

**Note**

Changing clock values may modify or invalidate Panel settings. Confirm all settings on the Panel tab after changing any clock settings.

When “Enable clock chip support” is selected on the General Tab, 13A05CFG performs calculations to determine the nearest actual clock frequency generated by the programmable clock. When clock chip support is disabled, 13A05CFG assumes the input clocks will be derived from a clock source of exactly the indicated frequency.

**CLKI**

This setting determines the frequency of CLKI.

Timing

Set this value by selecting a preset frequency from the drop down list or entering the desired frequency (MHz) in the edit box.

Actual

This field displays the actual value of the CLKI frequency. If “Enable clock chip support” is selected on the General Tab, then this value may differ slightly from the value entered in the timing control.

**CLKI2**

This setting determines the frequency of CLKI2.

Timing

Set this value by selecting a preset frequency from the drop down list or entering the desired frequency (MHz) in the edit box.

Actual

This field displays the actual value of the CLKI2 frequency. If “Enable clock chip support” is selected on the General Tab, then this value may differ slightly from the value entered in the timing control.

**PCLK**

These settings select the clock source and divisor for the internal pixel clock (PCLK).

Source

Selects the PCLK source. Possible sources include CLKI, CLKI2, BCLK or MCLK. Note that BCLK and MCLK may be previously divided from CLKI or CLKI2.

Divide

Specifies the divide ratio for the clock source. The divide ratio is applied to the PCLK source to derive PCLK.

Selecting “Auto” for the divisor allows the configuration program to calculate the best clock divisor. Unless a very specific clocking is being specified, it is best to leave this setting on “Auto”.

Timing

This field shows the actual PCLK used by the configuration process.

| | |
|---|---|
| **BCLK** | These settings select the clock source and divisor for the internal bus interface clock (BCLK). |
| Source | The BCLK source is always CLKI. |
| Divide | Specifies the divide ratio for the clock source. The divide ratio is applied to the BCLK source to derive BCLK. |
| Timing | This field shows the actual BCLK frequency used by the configuration process. |
| **MCLK** | These settings select the clock source and input clock divisor for the internal memory clock (MCLK). For the best performance, MCLK should be set as close to the maximum (50 MHz) as possible. |
| Source | The MCLK source is always BCLK. |
| Divide | Specifies the divide ratio for the clock source. The divide ratio is applied to the MCLK source to derive MCLK.<br><br>This divide ratio should be left at 1:1 unless the resultant MCLK is greater that 50MHz. |
| Timing | This field shows the actual MCLK frequency used by the configuration process. |

**PWMCLK**

These controls configure various PWMCLK settings. The PWMCLK is the internal clock used by the Pulse Width Modulator for output to the panel.

Enable

When this box is checked, the PWMCLK circuitry is enabled.

Force High

The signal PWMOUT is forced high when this box is checked. When not checked, PWMOUT will be low if PWM is not enabled or will change state according to the configured values when PWM is enabled.

Source

Selects the PWMCLK source. Possible sources include CLKI, CLKI2, MCLK, and PCLK.

Divide

Specifies the divide ratio for the clock source. The divide ratio is applied to the PWMCLK source to derive PWMCLK.

**Note**

After this divide is applied, PWMCLK is further divided by 256 to achieve the final PWMCLK frequency.

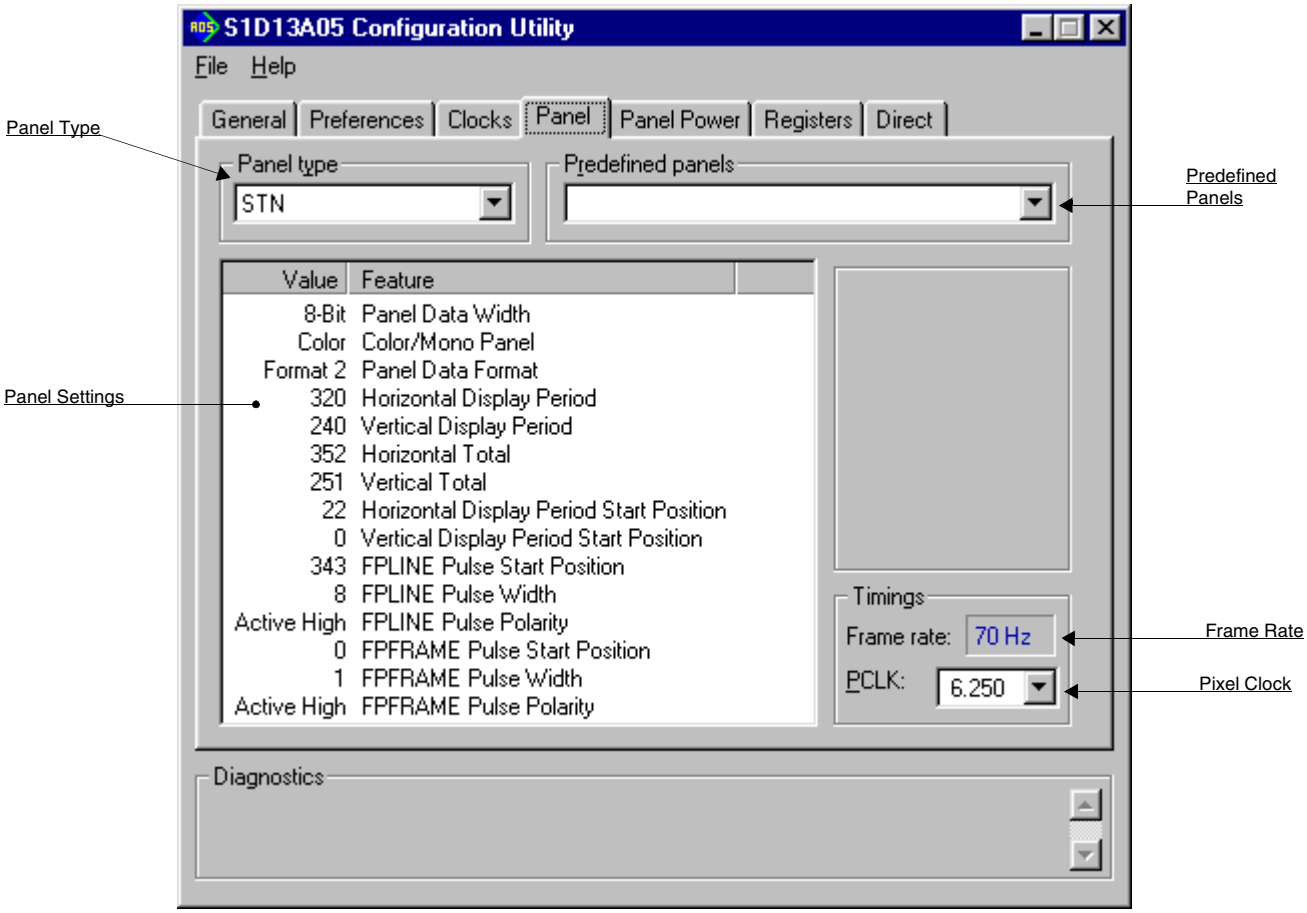
Timing

This field shows the actual PWMCLK frequency used by the configuration process.

Duty Cycle

Selects the number of cycles that PWMOUT is high out of 256 clock periods.

## Panel Tab




The S1D13A05 supports several panel types. This tab allows configuration of most panel related settings such as dimensions, type and timings.

| | |
|---|---|
| Panel Type | Selects the panel type (i.e. STN, TFT, HR-TFT, etc).<br><br>Some “Panel Settings” options may change or become unavailable when this control is changed. Re-confirm all settings on this tab after the Panel Type is changed. |
| Predefined Panels | 13A05CFG uses a file (**panels.def**) which contains predefined settings for a number of LCD panels. If the file **panels.def** is present in the same directory as **13A05cfg.exe**, the predefined panels are available in the drop-down list. If a panel is selected from the list, 13A05CFG pre-configures its settings to nominal panel values. |

Panel Settings

This area allows the user to configure a number of panel specific settings. Items listed here change according to the panel type selected.

The following settings can be changed within this pane. For more details on any of the following settings, see the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx.

Panel Data Width

Selects the panel data width. Panel data width is the number of bits of data transferred to the LCD panel on each clock cycle and shouldn't be confused with color depth which determines the number of displayed colors.

When a passive panel type is selected, the available options are 4, 8, and 16 bit. When an active panel type (TFT/HR-TFT) is selected, the available options are 9, 12, and 18 bit.

Color/Mono Panel

Selects between a monochrome or color panel.

Panel Data Format

Selects the color STN panel data format. This option only applies to 8-bit color STN panels. Most new panels use the format 2 data format.

See the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx, for description of format 1 / format 2 data formats.

Horizontal and Vertical Display Period

These fields specify the panel width and height. A number of common widths and height are available in the selection boxes. If the width/height of your panel is not listed, enter the actual panel dimensions into the edit field.

For passive panels, manually entered pixel widths must be a minimum of 32 pixels and can be increased by multiples of 16. For TFT panels, manually entered pixel widths must be a minimum of 8 pixels and can be increased by multiples of 8. If a value is entered that does not meet these requirements, 13A05CFG rounds up the value to the next allowable width. The changed value is reported in the diagnostics portion of the window.

Horizontal Total

Sets the number of pixels on each line of the display. This value is the sum of both the visible (Horizontal Display Period) and non-visible (Horizontal Non-Display Period) values. It is recommended that the automatically generated values be used. However, manual adjustment may be used to improve the quality of the displayed image by fine tuning the horizontal display total.

Refer to *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx, for a complete description of the Display Total settings.

**Note**

If the horizontal total is set too small, 13A05CFG will display a yellow warning message in the diagnostics portion of the window.

Vertical Total

Sets the number of lines of the display. This value is the sum of both the visible (Vertical Display Period) and non-visible (Vertical Non-Display Period) values. It is recommended that the automatically generated values be used. However, manual adjustment may be used to improve the quality of the displayed image by fine tuning the vertical display total.

Refer to *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx, for a complete description of the Display Total settings.

**Note**

If the vertical total is set too small, 13A05CFG will display a yellow warning message in the diagnostics portion of the window.

Horizontal Display Period Start Position

It is recommended that the automatically generated values be used. However, manual adjustment may be used to improve the quality of the displayed image by fine tuning the horizontal display period start positions.

Refer to *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx, for a complete description of the Display Start settings.

**Note**

If the horizontal display start values are set to values that violate the *S1D13A05 Hardware*

*Functional Specification*, 13A05CFG will display a yellow warning message in the diagnostics portion of the window.

Vertical Display Period Start Position

It is recommended that the automatically generated values be used. However, manual adjustment may be used to improve the quality of the displayed image by fine tuning the vertical display period start positions.

Refer to *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx, for a complete description of the Display Start settings.

**Note**

If the vertical display start values are set to values that violate the *S1D13A05 Hardware Functional Specification*, 13A05CFG will display a yellow warning message in the diagnostics portion of the window.

FPLINE Start Position

Specifies the delay (in pixels) from the start of the horizontal non-display period to the leading edge of the FPLINE pulse.

FPLINE Pulse Width

Specifies the width (in pixels) of the horizontal sync signal (FPLINE).

FPLINE Pulse Polarity

Specifies the polarity (active high or active low) of the horizontal sync signal (FPLINE).

**Note**

Selecting the wrong pulse polarity may damage the panel.

FPFRAME Start Position

Specifies the delay (in lines) from the start of the vertical non-display period to the leading edge of the FPFRAME pulse.

FPFRAME Pulse Width

Specifies the pulse width (in lines) of the vertical sync signal (FPFRAME).

FPFRAME Pulse Polarity

Specifies the polarity (active high or active low) of the vertical sync signal (FPFRAME).

**Note**

Selecting the wrong pulse polarity may damage the panel.

| | |
|---|---|
| CLS Pulse Width | Sets the width of CLS signals in PCLKs. **This setting is used for HR-TFT panels only.** |
| PS1 Rising Edge | Selects the number of PCLKs between the CLS falling edge and the PS1 rising edge. **This setting is used for HR-TFT panels only.** |
| PS2 Rising Edge | Selects the number of PCLKs between the CLS falling edge and the PS2 rising edge. **This setting is used for HR-TFT panels only.** |
| PS2 Toggle Width | Sets the width of the PS2 signal before toggling (in number of PCLKs). **This setting is used for HR-TFT panels only.** |
| PS3 Signal Width | Sets the width of the PS3 signal in PCLKs. **This setting is used for HR-TFT panels only.** |
| REV Toggle Point | Sets the width in PCLKs to toggle the REV signal to LP rising edge. **This setting is used for HR-TFT panels only.** |
| PS1/2 End | Allows the PS signal to continue into vertical non-display period (in lines). **This setting is used for HR-TFT panels only.** |
| POL Type | Selects how often the POL signal is toggled (as either ever line or every frame). **This setting is used for Type 2 TFT panels only.** |
| AP Pulse Width | Selects the AP width used for the TFT Type 2 interface (in PCLKs). **This setting is used for Type 2 TFT panels only.** |
| AP Rising Edge Position | Controls the TFT Type 2 AC timing parameter from the rising edge of FPLINE (STB) to the rising edge of GP101 (AP) (in PCLKs). **This setting is used for Type 2 TFT panels only.** |
| VCLK Hold | Controls the AC timing parameter from the rising edge of FPLINE (STB) to the falling edge of GPIO0 (VCLK) (in PCLKs). **This setting is used for Type 2 TFT panels only.** |
| VCLK Setup | Controls the AC timing parameter from the rising edge of GPIO0 (VCLK) to the rising edge of FPLINE (STB) (in PCLKs). **This setting is used for Type 2 TFT panels only.** |

POL Toggle Position — Sets the toggle position of the POL signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

OE Pulse Width — Sets the pulse width of the OE signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

OE Rising Edge Position — Sets the rising edge position of the OE signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

XOEV Falling Edge Position — Sets the falling edge position of the XOEV signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

XOEV Rising Edge Position — Sets the rising edge position of the XOEV signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

CPV Pulse Width Position — Sets the pulse width of the CPV in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

VCOM Toggle Position — Sets the toggle position of the VCOM signal in 2 pixel resolution. **This setting is used for Type 3 TFT panels only.**

PCLK2 Divide Rate — Selects the divide rate for PCLK2 (GPO5). **This setting is used for Type 3 TFT panels only.**

PCLK1 Divide Rate — Selects the divide rate for PCLK1 (GPO4). **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Refresh Cycle — Selects the refresh cycle for the Partial Mode Display (as value from 0 to 63). **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Enable — Enables the Partial Mode Display. **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Type — Selects the type of Partial Mode Display. Stripe means that only the Y Position registers are used in calculating the partial display, where Block means that both the X and Y Position registers are used. **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Area 2 Enable — Enables the Area 2 for Partial Mode Display. **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Area 1 Enable Enables the Area 1 for Partial Mode Display. **This setting is used for Type 3 TFT panels only.**

Partial Mode Display Area 0 Enable Enables the Area 0 for Partial Mode Display. **This setting is used for Type 3 TFT panels only.**

Partial Area 0 Y End PositionSelects the Y End Position of Partial Area 0 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 0 X End PositionSelects the X End Position of Partial Area 0 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 0 Y Start PositionSelects the Y Start Position of Partial Area 0 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 0 X Start PositionSelects the X Start Position of Partial Area 0 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 1 Y End PositionSelects the Y End Position of Partial Area 1 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 1 X End PositionSelects the X End Position of Partial Area 1 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 1 Y Start PositionSelects the Y Start Position of Partial Area 1 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 1 X Start PositionSelects the X Start Position of Partial Area 1 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 2 Y End PositionSelects the Y End Position of Partial Area 2 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 2 X End PositionSelects the X End Position of Partial Area 2 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 2 Y Start PositionSelects the Y Start Position of Partial Area 2 in 8 line resolution. **This setting is used for Type 3 TFT panels only.**

Partial Area 2 X Start Position Selects the X Start Position of Partial Area 2 in 8 pixel resolution. **This setting is used for Type 3 TFT panels only.**

Command 1 Store Stores command 1 for the TFT Type 3 Interface. **This setting is used for Type 3 TFT panels only.**

Command 0 Store Stores command 0 for the TFT Type 3 Interface. **This setting is used for Type 3 TFT panels only.**

Source Driver IC Number Selects the number of Source Driver ICs. **This setting is used for Type 3 TFT panels only.**

Command Send Request Enables the S1D13A05 to send the command in the next non-display period. **This setting is used for Type 3 TFT panels only.**

GPCK Rising Edge to STH Pulse Sets the number of PCLKs from GPCK rising edge to STH pulse. **This setting is used for Casio TFT panels only.**

GRES Falling Edge to FRP Toggle Point Sets the number of PCLKs from GRES falling edge to FRP toggle point. **This setting is used for Casio TFT panels only.**

GRES Falling Edge to GPCK Rising Edge Sets the number of PCLKs from GRES falling edge to GPCK rising edge. **This setting is used for Casio TFT panels only.**

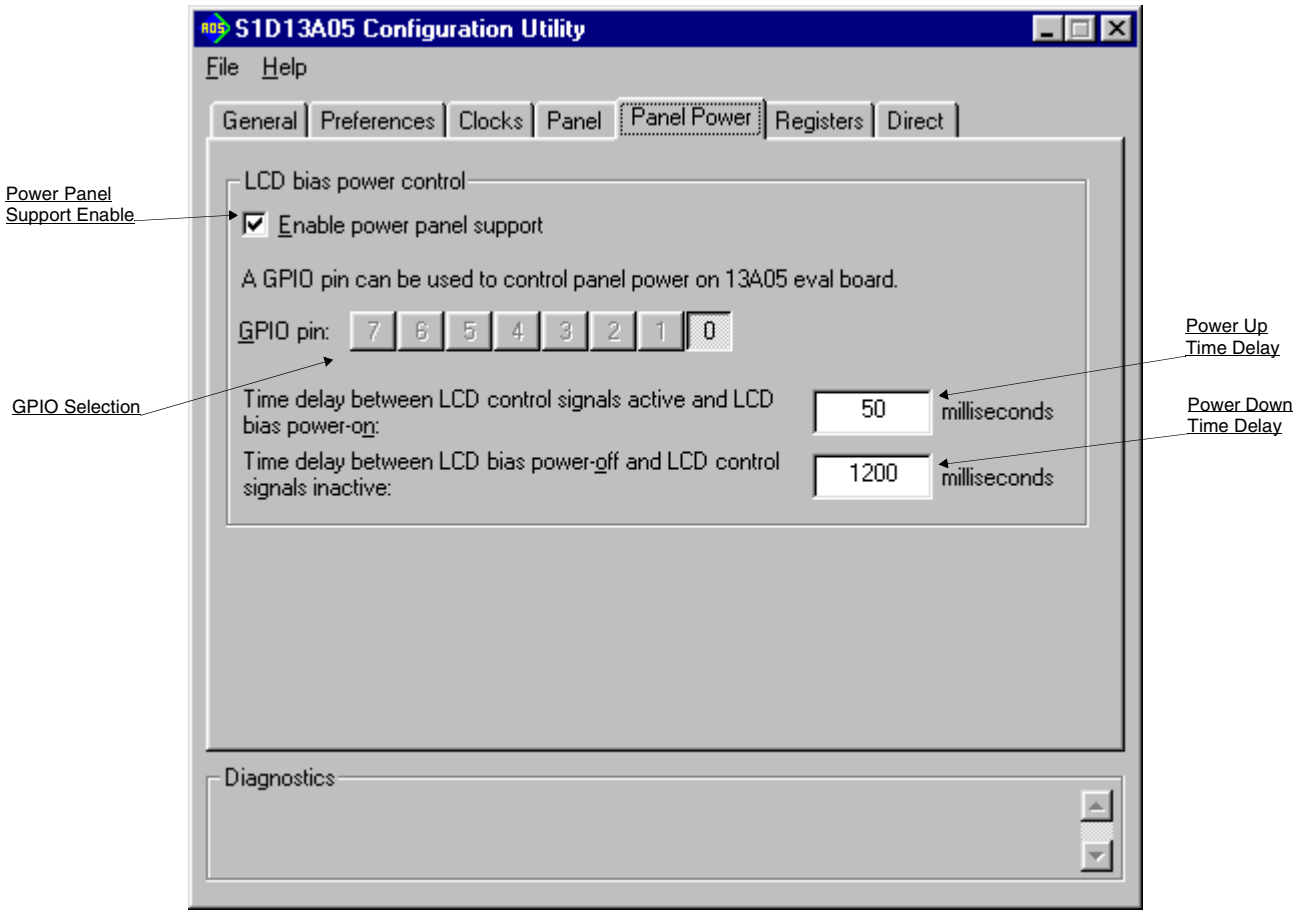
GPCK Rising Edge to GRES Rising Edge Sets the number of PCLKs from GPCK rising edge to GRES rising edge. **This setting is used for Casio TFT panels only.**

Frame Rate The Frame Rate (in Hz) is calculated and displayed based on the current settings as selected on the various tabs. If the resulting Frame Rate is not acceptable, adjust the settings to change the frame rate.

Panel dimensions are fixed therefore frame rate can only be adjusted by changing either the PCLK frequency or display total values.

Pixel Clock Select the desired Pixel Clock (in MHz) from the drop-down list. The range of frequencies displayed is dependent on the PCLK source and divide settings as selected on the Clocks tab.

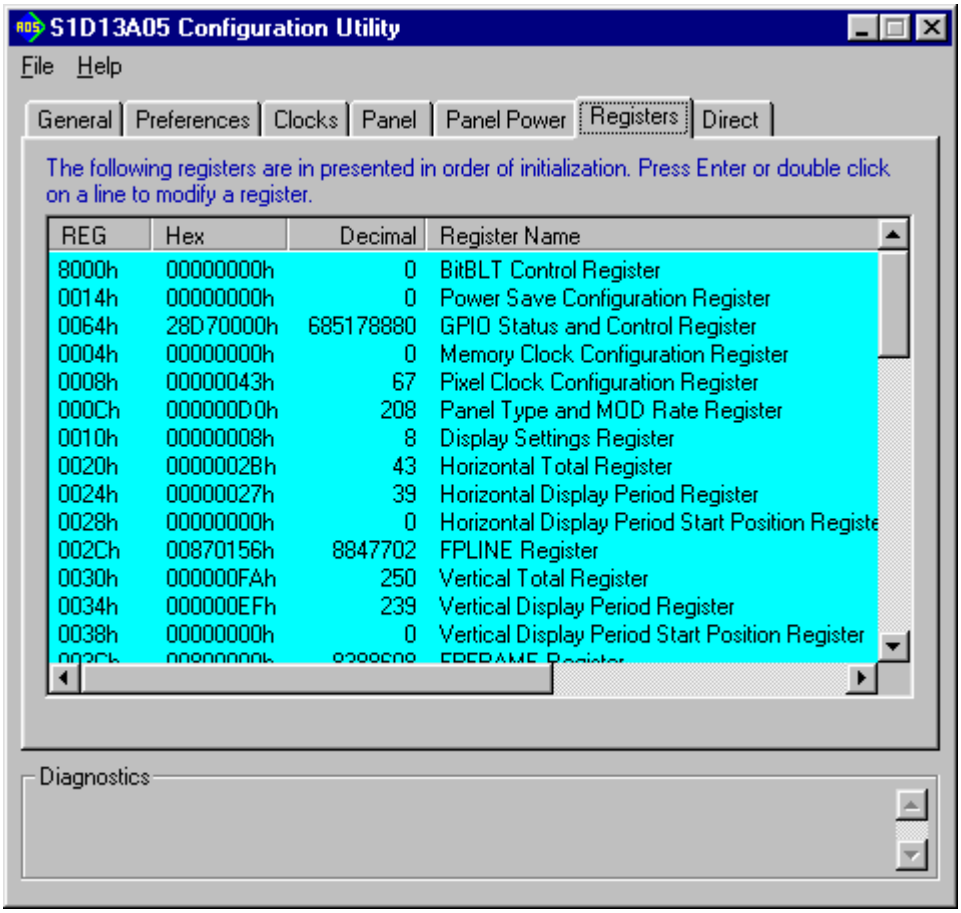
## Panel Power Tab



The S1D13A05 evaluation board is designed to use a GPIO signal to control the LCD bias power. The following settings configure panel power support.

| | |
|---|---|
| Power Panel Support Enable | When this box is checked, the LCD bias power to the panel is controlled by the selected GPIO pin. When this box is unchecked, the LCD bias power must be controlled by the CPU or some other means. |
| GPIO Selection | This setting selects the GPIO pin used to control the LCD bias power. The default is GPIO0 (GPIO0 is used on the S1D13A05 evaluation board). |
| Power Up Time Delay | This setting controls the maximum time delay between when the S1D13A05 control signals are turned on and the LCD panel is powered-on. This setting must be configured according to the specification for the panel being used.<br><br>This value is used by Epson evaluation software designed for the S1D13A05 evaluation board. |
| Power Down Time Delay | This setting controls the minimum time delay between when the LCD panel is powered-off and when the S1D13A05 control signals are turned off. This setting must be configured according to the specification for the panel being used.<br><br>This value is used by Epson evaluation software designed for the S1D13A05 evaluation board. |

## Registers Tab



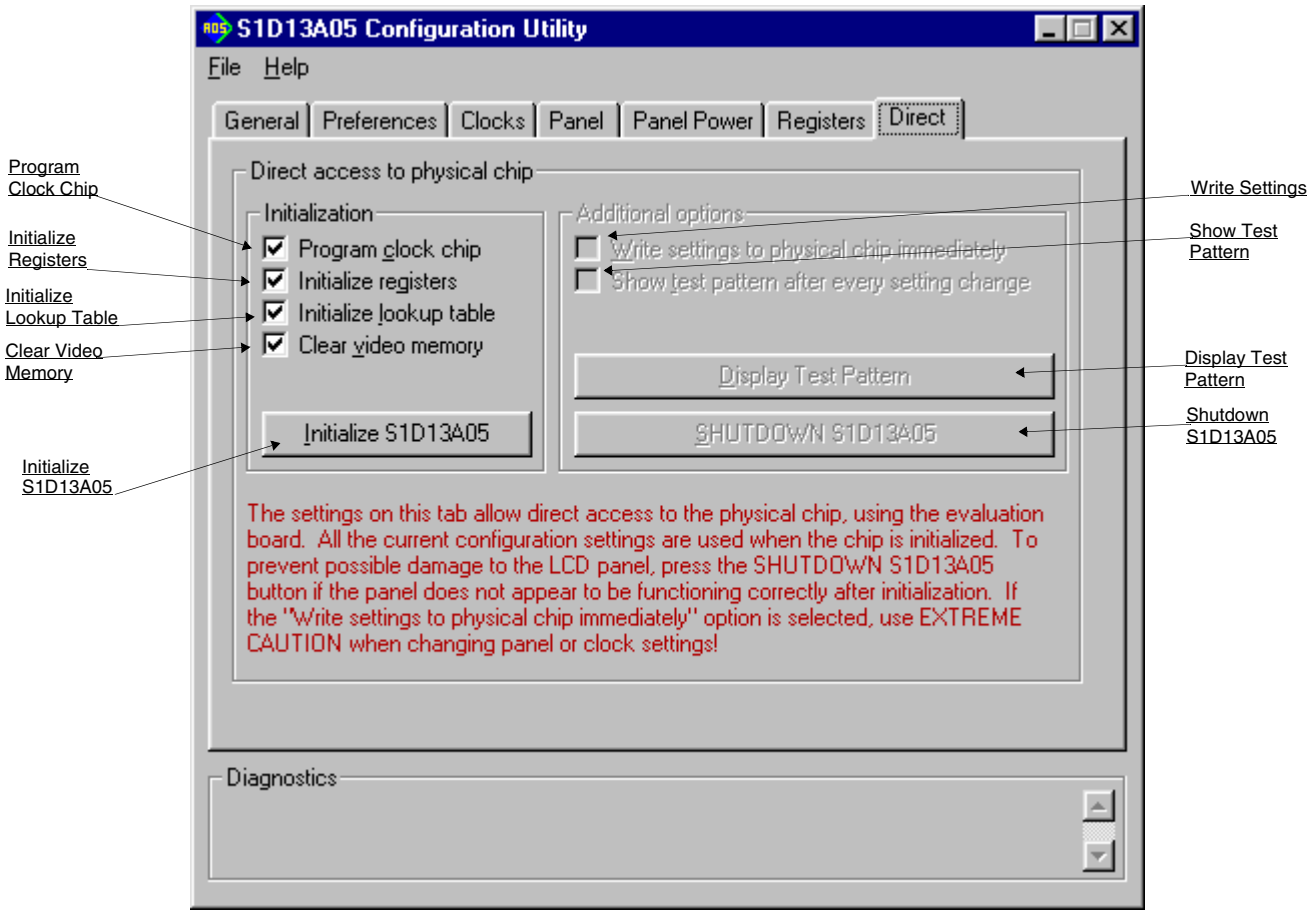

The Registers tab allows viewing and editing of the S1D13A05 register values.

Scroll up and down the list to view register values which are determined from the configuration settings of the previous tabs. Hovering over a register displays a pop-up help box which describes the functionality of the bits in that register. Register settings may be changed by double-clicking on the register in the listing. **Manual changes to the registers are not checked for errors, so caution is warranted when directly editing these values.** It is strongly recommended that the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx be referred to before making any manual register settings.

### Note

Manually entered values may be changed by 13A05CFG if further configuration changes are made on other tabs. In this case, the user is notified.

## Direct Tab




This tab allows the user to directly interact with the S1D13A05 configuration process. The effect of register changes on the displayed image can be observed before writing any configuration files. Fine tuning adjustments may be made to achieve the best possible image on the panel.

Using this tab requires that a S1D13A05 evaluation board is installed in the computer and a panel is attached.

Initialization — These settings define which actions will be carried out when the Initialize S1D13A05 button is clicked.

Program Clock Chip — The S5U13A05B00C evaluation board design includes a clock chip which can provide the signals for CLKI and CLKI2. Checking this box will include programming the clock chip as part of the S1D13A05 initialization.

Initialize Registers — When this box is checked the S1D13A05 registers will be programmed to their configured values as part of the initialization.

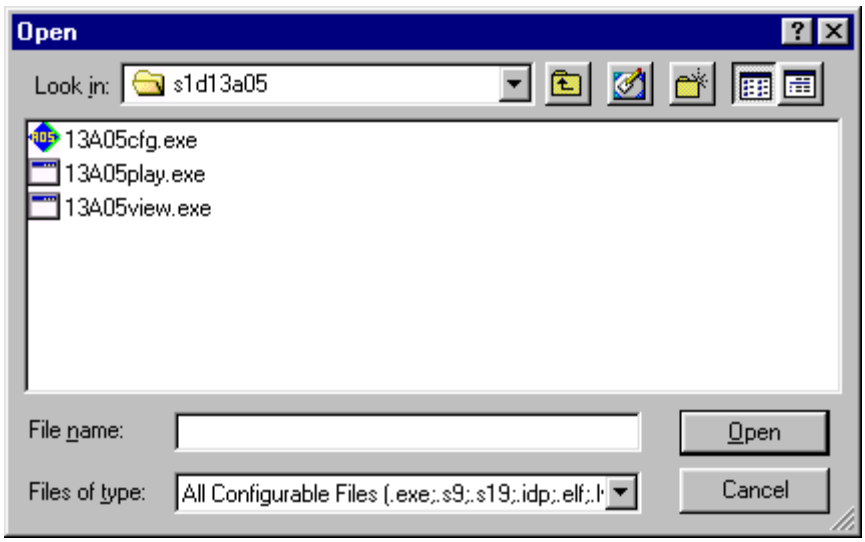
| | |
|---|---|
| Initialize Lookup Table | When this box is checked the S1D13A05 Lookup Table is programmed as part of the initialization. |
| Clear Video Memory | When this box is checked the S1D13A05 display buffer will be cleared (set to zeros) as part of the initialization. |
| Initialize S1D13A05 | Clicking this button initializes the S1D13A05 according to the options selected. |
| Additional Options | After initializing the S1D13A05, these further options become available. |
| Write Settings | This setting should be used with caution. Checking this box will cause setting changes on any tab to immediately update the associated register(s). |
| Show Test Pattern | Checking this box will update the test pattern in the display buffer after every setting change. This is useful when fine tuning panel settings as the results of the change are immediately visible. |
| Display Test Pattern | Clicking this button causes 13A05CFG to draw a test pattern into display memory. The pattern is based on the configured width, height, rotation and color depth. |
| Shutdown S1D13A05 | Clicking this button shuts down the S1D13A05. This feature is necessary should a setting change appear to be damaging or harmful to the attached panel. |

# 13A05CFG Menus

The following sections describe each of the options in the File and Help menus.

## Open...

From the Menu Bar, select “File”, then “Open...” to display the Open File Dialog Box.




The Open option allows 13A05CFG to read the configuration information from programs based on the HAL library. When 13A05CFG opens a file it scans the file for an identification string, and if found, reads the configuration information. This feature may be used to quickly arrive at a starting point for register configuration. The only requirement is that the file being opened must contain a valid S1D13A05 HAL library information block.

13A05CFG supports a variety of executable file formats. Select the file type(s) 13A05CFG should display in the Files of Type drop-down list and then select the filename from the list and click on the Open button.

**Note**

13A05CFG is designed to work with utilities programmed using a given version of the HAL. If the configuration structure contained in the executable file differs from the version 13A05CFG expects the Open will fail and an error message is displayed. This may happen if the version of 13A05CFG is substantially older, or newer, than the file being opened.

## Save

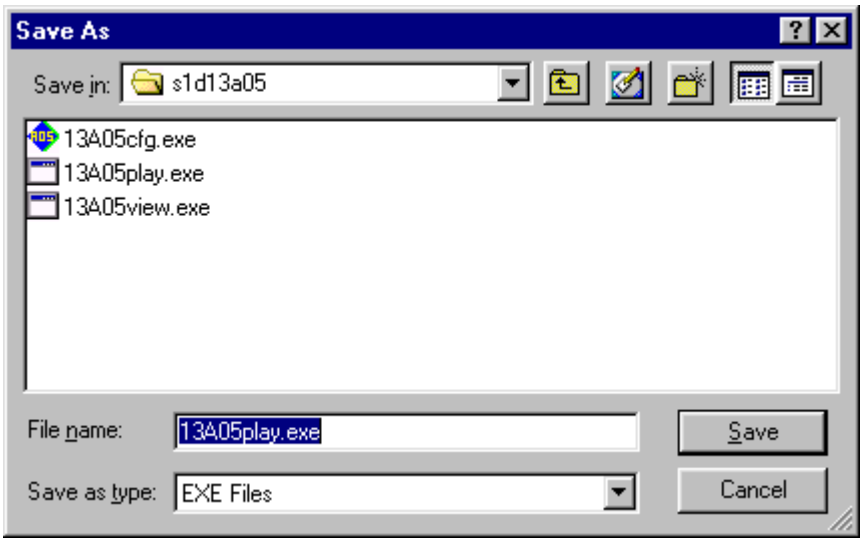
From the Menu Bar, select “File”, then “Save” to initiate the save action. The Save menu option allows a fast save of the configuration information to a file that was opened with the Open menu option.

**Note**

This option is only available once a file has been opened.

## Save As...

From the Menu Bar, select “File”, then “Save As...” to display the Save As Dialog Box.




“Save as” is very similar to Save except a dialog box is displayed allowing the user to name the file before saving.

Using this technique a tester can configure a number of files differing only in configuration information and name (e.g. BMP60Hz.EXE, BMP72Hz.EXE, BMP75Hz.EXE where only the frame rate changes in each of these files).

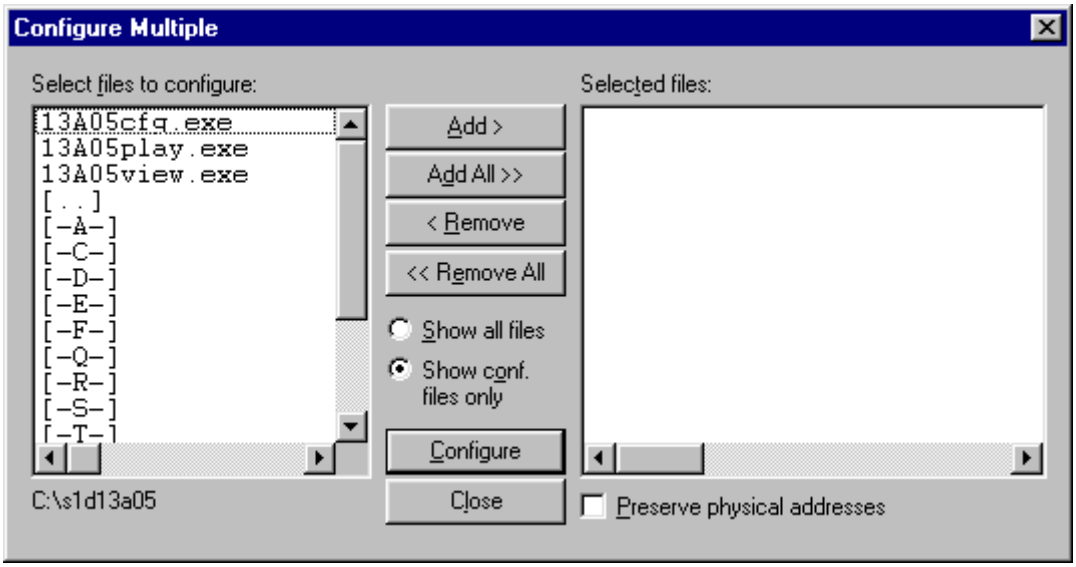
**Note**

When “Save As” is selected then an exact duplicate of the file as opened by the “Open” option is created containing the new configuration information.

## Configure Multiple

After determining the desired configuration, “Configure Multiple” allows the information to be saved into one or more executable files built with the HAL library.

From the Menu Bar, select “File”, then “Configure Multiple” to display the Configure Multiple Dialog Box.This dialog box is also displayed when a file(s) is dragged onto the 13A05CFG window.




The left pane lists files available for configuration; the right pane lists files that have been selected for configuration. Files can be selected by clicking the “Add” or “Add All” buttons, double clicking any file in the left pane, or by dragging the file(s) from Windows Explorer.

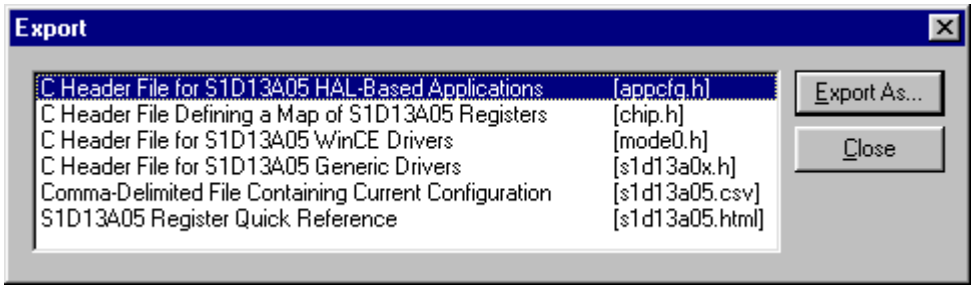
Selecting “Show all files” displays all files in the selected directory, whereas selecting “Show conf. files only” will display only files that can be configured using 13A05CFG (i.e. .exe, .s9).

Checking “Preserve Physical Addresses” instructs 13A05CFG to use the register and display buffer address values the files were previously configured with. Addresses specified in the General Tab are discarded. This is useful when configuring several programs for various hardware platforms at the same time. For example, if configuring PCI, MPC and IDP based programs at the same time for a new panel type, the physical addresses for each are retained. This feature is primarily intended for the test lab where multiple hardware configurations exist and are being tested.

## Export

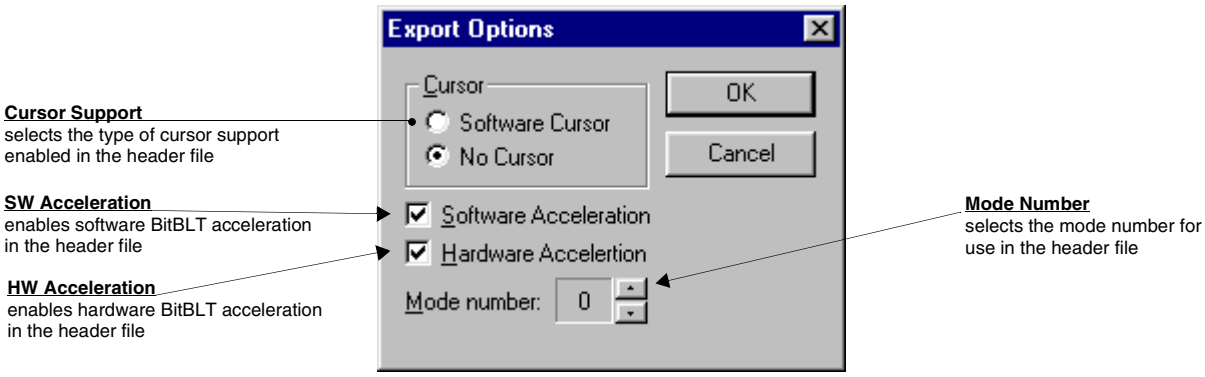
After determining the desired configuration, “Export” permits the user to save the register information as a variety of ASCII text file formats. The following is a list and description of the currently supported output formats:

- a C header file for use in writing HAL library based applications.
- a C header file which lists each register and the value it should be set to.
- a C header file for use in developing Window CE display drivers.
- a C header file for use in developing display drivers for other operating systems such as Linux, QNX, and VxWorks WindML.
- a comma delimited text file containing an offset, a value, and a description for each S1D13A05 register.
- a .html based reference guide to the S1D13A05 registers.




After selecting the file format, click the “Export As..." button to display the file dialog box which allows the user to enter a filename before saving. Clicking the “Preview” button uses Notepad or the web browser to display a copy of the file to be saved.

When the **C Header File for S1D13A05 WinCE Drivers** option is selected as the export type, additional options are available and can be selected by clicking on the Options button. The options dialog appears as:



## Enable Tooltips

Tooltips provide useful information about many of the items on the configuration tabs. Placing the mouse pointer over nearly any item on any tab generates a popup window containing helpful advice and hints.

To enable/disable tooltips check/uncheck the “Tooltips” option form the “Help” menu.

**Note**
Tooltips are enabled by default.

## Tooltip Delay

This option sets the length of time the cursor must be left over an item before its associated tooltip is displayed.

## ERD on the Web

This “Help” menu item is actually a hotlink to the Epson Research and Development website. Selecting “Help” then “ERD on the Web” starts the default web browser and points it to the ERD product web site.

The latest software, drivers, and documentation for the S1D13A05 is available at this website.

## Update Common Controls

13A05CFG uses some of the latest common control DLLs. On systems using earlier versions of the common controls, certain controls may not appear correctly. This option updates the Common Controls required for proper operation of 13A05CFG.

## About 13A05CFG

Selecting the “About 13A05CFG” option from the “Help” menu displays the about dialog box for 13A05CFG. The about dialog box contains version information and the copyright notice for 13A05CFG.

## Comments

- On any tab particular options may be grayed out if selecting them would violate the operational specification of the S1D13A05 (i.e. Selecting TFT or STN on the Panel tab enables/disables options specific to the panel type).
- The file **panels.def** is a text file containing operational specifications for several supported, and tested, panels. This file can be edited with any text editor.
- 13A05CFG allows manually altering register values. The manual changes may violate memory and LCD timings as specified in the *S1D13A05 Hardware Functional Specification*, document number X40A-A-001-xx. If this is done, unpredictable results may occur. Epson Research and Development, Inc. does not assume liability for any damage done to the display device as a result of configuration errors.
- Yellow diagnostic warnings are designed to draw attention to important errors in the configuration and should be corrected before saving the configuration.
- **13A05CFG** can be configured by making a copy of the file 13A05cfg.exe and configuring the copy. It is not possible to configure the original while it is running. The newly saved information becomes the default configuration for that copy of 13A05cfg.exe.

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