EPSON
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S1V30080 Series
Evaluation Board
User's Guide

SEIKO EPSON CORPORATION

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1. Introduction

1.1 Overview

This evaluation kit is a customer evaluation kit for use with the S1V30080 voice LSI (hereinafter referred to as the "voice LSI").

The kit consists of a "Cinderella" voice LSI evaluation board and associated components. The Cinderella board features the push switches, clock, DIP switches, audio amplifier, and host CPU interface necessary for voice LSI evaluation.

The following functions are provided by using the board on its own or in conjunction with a "CASTLE" board incorporating a voice LSI control host CPU.

- **Data writing function from CASTLE to flash memory on Cinderella board**

  This function allows S1V30080 ROM data in the micro SD card inserted in the CASTLE board to be written to the flash memory on the Cinderella board.

  Data is written with the Cinderella connected to the CASTLE.

  The data written can be accessed as a standalone Cinderella demo or by connecting an external host CPU.

- **Cinderella standalone demo function**

  Evaluation is possible with the standalone Cinderella using the built-in ROM of the S1V30080 or data in the Cinderella flash memory. Push switches on the Cinderella are used for selecting audio and starting and stopping playback with the S1V30080 in standalone mode.

  With this function, the host interface mode written in the data must be either "Standalone 1" or "Standalone 2."

- **External host CPU connection function**

  This function connects the Cinderella board to the host CPU board used by the customer.

  This allows debugging of the voice LSI control program using the built-in ROM of the S1V30080 or data in the Cinderella flash memory.

  With this function, the host interface mode written in the data may be "SPI (clock synchronized serial)," "I2C," "Standalone 1" or "Standalone 2."

1.2 Cinderella board series configuration

The Cinderella boards are configured as shown below.

Table 1.1 Cinderella board series configuration

Board model number	S5U1V30080D00A1	S5U1V30080D00A3
S1V30080 model number	S1V30080F00A300	S1V30080F00A300
Built-in ROM data	Japanese voice data	Japanese voice data
Interface mode when initialized by built-in ROM	I2C	I2C
Default data in external flash memory	Non-Japanese voice data	Japanese voice data
Interface mode when initialized by external flash memory (default)	Standalone 2	Standalone 2

Note For details of the default data contained in the ROM and flash memory, refer to the *S5U1V30080D00A1 Data List* or *S5U1V30080D00A3 Data List* provided separately.

1.3 User guide overview

This user guide is arranged as follows.

Section 2 describes the preparations before use, the names and functions of the items included with the evaluation kit as preparation for use.

Section 3 describes how to use the evaluation kit.

Section 4 describes precautions when using the evaluation kit.

Section 5 includes the evaluation kit circuit diagrams.

2. Before Starting

This section describes the names and functions of the items included with the evaluation kit as preparation for use.

2.1 Items provided

1) Cinderella (S1V30080 voice LSI evaluation board) ×1
2) Customer's host CPU interface cable (for connecting to CON3) ×1
3) Speaker cable ×1
4) CASTLE (host CPU board for voice LSI control) ×1
5) micro SD card ×1
6) micro SD card USB adapter ×1
7) Evaluation board USB power supply cable ×1
8) Cinderella – CASTLE connector cable (Note 1) ×1
9) Item list and sheet describing voice LSI web page ×1

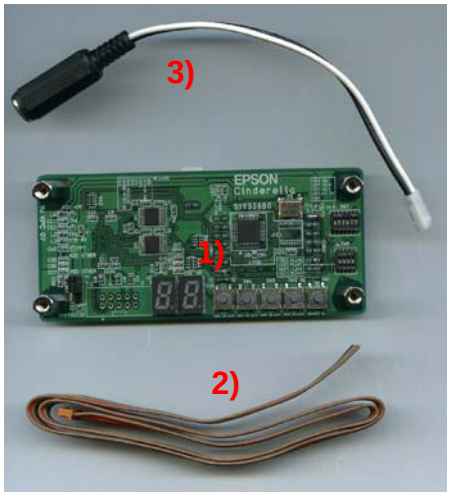

Figure 2.1

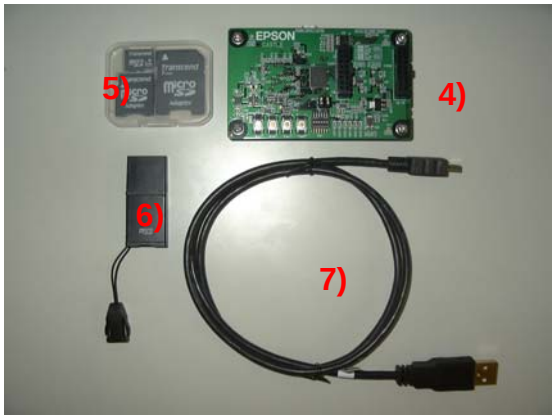

Figure 2.2

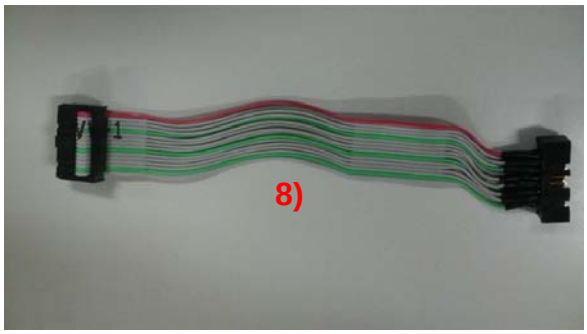

Figure 2.3

Note Items 2), 3), 5), 6), 7), and 8) may differ from those shown in the photographs here.

Note 1 Used for S1V30080 demo with the CASTLE, and not within the scope of this document.

2.2 Cinderella (S1V30080 voice LSI evaluation board)

2.2.1 Part names and functions

Figures 2.4 and 2.5 illustrate the main parts of the Cinderella board.

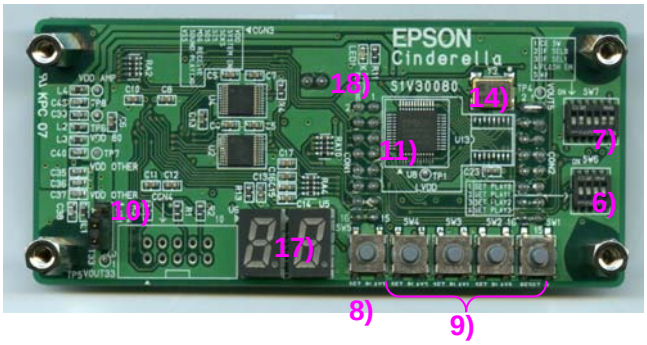

Figure 2.4 Cinderella board obverse side

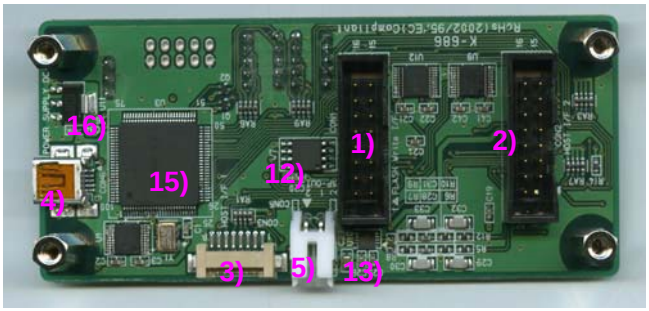

Figure 2.5 Cinderella board reverse side

- Connectors

  1) Flash memory write connector CON1 (Slave)

  This is used to write ROM data to the flash memory on the Cinderella by connecting to CON1 on the CASTLE.

  The CON1 pin layout is shown in Table 2.1.

Table 2.1 Cinderella CON1

connector	No.	I/O	Cinderella CON1	CASTLE CON1	signal level
CON1	1	-	-	VDD1 (+5 V)	-
	2	-	-	VDD2 (+3.3 V)	-
	3	-	-	VDD3 (+1.8 V)	-
	4	-	-	CLOCK_OUT	-
	5	-	-	NRESET	-
	6	I	SCKS_FLASH	SCKM	3.3 V LVCMOS
	7	I	SIS_FLASH	SOM	3.3 V LVCMOS
	8	O	SOS_FLASH	SIM	3.3 V LVCMOS
	9	I	NSCSM_FLASH	NSCSM	3.3 V LVCMOS
	10	-	-	MSGRDY	-
	11	-	-	STBYEXIT	-
	12	-	-	MUTE	-
	13	P	VSS	VSS	-
	14	P	VSS	VSS	-
	15	P	VSS	VSS	-
	16	P	VSS	VSS	-

2) Host interface connector CON2 (Slave)

This is used for controlling the S1V30080 on the Cinderella via the host CPU. Messages can be sent to the S1V30080 from the host CPU via the I2C, Standalone 1, or Standalone 2 interface.

It should be connected to CON2 on the CASTLE, and this also allows interfacing via I2C. A 3.3 V system power supply is also fed from the CASTLE via VDD2 (+3.3 V) at the same time.

The CON2 pin layout is shown in Table 2.2.

Table 2.2 Cinderella CON2

connector	No.	I/O	Cinderella CON2	Castle CON2	signal level
CON2	1	P	- (None)	VDD1 (+5 V)	-
	2	P	VDD	VDD2 (+3.3 V)	-
	3	P	-	VDD3 (+1.8 V)	-
	4	I	SCLK	GPIO0	3.0-5.5 V CMOS
	5	IO	SDA	GPIO1	3.0-5.5 V CMOS
	6	I	SET_PLAY0	GPIO2	3.0-5.5 V CMOS
	7	I	SET_PLAY1	GPIO3	3.0-5.5 V CMOS
	8	I	SET_PLAY2	GPIO4	3.0-5.5 V CMOS
	9	I	SET_PLAY3	GPIO5	3.0-5.5 V CMOS
	10	O	MSG_RECEIVE	GPIO6	3.0-5.5 V CMOS
	11	O	SOUND_PLAYING	GPIO7	3.0-5.5 V CMOS
	12	I	SYSTEM_EN	GPIO8	3.0-5.5 V CMOS
	13	P	VSS	VSS	-
	14	P	VSS	VSS	-
	15	P	VSS	VSS	-
	16	P	VSS	VSS	-

Note Details of how to control the S1V30080 on the Cinderella board using CASTLE are not included in this document. Contact Seiko Epson for more information.

3) Host interface connector CON3 (Slave)

This is used for controlling the S1V30080 on the Cinderella by the host CPU. Messages can be sent to the S1V30080 from the host CPU via the SPI, I2C, clock synchronized serial, Standalone 1, or Standalone 2 interface.

The CON3 pin layout is shown in Table 2.3.

Table 2.3 Cinderella CON3

connector	No.	I/O	Cinderella CON3	External host CPU	signal level
CON3	1	P	VDD	VDD	-
	2	I	SYSTEM_EN	SYSTEM_EN	3.0-5.5 V CMOS
	3	I	SCKS/SCLK/SET_PLAY[1]	SCKM	3.0-5.5 V CMOS
	4	IO	SIS/SDA/SET_PLAY[0]	SOM	3.0-5.5 V CMOS
	5	IO	SOS/-/SET_PLAY[2]	SIM	3.0-5.5 V CMOS
	6	IO	MSG_RECEIVE/SET_PLAY[3]	MSG_RECEIVE	3.0-5.5 V CMOS
	7	O	SOUND_PLAYING	SOUND_PLAYING	3.0-5.5 V CMOS
	8	P	VSS	VSS	-

4) Mini-USB power supply connector CON6

This provides a single 5 V DC power supply from USB connector J7 on the Cinderella board.

* Do not provide power from this connector when VDD is fed from J1 or J3 on the Cinderella board. This will short-circuit the power supply, possibly resulting in damage.

5) Voice output connector CON5

This should be connected using the speaker cable provided.

- Switches

  6) DIP switch 1 (SW6)

  This DIP switch can be used as an auxiliary for demos in standalone 1 mode with the Cinderella board on its own. For details, refer to "3.2 Cinderella board standalone demo."

  7) DIP switch 2 (SW7)

  This DIP switch is used for the various Cinderella board settings.

  For details of the DIP switch 2 (SW7) functions, refer to Table 2.4.

  For DIP switch definitions, refer to "4.1 DIP switch definitions."

Table 2.4 Cinderella SW7

SW No.	Function	Description
SW7-1	S1V30080 internal regulator control	Off: Normal operation On: S1V30080 stopped * Should normally be set to "Off: Normal operation."
SW7-2	Interface mode lower-order bit	* Controls the 7-segment LED display supporting interface mode by setting the CPLD interface mode combining SW7-2 and SW7-3 for Cinderella standalone demo operation. For Cinderella standalone demo operation, use in conjunction with S1V30080 ROM data I/F mode settings. For correlation of functions with interface mode, refer to Table 2.5.
SW7-3	Interface mode higher-order bit	
SW7-4	External flash memory access control * Selects whether to use data written to the external flash memory or S1V30080 internal ROM data.	Off: External flash memory access On: S1V30080 internal ROM access
SW7-5	External flash memory write protection	Off: Permits external flash memory writing On: Protects external flash memory data * For details, refer to "3.1 Writing data to Cinderella board."
SW7-6	Test switch	Always use in the On position.

Table 2.5 Cinderella SW7-2/3

SW7-3	SW7-2	Interface mode
ON	ON	• Writing data to Cinderella board • Cinderella + CASTLE demo • Connecting to an external host CPU
OFF	ON	Cinderella standalone demo Standalone 1
OFF	OFF	Cinderella standalone demo Standalone 2

8) Reset switch (SW1)

Push-switch SW1 is used for system resetting the Cinderella board. After turning on the power or altering the DIP switches, always press SW1 to reset the system, or reset the system externally via host interface connector J3 or J1.

9) Cinderella standalone demo control push-switches (SW2 to SW5)

Push-switches SW2 to SW5 are used to control the Cinderella standalone demo functions.

For details, refer to "3.2 Cinderella board standalone demo."

10) CPLD and external flash memory power supply selection jumper JP1

Depends on the external power supply voltage.

Refer to Table 2.6.

Table 2.6 Cinderella JP1

Host CPU board voltage	JP1
3.0-3.6 (V)	Short circuit Pin 1 to 2
3.6-5.5 (V)	Short circuit Pin 2 to 3
With CASTLE connected (3.3 V ±0.3 V)	Short circuit Pin 1 to 2
With power supply from mini-USB connector CON6	Short circuit Pin 2 to 3

* Avoid short-circuiting pin 1 to 2 with a 5 V power supply, as this will subject the CPLD and external flash memory to a voltage exceeding the specified ratings and result in damage.

- Other main components

  11) S1V30080

      Incorporates the S1V30080 QFP12-48 package items.

  12) S1V30080 external flash memory

      Flash memory for storing S1V30080 data. Communication with the S1V30080 uses the clock-synchronized serial interface.

  13) S1V30080 external audio signal amplifier

  14) S1V30080 clock generator

      This includes a 16.384 MHz crystal oscillator for the S1V30080.

      Set the input clock division ratio as appropriate to suit the sampling frequency and DAC bit width. For details, refer to the *S1V30080 Series Hardware Specifications* and *S1V30080 Series Message Protocol Specifications*.

  15) 7-segment LED driver CPLD

      Drives the 7-segment LED according to the interface mode, and displays the file index number on the 7-segment LED in "Standalone 1" or "Standalone 2."

  16) CPLD and external flash memory step-down regulator

      Generates a 3.3 V ±0.3 V power supply voltage for the CPLD and external flash memory when the external supply voltage is between 3.6 V and 5.5 V.

  17) Standalone mode 7-segment LED

      Displays the file index number in "Standalone 1" or "Standalone 2."

  18) LED indicator

      Illuminates when connected to the S1V30080 SOUND_PLAYING and play-back is in progress.

2.2.2 Cinderella block diagram

Figure 2.6 illustrates the Cinderella block diagram.

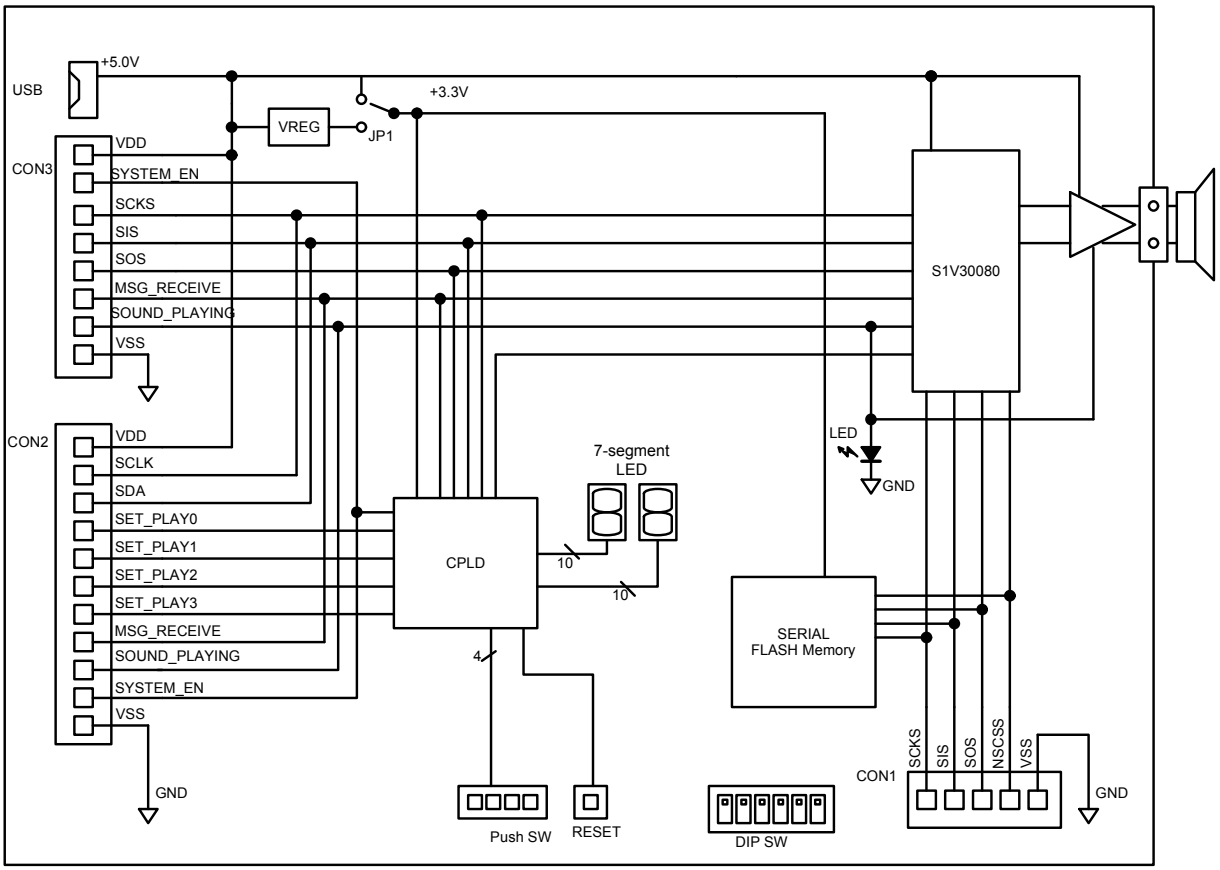

Figure 2.6 Cinderella block diagram

2.3 CASTLE board

The CASTLE board can be used for writing ROM data to the Cinderella board flash memory.

The CASTLE can also be used to control the S1V30080 on the Cinderella board. Details of how to control the S1V30080 on the Cinderella board using the host CPU on the CASTLE are not included in this document. Contact Seiko Epson for more information.

2.3.1 CASTLE Part names and functions

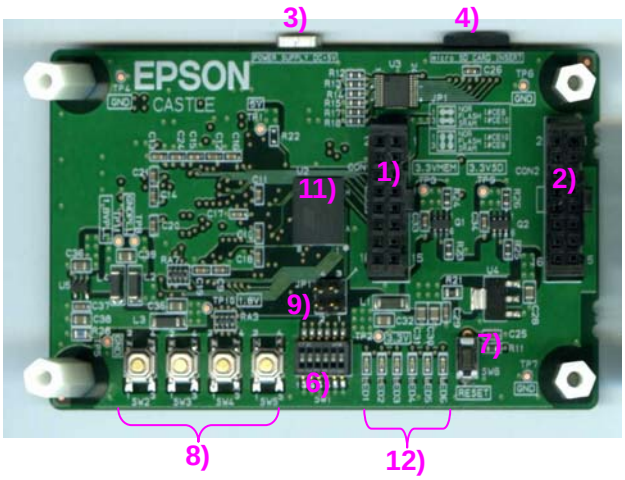

Figure 2.7 CASTLE board obverse side

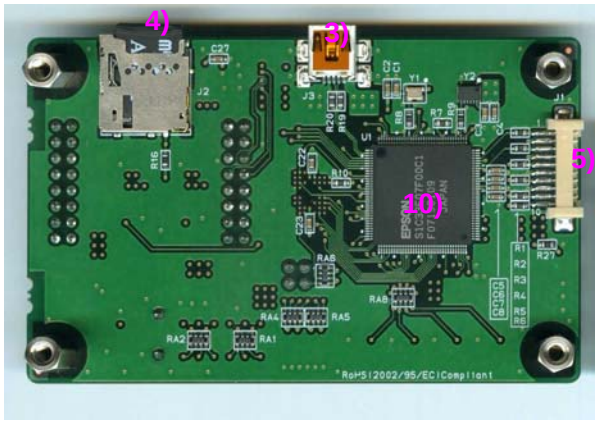

Figure 2.8 CASTLE board reverse side

The main components of the CASTLE board shown in Figures 2.7 and 2.8 are described below.

- Connectors

  1) Host interface connector CON1 (Master)

     This is connected to J4 on the Cinderella board and is used when writing ROM data to the flash memory on the Cinderella board.

     The CON1 pin layout is shown in Table 2.7.

Table 2.7 CASTLE CON1

connector	No.	I/O	CASTLE CON1	Cinderella J11	signal level
CON1	1	-	VDD1 (+5 V)	-	-
	2	-	VDD2 (+3.3 V)	-	-
	3	-	VDD3 (+1.8 V)	-	-
	4	-	CLOCK_OUT	-	-
	5	-	NRESET	-	-
	6	O	SCKM	SCKS_FLASH	3.3 V LVCMOS
	7	O	SOM	SIS_FLASH	3.3 V LVCMOS
	8	I	SIM	SOS_FLASH	3.3 V LVCMOS
	9	O	NSCSM	NSCSM_FLASH	3.3 V LVCMOS
	10	-	MSGRDY	-	-
	11	-	STBYEXIT	-	-
	12	-	MUTE	-	-
	13	P	VSS	VSS	-
	14	P	VSS	VSS	-
	15	P	VSS	VSS	-
	16	P	VSS	VSS	-

2) Host interface connector CON2 (Master)

This is connected to CON2 on the Cinderella board and is used for controlling the S1V30080 on the Cinderella board.

Messages can be sent to the S1V30080 from the voice LSI control S1C33E07 via the I2C, Standalone 1, or Standalone 2 interface.

The CON2 pin layout is shown in Table 2.8.

Table 2.8 CASTLE CON2

connector	No.	I/O	CASTLE	Cinderella	signal level
CON2	1	P	VDD1 (+5 V)	-	-
	2	P	VDD2 (+3.3 V)	VDD	-
	3	P	VDD3 (+1.8 V)	-	-
	4	O	SCLK	SCLK	3.3 V CMOS
	5	O	SDA	SDA	3.3 V CMOS
	6	O	SET_PLAY0	SET_PLAY0	3.3 V CMOS
	7	O	SET_PLAY1	SET_PLAY1	3.3 V CMOS
	8	O	SET_PLAY2	SET_PLAY2	3.3 V CMOS
	9	O	SET_PLAY3	SET_PLAY3	3.3 V CMOS
	10	I	MSG_RECEIVE	MSG_RECEIVE	3.3 V CMOS
	11	I	SOUND_PLAYING	SOUND_PLAYING	3.3 V CMOS
	12	O	SYSTEM_EN	SYSTEM_EN	3.3 V CMOS
	13	P	VSS	VSS	-
	14	P	VSS	VSS	-
	15	P	VSS	VSS	-
	16	P	VSS	VSS	-

3) Mini-USB power supply connector

This provides a single 5 V DC power supply from USB connector J3 on the CASTLE board.

When connected to the Cinderella board, power is fed from the CASTLE board to the Cinderella board via host interface connector CON2 VDD2 pin.

4) ROM data storage micro SD connector

For inserting a micro SD card containing ROM data.

The CASTLE transfers to the flash memory on the Cinderella board via CON1 in accordance with the voice data stored.

5) S1C33E07 debugging ICD interface connector

Used for voice LSI control S1C33E07 debugging. The S1C33E07 program is written in the flash/SRAM multi-chip memory.

Do not use this connector.

- Switches

  6) DIP switch (SW1)

     The settings of this DIP switch are used to select the CASTLE board function.

  7) Reset switch (SW6)

     Push-switch SW6 is used for system resetting the CASTLE board. After turning on the power or altering the DIP switches, always press SW6 to reset the system.

  8) CASTLE control push-switches (SW2 to SW5)

     Push-switches SW2 to SW5 are used to control the CASTLE.

  9) S1C33E07 external memory selection jumper pin

     Check that JP1 is set to the default setting as shown in Table 2.9.

Table 2.9 JP1 setting

JP1 setting	Remarks
Short circuit Pin 1 to 3, Pin 2 to 4	Default

- Other main components

  10) Voice LSI control S1C33E07

      32-bit RISC controller

  11) Flash/SRAM multi-chip memory

      S1C33E07 external memory

  12) LED indicators (LED1 to LED6)

      The LEDs illuminate according to the operating status. Table 2.10 shows the LED indication patterns for the corresponding operating status, and Table 2.11 shows the error indication patterns.

Table 2.10 LED indication patterns

LED6	LED5	LED4	LED3	LED2	LED1	Description
Flashing	Flashing	Flashing	Flashing	Flashing	Flashing	When power is turned on (flashes repeatedly 3 times)
Off	Off	Off	On	Off	On	Cinderella board data writing mode
On	On	On	On	On	On	Cinderella board data writing complete

Table 2.11 Error indication patterns

LED6	LED5	LED4	LED3	LED2	LED1	Description
On	Off	Off	Off	Off	Flashing	SD card format error
Off	Off	On	On	Off	Flashing	Data transfer error
Off	On	On	On	Off	Flashing	Memory capacity overload
Off	Off	Off	Off	Off	Off	Communication error

2.3.2 CASTLE block diagram

Figure 2.9 illustrates the CASTLE board block diagram.

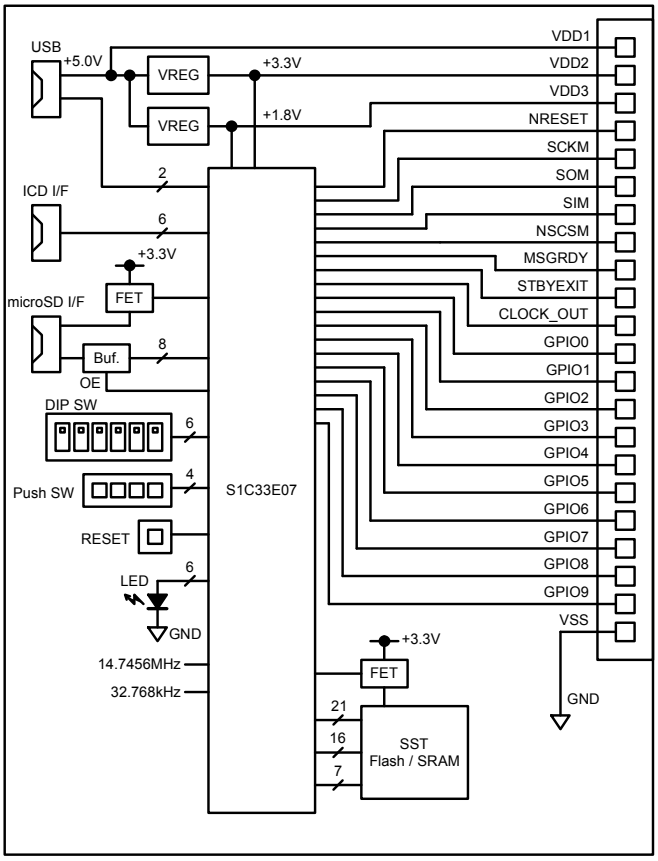

Figure 2.9 CASTLE board block diagram

2.4 Cinderella and CASTLE connection

This section explains how to connect the CASTLE board to the Cinderella board. Insert CON1 and CON2 on the Cinderella board into CON1 and CON2 on the CASTLE board. (Connections are unidirectional.) Figure 2.10 shows the Cinderella and CASTLE boards connected.

Figure 2.10

3. Usage Instructions

3.1 Writing data to Cinderella board

ROM data can be written to the Cinderella flash memory by connecting the Cinderella to the CASTLE. S1V30080 ROM data contained in the micro SD card inserted in the CASTLE board can be written to the Cinderella flash memory.

Data written can be accessed using Cinderella standalone demos or by connecting an external host CPU.

Note The product warranty does not cover using the CASTLE to write ROM data to a board other than the Cinderella board.

3.1.1 Data writing flowchart

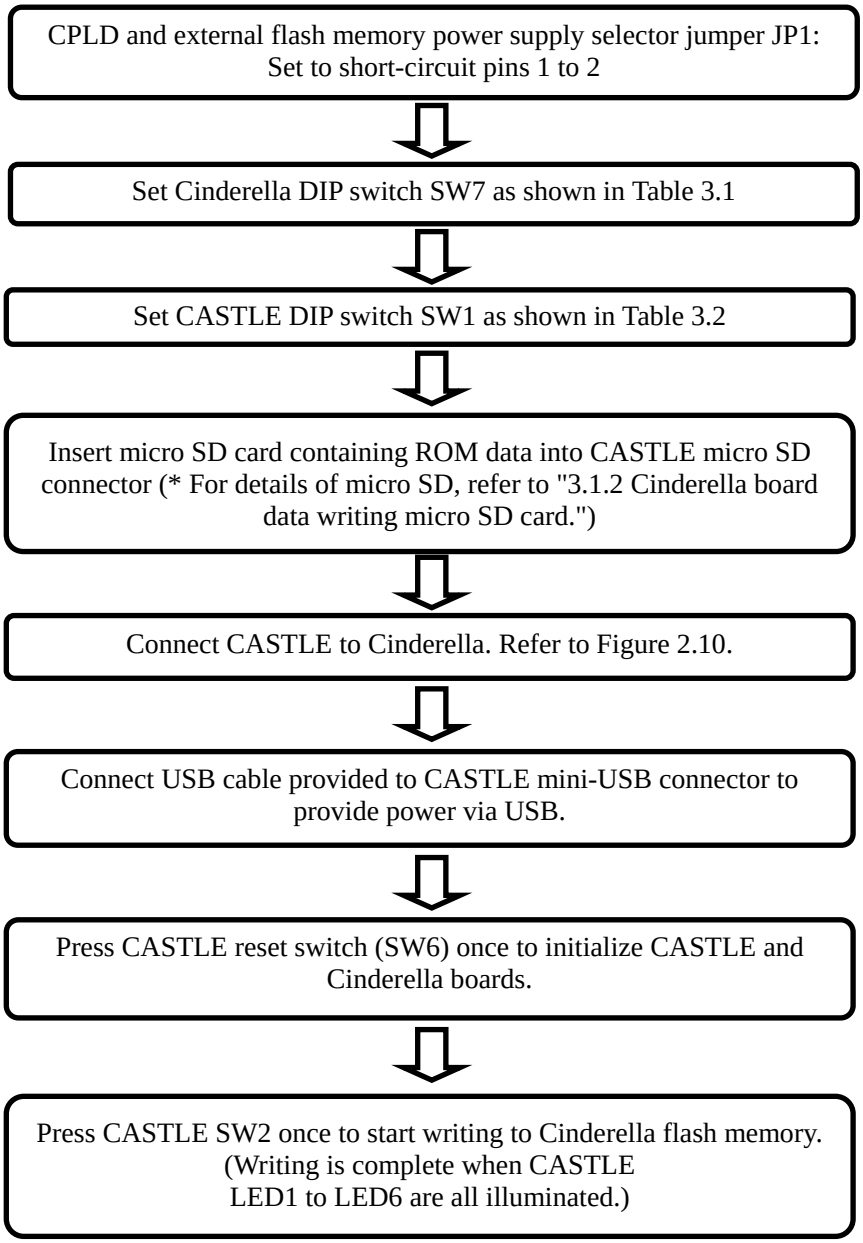

Table 3.1 Cinderella SW7 settings for writing data to Cinderella board

SW No.	Function	Description
SW7-1	S1V30080 internal regulator control	Off: Normal operation
SW7-2	Interface mode lower-order bit	ON
SW7-3	Interface mode higher-order bit	ON
SW7-4	External flash memory access control Selects whether to use data written to the external flash memory or S1V30080 internal ROM data.	On: S1V30080 internal ROM access Do not access from the S1V30080 to write from the flash memory write connector CON1.
SW7-5	External flash memory write protection	Off: Permits external flash memory writing
SW7-6	Test switch	On: Default

Table 3.2 CASTLE SW1 settings for writing data to Cinderella board

SW No.	Function	Description
SW1-1		Off: Default
SW1-2		Off: Default
SW1-3		Off: Default
SW1-4		Off: Default
SW1-5		Off: Default
SW1-6	Function selection	On: External flash write mode

3.1.2 Cinderella board data writing micro SD card

When using the function to write ROM data to the Cinderella board, the file shown in Table 3.3 is stored in a micro SD card and the card is inserted into the card slot on the CASTLE board.

Table 3.3 Storage file

File name	Description
ROMImage_YYMMDD_HHMMSS.bin	ROM data to be written to the Cinderella flash memory. The file name includes the date and time the file was created. This file is generated by the "S1V30080 Series Sound Tool." For more details of the "S1V30080 Series Sound Tool," refer to the *S1V30080 Series Sound Tool User Guide* provided separately.

3.2 Cinderella board standalone demo

A Cinderella board standalone demo is possible using the S1V30080 standalone mode.

The demo is possible using SW2 to SW5 on the Cinderella board.

Playback is possible using the S1V30080 internal ROM data or the ROM data written to the flash memory on the Cinderella board. In this case, the host interface mode of the ROM data must be "Standalone 1" or "Standalone 2."

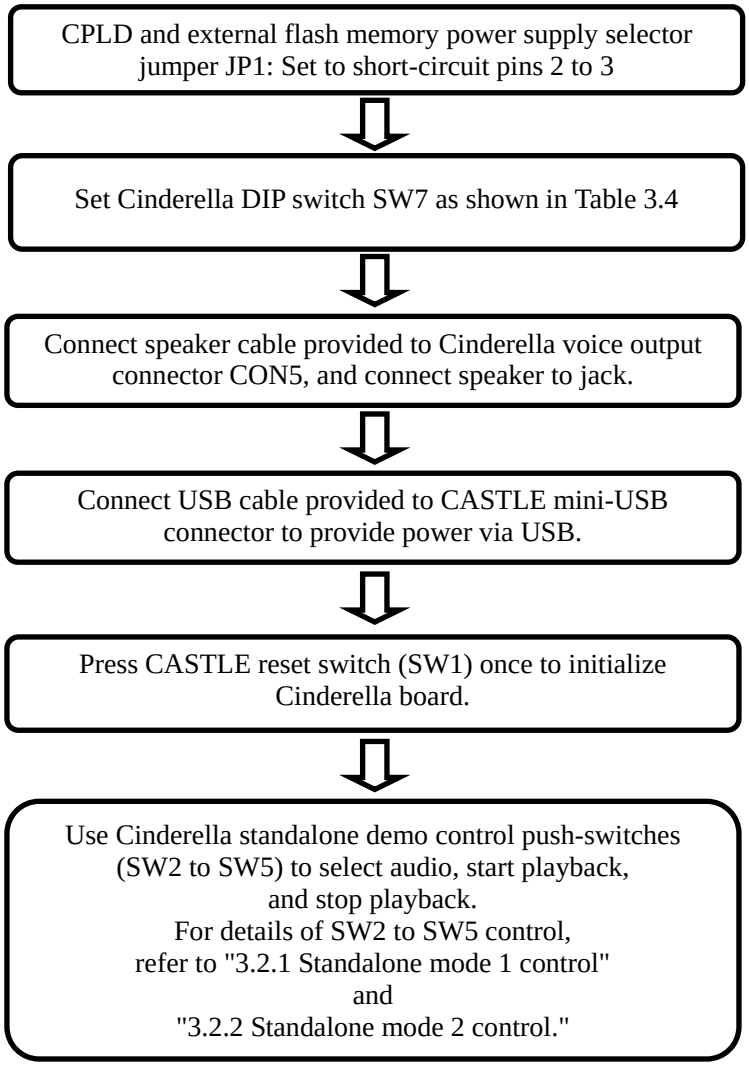

Table 3.4 SW7 settings for Cinderella board standalone demo (1)

SW No.	Function	Description
SW7-1	S1V30080 internal regulator control	Off: Normal operation
SW7-2	Interface mode lower-order bit	Set as shown in Table 3.5 depending on whether ROM data is Standalone 1 or Standalone 2.
SW7-3	Interface mode higher-order bit	
SW7-4	External flash memory access control Selects whether to use data written to the external flash memory or S1V30080 internal ROM data.	Off: External flash memory access On: S1V30080 internal ROM access
SW7-5	External flash memory write protection	On: Protects external flash memory data
SW7-6	Test switch	On: Default

Table 3.5 SW7 settings for Cinderella board standalone demo (2)

SW7-3	SW7-2	Interface mode
OFF	ON	Standalone 1
OFF	OFF	Standalone 2

3.2.1 Standalone mode 1 control

The Cinderella standalone demo control push-switches (SW2 to SW5) are as shown in Table 3.6 for Standalone mode 1.

Table 3.6 Standalone 1 push-switch (SW2 to SW5) functions

Interface	SW2 to 5			
	SW5	SW4	SW3	SW2
Standalone 1	SET_PLAY[3]	SET_PLAY[2]	SET_PLAY[1]	SET_PLAY[0]

The status of push-switches SW2 to SW5 determines the value of S1V30080 standalone 1 SET_PLAY[3:0]. The value is "0" when pressed, and "1" when released. For example, to play back file index number 4, press SW5, SW3, and SW2.

DIP switch SW6 acts as an auxiliary function, allowing the pin corresponding to SET_PLAY[3:0] to be set to "0" while SW6 is set to "On." The correlation between SW6 and SET_PLAY[3:0] is shown in Table 3.7. Push-switches SW2 to SW5 can be used for control when it is off.

Table 3.7 DIP switch (SW6) functions for Standalone 1

	SW6-1	SW6-2	SW6-3	SW6-4
Standalone 1	SET_PLAY[0]	SET_PLAY[1]	SET_PLAY[2]	SET_PLAY[3]

3.2.2 Standalone mode 2 control

The Cinderella standalone demo control push-switches (SW2 to SW5) are as shown in Table 3.8 for Standalone mode 2.

Table 3.8 Standalone 2 push-switch (SW2 to SW5) functions

Interface	SW2 to 5			
	SW5	SW4	SW3	SW2
Standalone 2	START	File index number 0x10 digit	File index number 0x01 digit	STOP

SW3 and SW4 are used to specify the file index number.

SW4 specifies the higher-order digit in hexadecimal, and SW3 specifies the lower-order digit. The file index number is determined by the number of times SW3 and SW4 are pressed. For example, to specify file index number 21 (0x15), press SW4 once and SW3 five times.

SW5 starts playback, and SW2 stops playback.

3.3 Connecting to an external host CPU

Playback is possible using either S1V30080 internal ROM data or ROM data written to the flash memory on the Cinderella board.

Data created as S1V30080 ROM data can be written to the Cinderella board flash memory and emulated by the host CPU.

In this case, the ROM data host interface mode can be "SPI (clock-synchronized serial)," "I2C," "Standalone 1," or "Standalone 2."

The interface mode used by the host CPU must however match the host interface mode (internal ROM host interface mode for internal ROM) set when creating ROM data.

For details of how to create ROM data, refer to the *S1V30080 Series Sound Tool User Guide*.

For details of S1V30080 specifications, refer to the *S1V30080 Series Hardware Specifications* and *S1V30080 Series Message Protocol Specifications*.

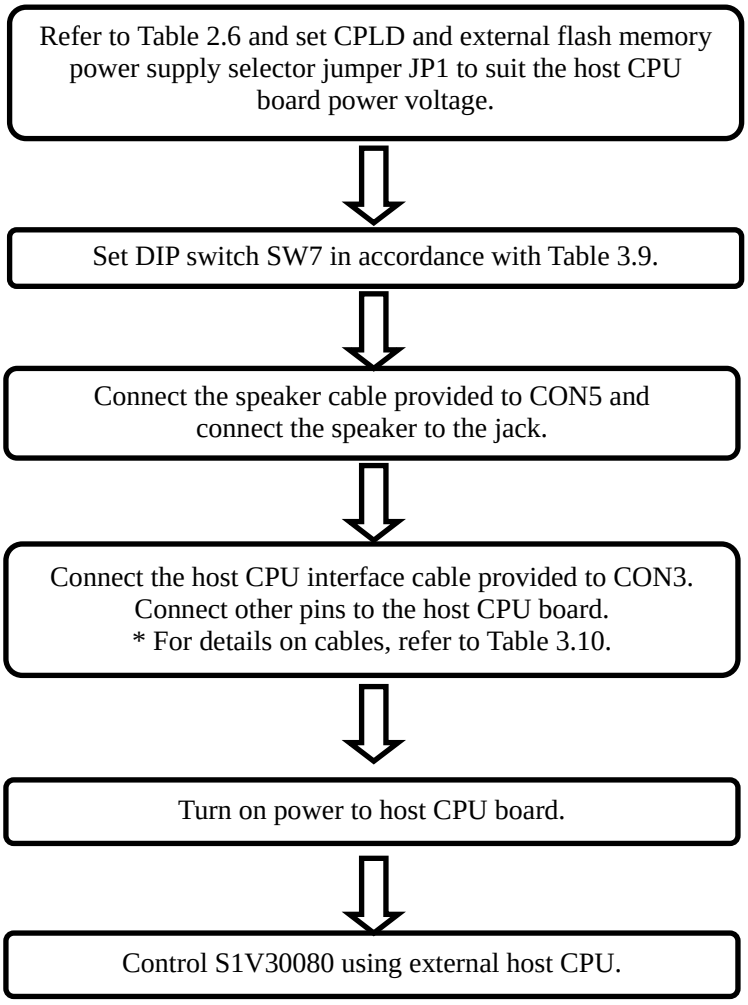

Table 3.9 SW7 settings for connection to external host CPU

SW No.	Function	Description
SW7-1	S1V30080 internal regulator control	Off: Normal operation
SW7-2	Interface mode lower-order bit	ON
SW7-3	Interface mode higher-order bit	ON
SW7-4	External flash memory access control * Selects whether to use data written to the external flash memory or S1V30080 internal ROM data.	Off: External flash memory access On: S1V30080 internal ROM access
SW7-5	External flash memory write protection	On: Protects external flash memory data
SW7-6	Test switch	On: Default

Table 3.10 External host CPU interface cable connection

connector	No.	I/O	Cable color	S1V30080 input/output pin	signal level
CON3	1	P	Brown	VDD (3 to 5.5 V)(*)	-
	2	I	Red	SYSTEM_EN	3.0-5.5 V CMOS
	3	I	Orange	SCKS/SCL /SET_PLAY1	3.0-5.5 V CMOS
	4	I	Yellow	SIS /SDA /SET_PLAY0	3.0-5.5 V CMOS
	5	O	Green	SOS /- /SET_PLAY2	3.0-5.5 V CMOS
	6	O	Blue	MSG_RECEIVE/MSG_RECEIVE/SET_PLAY3	3.0-5.5 V CMOS
	7	O	Purple	SOUND_PLAYING	3.0-5.5 V CMOS
	8	P	Gray	VSS	-

* Power should be supplied from the host CPU board. The power supply voltage must be between 3.0 V and 5.5 V and must match other signal levels.

4. Usage Precautions

4.1 DIP switch definitions

Figures 4.1 and 4.2 show the DIP switch on/off states. ■ indicates the DIP switch position. DIP switches are shorted to GND when on, and so are 0 when on and 1 when off.

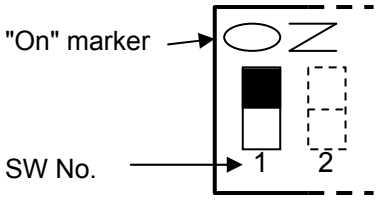

Figure 4.1 DIP switch on (0)

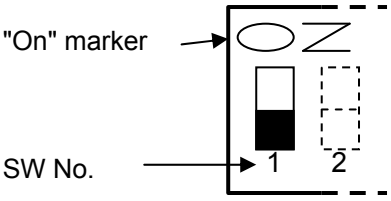

Figure 4.2 DIP switch off (1)

4.2 Voice output pin precautions

The Cinderella voice output (connector CON5) is a differential output due to speaker amplifier IC specifications. Care must be taken to avoid short-circuiting the voice output signal to other signals (especially GND) when connecting devices, as this may damage the speaker amplifier IC.

In particular, avoid connecting devices with power supplies, such as PCs.

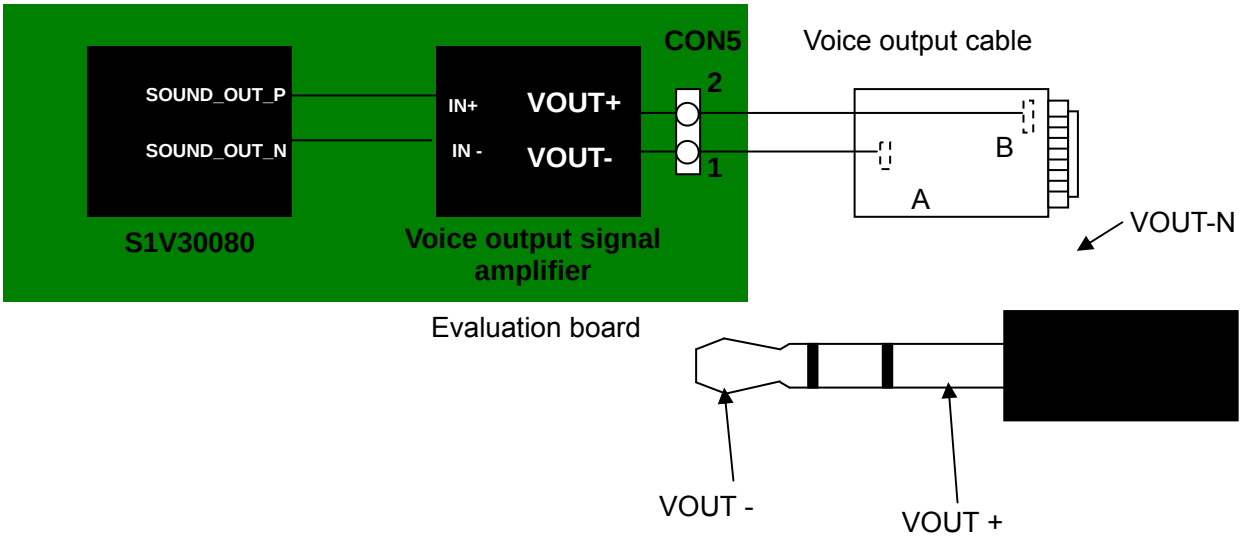

Figure 4.3 Device connection to voice output pin

4.3 External power supply precautions

The Cinderella board allows power supply via the host interface connector CON2, host interface connector CON3, or mini-USB connector CON6, but care must be taken to avoid conflicts between multiple power supplies.

When different power supply voltages are fed through a number of connectors, in particular, there is a risk of damage to the power supply devices or fire due to short circuiting.

4.4 PLD and external flash memory power supply selector jumper pin J6

This must be set as shown in Table 2.6 according to the external power supply voltage. In particular, avoid short-circuiting pins 1 to 2 on JP1 with a 5 V supply, as this will subject the CPLD and external flash memory to a voltage exceeding the specifications, resulting in damage.

4.5 Micro SD card precautions

The micro SD card provided with the evaluation board is pre-formatted. It can be used for storing data without the need to format it beforehand.

If formatting is necessary due to problems writing to the micro SD card, it should be reformatted to FAT16 specifications.

Use of cards other than the micro SD card provided is not covered by the warranty.

5. Board Circuit Diagram

The S1V30080 evaluation kit circuit diagrams are shown below.

HOST I/F 1

VDD
SYSTEM EN
SCKS
SIS
SOS
MSG RECEIVE
SOUND PLAYING
VSS

CON3
IL-Z-8PL-SMTYE
SYSTEM_EN_HOST
SCKS_HOST
SIS_HOST
SOS_HOST
MSG_RCV_HOST
SOUND_PLAYING_HOST
SCKS
SIS
SOS
MSG_RECIEVE
SOUND_PLAYING

HOST I/F 2

VDD
NC
NC
SCLK
SDA
SET PLAY0
SET PLAY1
SET PLAY2
SET PLAY3
MSG RECEIVE
SOUND PLAYING
SYSTEM EN
VSS
VSS
VSS
VSS

CON2
HIF3FC-16PA-2.54DSA
SCLK_HOST
SDA_HOST
SET_PLAY0_HOST
SET_PLAY1_HOST
SET_PLAY2_HOST
SET_PLAY3_HOST
MSG_RCV_HOST
SOUND_PLAYING_HOST
SYSTEM_EN_HOST

RA1 10k
RA2 10k
RA3 10k
RA4 10k
RA6 330
RA7 10k
RA9 330
R4 10k
R13 10k
R14 10k

Y1
KC2520B-C2
16.384MHz
CLK_CPLD
C1 0.01u

U1
SN74LVC8T245
C2 0.1u
C3 0.1u

R1 4.7K
R2 4.7K
R3 4.7K
CON4
Unmounting
XM4C-1031
CPLD_TCK
CPLD_TDO
CPLD_TMS
CPLD_TDI

U2
SN74LVC8T245
C4 0.1u
C5 0.1u
SYSTEM_EN
CE
FLASH_EN

U3
EPM240T100C5
C6 0.1u
C8 0.1u
C10 0.1u
C11 0.1u
C12 0.1u
C13 1u
C14 0.1u
C15 0.1u
C16 0.1u
C17 0.1u
C18 0.1u
GND Sheild
SYSTEM_EN_HOST
SET_PLAY0_HOST
SET_PLAY1_HOST
SET_PLAY2_HOST
SET_PLAY3_HOST
RESET_N
SET_PLAY0_SW
SET_PLAY1_SW
SET_PLAY2_SW
SET_PLAY3_SW
CPLD_TMS
CPLD_TDI
CPLD_TCK
CPLD_TDO
SYSTEM_EN_80
CE_80
FLASH_EN_80
SET_PLAY3_80
SET_PLAY2_80
SET_PLAY1_80
SET_PLAY0_80
IF_SEL1_LS
COM_10
COM_1
CE_SW
IF_SEL0
IF_SEL1
FLASH_EN_SW
FLASH_EN_LS
SEG_A
SEG_B
SEG_C
SEG_D
SEG_E
SEG_F
SEG_G
SEG_DOT

U4
SN74LVC8T245
C7 0.1u
C9 0.1u
MSG_RECIEVE
SOS
SCKS
SIS

Q1
Q2
RN2101

U5
U6
NAR131S

SW1 B3SL-1022P
SW2 B3SL-1022P
SW3 B3SL-1022P
SW4 B3SL-1022P
SW5 B3SL-1022P
RESET N
SET PLAY1
SET PLAY2
SET PLAY3
SET PLAY4

SW6 CHS-04
SET PLAY0
SET PLAY1
SET PLAY2
SET PLAY3

SW7 CHS-06
CE SW
IF SEL0
IF SEL1
FLASH EN
W#
W#
TEST_EN

VOUT5
VOUT33
VDD_OTHER
DGND

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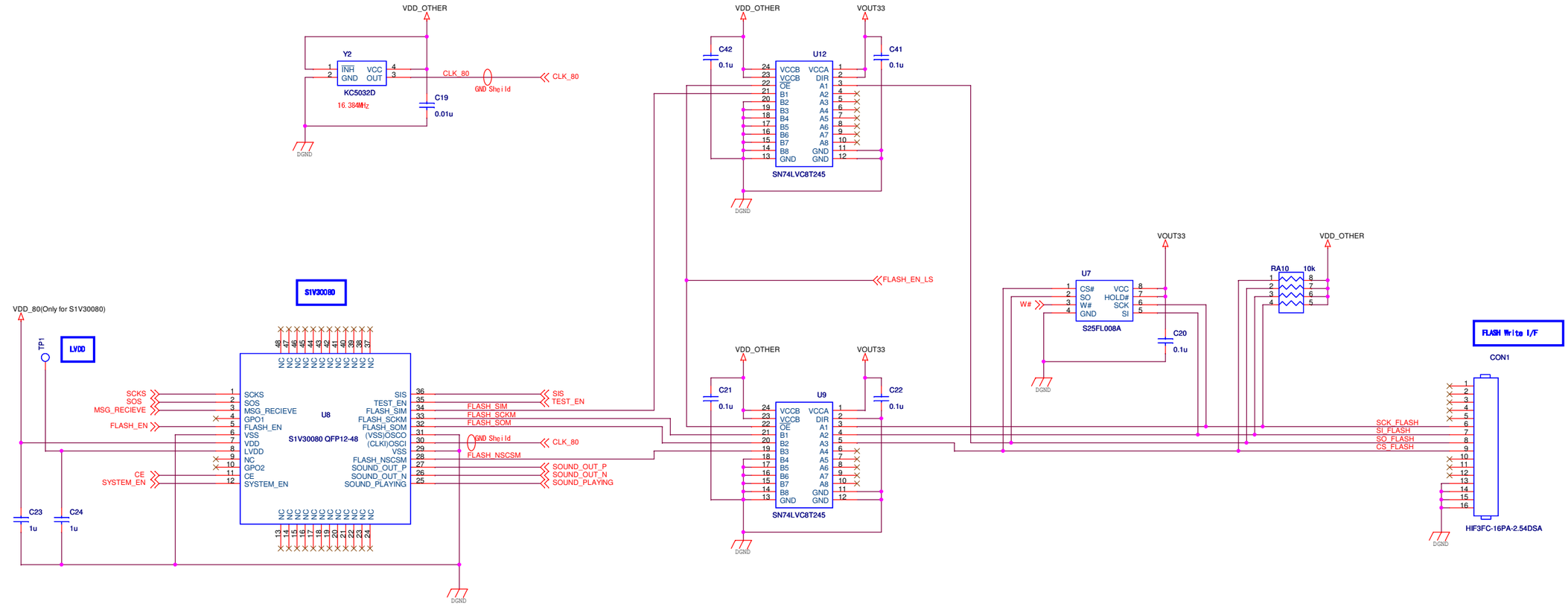
Date: Thursday, November 20, 2008	Sheet 1 of 3		



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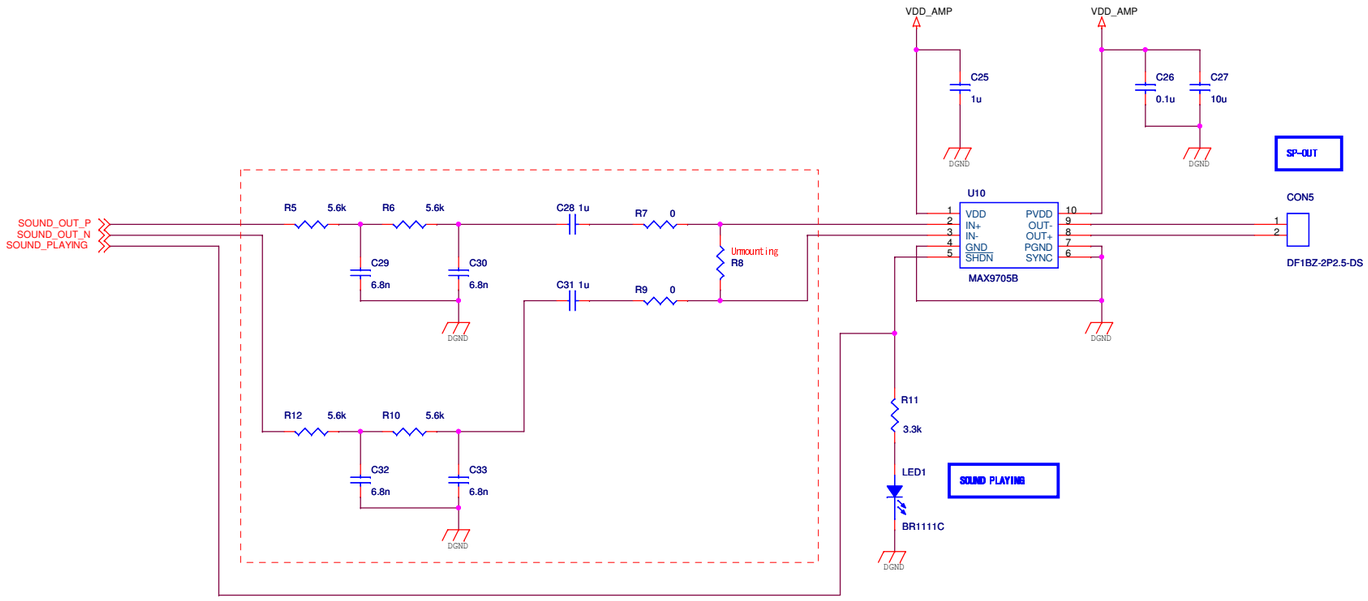

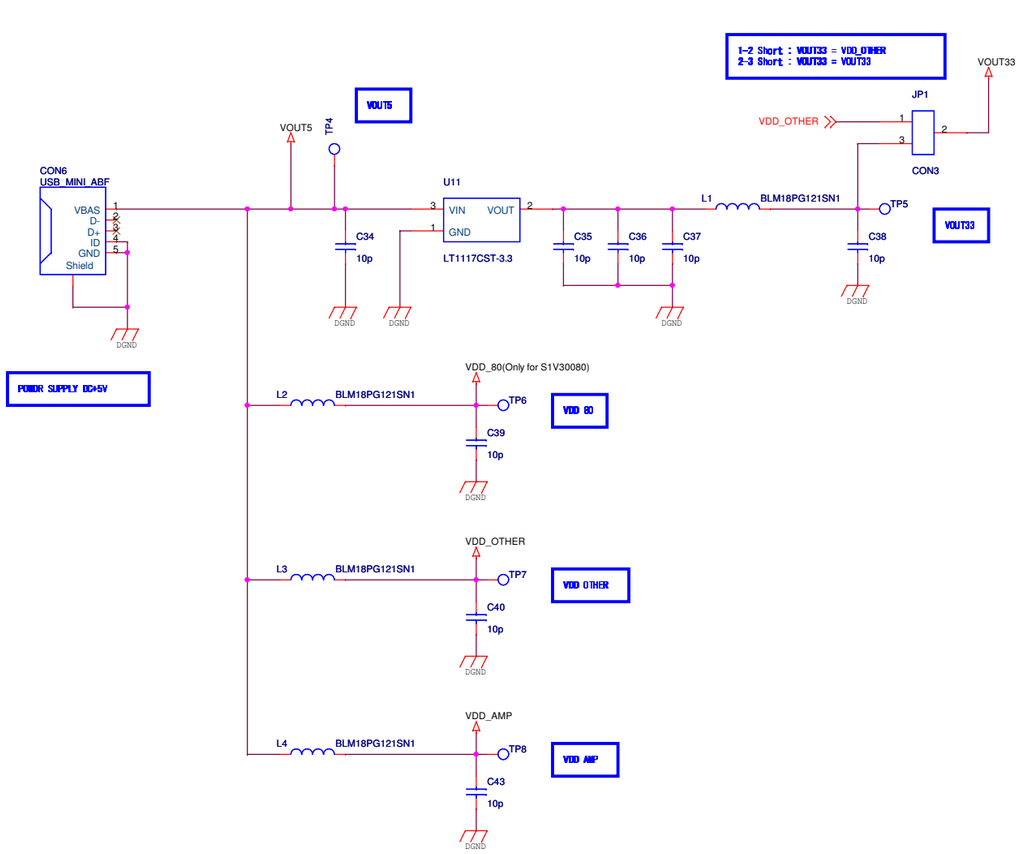

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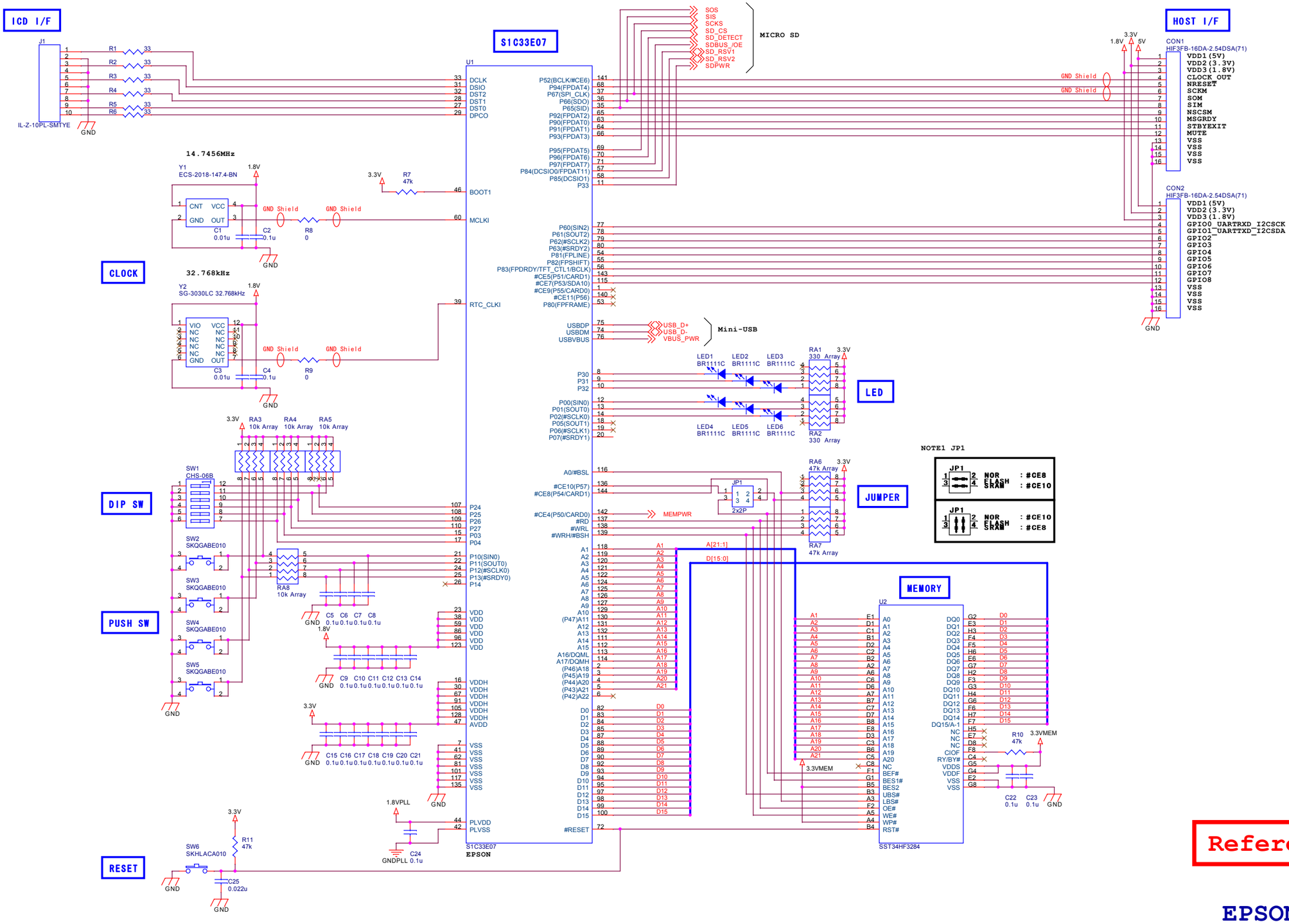
ICD I/F
J1
IL-Z-10PL-SMTYE
R1 33
R2 33
R3 33
R4 33
R5 33
R6 33
GND
S1C33E07
U1
DCLK
DSIO
DST2
DST1
DST0
DPCO
MICRO SD
SOS
SIS
SCKS
SD_CS
SD_DETECT
SDBUS_/OE
SD_RSV1
SD_RSV2
SDPWR
HOST I/F
CON1
HIF3FB-16DA-2.54DSA(71)
VDD1(5V)
VDD2(3.3V)
VDD3(1.8V)
CLOCK_OUT
NRESET
SCKM
SOM
SIM
NSCSM
MSGRDY
STBYEXIT
MUTE
VSS
GND Shield
CON2
HIF3FB-16DA-2.54DSA(71)
GPIO0_UARTRXD_I2CSCK
GPIO1_UARTTXD_I2CSDA
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
CLOCK
Y1
ECS-2018-147.4-BN
14.7456MHz
CNT VCC
GND OUT
C1 0.01u
C2 0.1u
R8 0
R7 47k
BOOT1
MCLKI
Y2
SG-3030LC 32.768kHz
32.768kHz
VIO VCC
NC NC
GND OUT
C3 0.01u
C4 0.1u
R9 0
RTC_CLKI
Mini-USB
USB_D+
USB_D-
VBUS_PWR
USBDP
USBDM
USBVBUS
LED
LED1 BR1111C
LED2 BR1111C
LED3 BR1111C
LED4 BR1111C
LED5 BR1111C
LED6 BR1111C
RA1 330 Array
RA2 330 Array
DIP SW
SW1
CHS-06B
RA3 10k Array
RA4 10k Array
RA5 10k Array
PUSH SW
SW2 SKQGABE010
SW3 SKQGABE010
SW4 SKQGABE010
SW5 SKQGABE010
RA8 10k Array
C5 C6 C7 C8 0.1u 0.1u 0.1u 0.1u
C9 C10 C11 C12 C13 C14 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u
C15 C16 C17 C18 C19 C20 C21 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u
JUMPER
NOTE1 JP1
JP1
NOR FLASH : #CE8
SRAM : #CE10
NOR FLASH : #CE10
SRAM : #CE8
RA6 47k Array
RA7 47k Array
MEMPWR
MEMORY
U2
SST34HF3284
A[21:1]
D[15:0]
3.3VMEM
R10 47k
C22 0.1u
C23 0.1u
RESET
SW6 SKHLACA010
R11 47k
C25 0.022u
C24 GNDPLL 0.1u
1.8VPLL
S1C33E07
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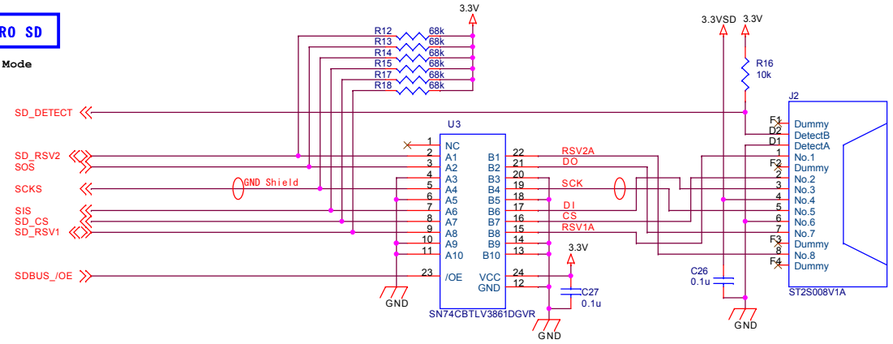
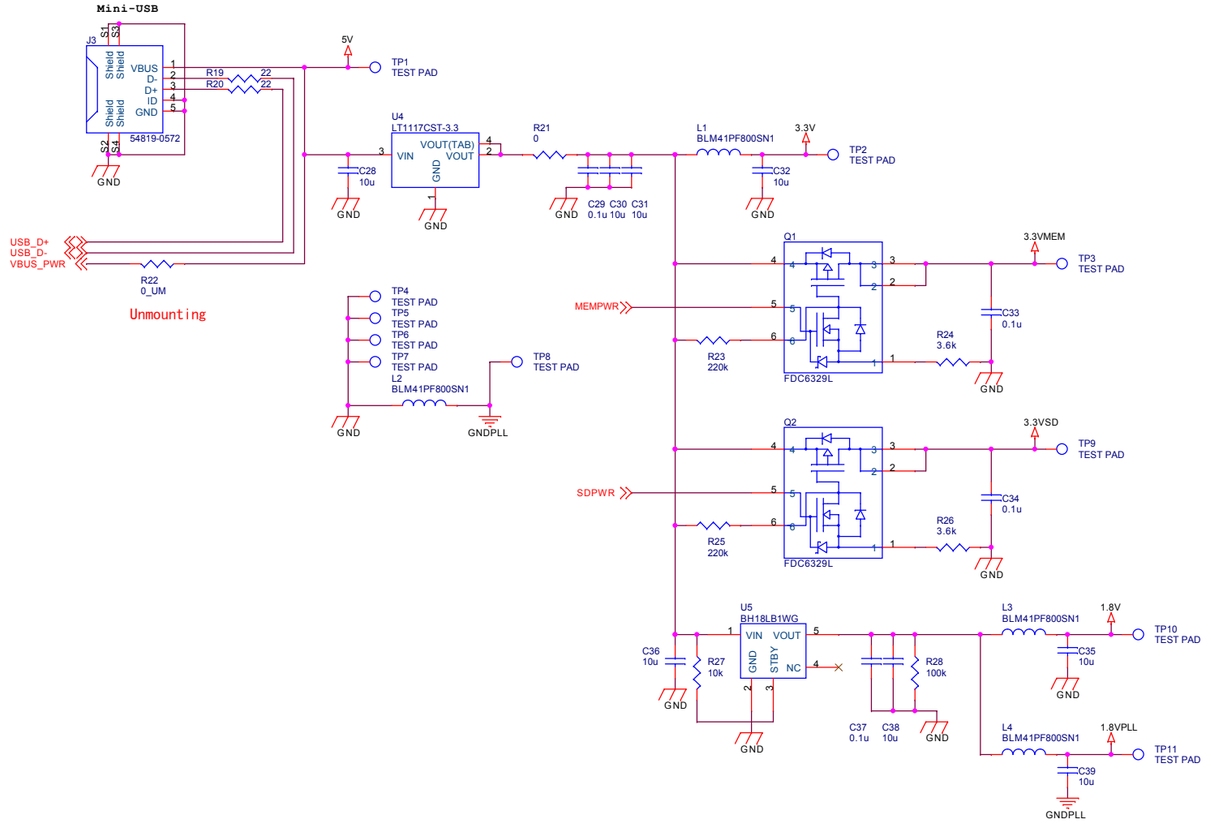
MICRO SD

SPI Mode



POWER SUPPLY (DC5V)

Mini-USB



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EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway,
San Jose, CA 95131, USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, Hi-Tech Bldg., 900 Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road,
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong,
Youngdeungpo-Ku, Seoul 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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