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S1V30120 Evaluation Board (FIRECREST) User Guide

SEIKO EPSON CORPORATION

Rev.2.0

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1. Introduction

1.1 Scope

FIRECREST is the customer evaluation board for the S1V30120 Speech Synthesis IC.

The FIRECREST board provides the necessary clocking, power, configuration and interfaces to allow evaluation of the S1V30120. It is designed to be used as a daughterboard to the S1V30100 Evaluation Board Nightingale, which provides a USB interface to a PC.

This user manual describes the FIRECREST board in detail.

1.2 Document Structure

The User Guide is structured as follows. Section 2 gives an overview of the FIRECREST board and the major components and interfaces. Section 3 describes the board configuration options available on FIRECREST. Section 4 describes each system component and interface in detail.

2. System Overview

FIRECREST provides the required clocks, power, configuration and interface connectors to allow evaluation of the S1V30120 Silicon.

This section gives an overview of the main blocks and interfaces in the system. Section 2.1 provides an overview of the major blocks on the FIRECREST board. Section 2.2 summarizes the main interfaces on FIRECREST.

2.1 System Block Diagram

Figure 1 is a block diagram of the FIRECREST board that illustrates the main system components. The clocking and system configuration options are also shown on the left-side of the figure. FIRECREST implements a number of amplifier circuits for converting the S1V30120 headphone output to a speaker output. Consult the BOM that is delivered with the evaluation kit for details of the fitted components

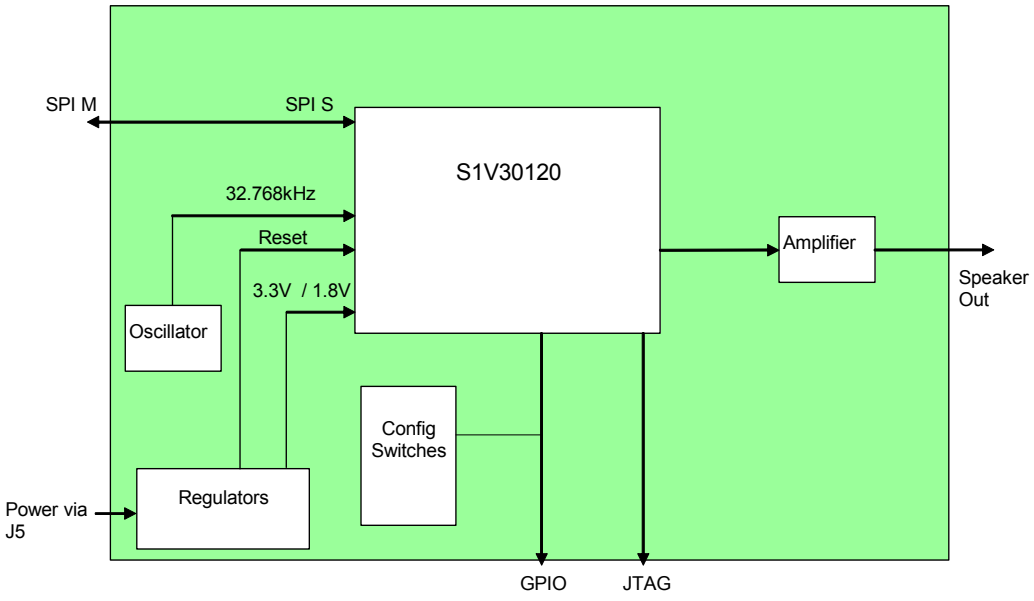


Figure 1 FIRECREST Block Diagram

2.2 System Interfaces

FIRECREST has a large number of connectors to support all the interfaces available on the S1V30120. These are summarized below in Table 1. A full description of these interfaces can be found in Section 4.

Table 1 Interface Connector Summary

Interface	Connector	Notes
Motherboard Interface	J5	Power / Reset / Control Lines
SPI Slave	J4	SPI Slave
GPIO A	J1	GPIO
JTAG	J2	JTAG interface
Dummy NC	J6	Dummy connector used for stability in stacking the board with the S1V30100
Speaker Out	J3	Speaker Out Jack

3. Configuration Options

FIRECREST has a number of configuration options. Some options are selected using configuration switches on the board.

3.1 Configuration Switches

FIRECREST has a DIP switch (SW5) for controlling configuration options. The table below describes the function of each of this configuration switch, together with its default position.

Table 2 FIRECREST Configuration Switch Summary

Switch	Position	Default	Description
SW5-1[GPIOA0]	Open		Reserved
	Closed	***	Enter S1V30120 Bootstrap Downloader on Reset.
SW5-2[GPIOA1]	Open		GPIOA2:A1 select bootstrap option. Defined values are: 0x00: Reserved 0x01: Boot from SPI interface (slave mode) 0x02: Reserved 0X03: Reserved
	Closed	***	
SW5-3[GPIOA2]	Open	***	
	Closed		
SW5-4	Open	***	GPIOA3: Reserved
	Closed		
SW5-5	Open	***	GPIOA5: Reserved
	Closed		
SW5-6	Open		UNUSED
	Closed	***	

4. Detailed Interface Descriptions

4.1 Power Supply

FIRECREST receives power from the J5 Connector when connected to the NIGHTINGALE board. Two yellow LEDs are fitted which indicate whether power is being supplied to the 3.3V and 1.8V – these are marked as 3.3V (LED1) and 1.8V (LED2) respectively on the board.

4.2 Clocks

FIRECREST requires only a single external clock of 32.768kHz for operation. The clock oscillator Y1 on the board supplies this signal.

4.3 Reset

Switch SW7 allows the FIRECREST board to be reset. The reset is commoned with SYS_RESET on the NIGHTINGALE board.

4.4 SPI Interfaces

The S1V30120 has a single SPI Slave Interface. Table 3 shows the pin-out of the SPI Test Connector. The SPI Slave Interface uses the signals SIN, SOUT, SCLK, SFRM1 for serial data in, serial data out, serial clock, and slave select respectively.

The SPI test-connectors uses a 6-pin AMP MicroMatch Test connector.

Table 3 SPI Slave Test Connector

J4 – SPI Slave	
Pin	***SPI S Signal***
1	GND
2	SOUT
3	SCLK
4	SIN
5	SFRM1
6	GND

4.5 GPIO Buttons

The S1V30120 firmware uses two GPIOs to communicate information to/from the host processor to control STANDBY mode and indicate the availability of a message to be received from the S1V30120. These can be controlled/observed on the FIRECREST board as shown in Table 4.

Table 4 GPIO Button Functions

Name	GPIO Port	Description
SW1	Port A Bit 9	
SW2	Port A Bit 8	
SW3	Port A Bit 7	
SW4	Port A Bit 6	
SW6	Port A Bit 4	STANDBY_EXIT
SW8	Port A Bit 10	
SW9	Port A Bit 11	

All the GPIO Port A signals of S1V30120 can be accessed via the 10-pin AMP MicroMatch test connector (J1). Connector J1 is given below in Table 5.

Table 5 GPIO Connector Mapping

J1 – GPIO PORT A	
Pin	***GPIO A Signal***
1	GND
2	GPIOA5
3	GPIOA6
4	GPIOA7
5	GPIOA8
6	GPIOA9
7	GPIOA10
8	GPIOA11
9	SFRM2
10	GND

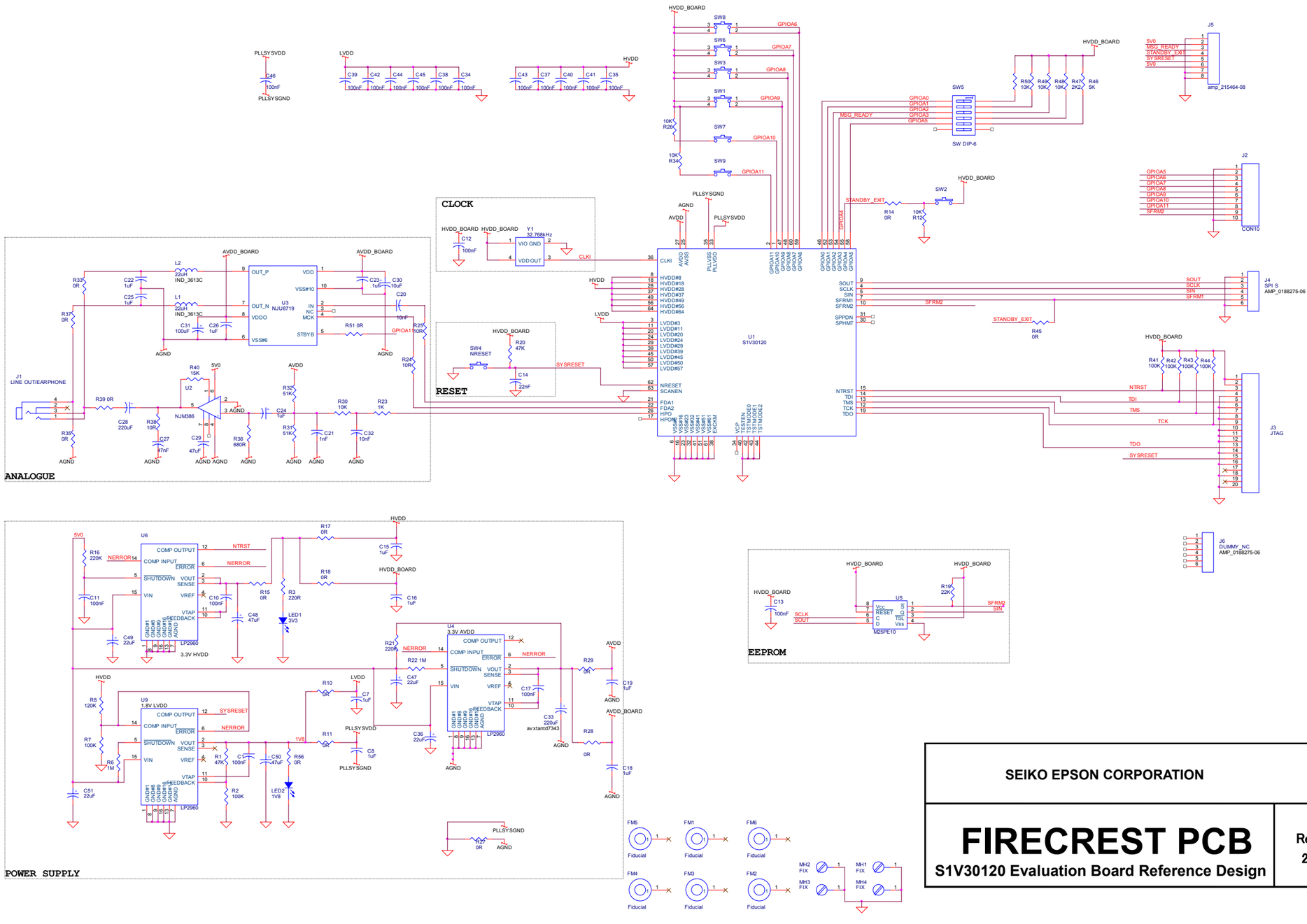
4.6 JTAG

The JTAG Interface provides access to the ARM Processor on the S1V30120.

Table 6 shows the pin-out of the JTAG connector. This is the standard pin-out used for connection to the ARM Multi-ICE unit.

Table 6 JTAG Connector Pin-out

J2– JTAG Connector	
Pin	***Signal***
1	HVDD
2	HVDD
3	NTRST
4	GND
5	TDI
6	GND
7	TMS
8	GND
9	TCK
10	GND
11	GND
12	GND
13	TDO
14	GND
15	SYSRESET
16	GND
17	NC
18	GND
19	NC
20	GND



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