

**S1V30333/300/120**  
**Evaluation Board**  
**User Guide**

## NOTICE

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# Table of Contents

<b>1. Introduction</b> .....	<b>1</b>
1.1 Overview.....	1
1.2 User Guide Overview .....	1
1.3 Items Included with the Evaluation Board.....	1
1.4 Evaluation Board Product Codes.....	1
<b>2. Function Overview</b> .....	<b>2</b>
2.1 Evaluation Board Layout Diagram .....	2
2.2 System Interface.....	4
2.3 Board Connection.....	4
<b>3. Detailed Description of Functions</b> .....	<b>7</b>
3.1 Power Supply .....	7
3.2 Clocks.....	7
3.3 Reset .....	8
3.4 SPI interface .....	8
3.5 DIP Switch Functions and Settings.....	9
3.5.1 DIP Switch On/Off Definitions.....	9
3.5.2 Audio IC Selection and Mode Setup.....	9
3.5.3 Multi-function Selection .....	10
3.5.4 General Switches .....	10
3.5.5 Audio IC GPIO Settings.....	10
3.5.6 Audio IC S1V30333 Settings.....	11
3.6 Jumper Pin Functions and Settings .....	12
3.6.1 External Memory Settings .....	12
3.6.2 Level Shifter Settings.....	12
3.6.3 Audio Output Jack Precautions .....	12
<b>4. Evaluation Board Exterior View (For reference)</b> .....	<b>13</b>

## 1. Introduction

### 1.1 Overview

This evaluation board is a client evaluation board designed for use with S1V30333/300/120 audio ICs (hereafter simply “audio ICs”).

The evaluation board includes the clocks, power supply, DIP switches, amplifier, and PC USB interfaces needed to evaluate audio ICs. Designed to enable easy evaluation by providing power and data via a PC USB interface, each evaluation board allows evaluations of up to three different types of audio IC.

This User Guide describes the evaluation board in detail.

### 1.2 User Guide Overview

This User Guide is arranged as follows. Section 2 outlines the functions of the evaluation board, its main components, and interfaces. Section 3 describes the evaluation board functions in greater detail.

### 1.3 Items Included with the Evaluation Board

The following items are included in the evaluation board set.

- (1) Evaluation board      x1
- (2) SPI interface cable    x2
- (3) USB cable              x1

### 1.4 Evaluation Board Product Codes

The audio ICs mounted vary depending on the product code.

- (1) Product code: S5U1V30333A2200  
Audio IC: S1V30333
- (2) Product code: S5U1V30333C0100  
Audio ICs: S1V30120, S1V30300, S1V30333
- (3) Product code: S5U1V30333C2100  
Audio ICs: S1V30120, S1V30333

Please note that peripheral circuits are provided only for the audio IC(s) listed under each product code, and not for all those mentioned or illustrated in this document.

## 2. Function Overview

## 2. Function Overview

The evaluation board includes the clocks, power supply, DIP switches, amplifier, and interfaces needed to evaluate audio ICs. This section gives a brief overview of the main components and interfaces. Section 2.1 describes the evaluation board's main blocks; Section 2.2 describes the board's main interfaces.

### 2.1 Evaluation Board Layout Diagram

Fig. 2-1 is a schematic diagram of the evaluation board showing the main system components.

Fig. 2-1 shows the layout for product code S5U1V30333C0100 with all components mounted.

Depending on the actual product code, some components may not be mounted.

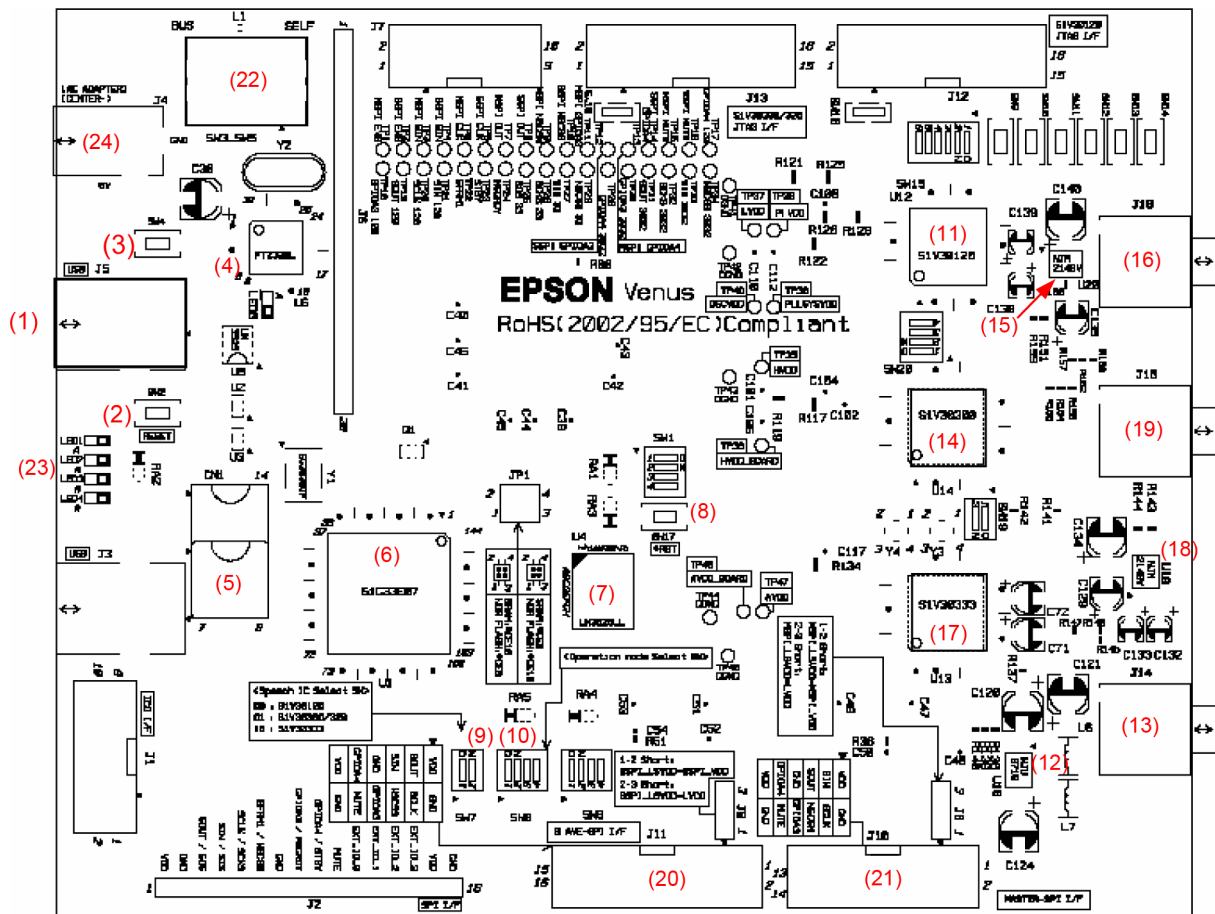


Fig. 2-1 Evaluation board layout diagram

<Main component names>

Listed below are the names of the main components illustrated in Fig. 2-1.

- (1) PC USB interface connector
- (2) Main hard reset switch
- (3) FT232BL IC reset switch
- (4) FT232BL USB-UART conversion IC
- (5) System clock crystal oscillator
- (6) S1C33E07 32-bit RISC controller
- (7) Flash/PSRAM multi-chip memory
- (8) Audio IC reset switch
- (9) Audio IC select switch
- (10) Interface mode selector switch
- (11) S1V30120 audio IC
- (12) S1V30120 audio output signal amplifier
- (13) S1V30120 audio output jack
- (14) S1V30300 audio IC
- (15) S1V30300 audio output signal amplifier
- (16) S1V30300 audio output jack
- (17) S1V30333 audio IC
- (18) S1V30333 audio output signal amplifier
- (19) S1V30333 audio output jack
- (20) Slave SPI interface
- (21) Master SPI interface
- (22) Input power supply selector switch
- (23) LED indicators (LED1 to LED4)
- (24) AC adapter mounting area

## 2. Function Overview

### 2.2 System Interface

The evaluation board includes a large number of connectors that support different interfaces to allow compatibility with a wide range of setups evaluated by clients. Table 2-1 lists these interfaces. Section 3 lists details of the interfaces.

**Table 2-1 Interface/connector list**

Interface	Connector	Function
PC USB interface	J5	Power/data control line
SPI master	J10	SPI master interface
SPI slave	J11	SPI slave interface
Speaker out	J14,J15,J16	Speaker out jack

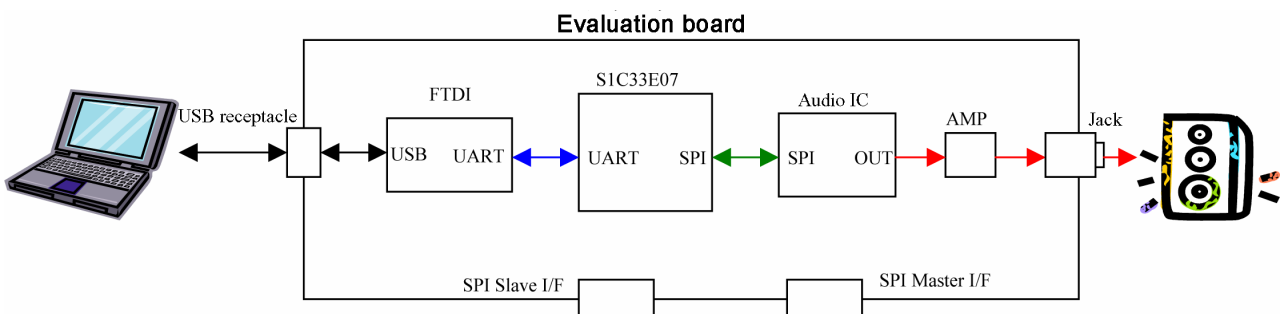
### 2.3 Board Connection

The evaluation board can be connected in three different ways, as shown in the figures below.

- (1) Fig. 2-2: Allows audio data generated using the audio generation tool to be played back and checked on the audio IC.
- (2) Fig. 2-3: Allows development and debugging using the client’s host CPU.
- (3) Fig. 2-4: Allows operation checking and debugging of the audio IC board developed by the client.
- (3) Fig. 2-5: ROM with a built-in audio IC can be emulated by connecting the optional ROM emulator.

For details, refer to the *S1V3033X ROM Emulator Hardware User Guide*.

For evaluations based on the configurations shown in Figures 3 and 4, fit a connector to suit the client’s board to the “open” end of the cable provided. Clients using the board while connected to an external host (Fig. 2-3) or an evaluation board host (Fig. 2-4) should contact Seiko Epson for detailed specifics.



**Fig. 2-2 PC host connection diagram**

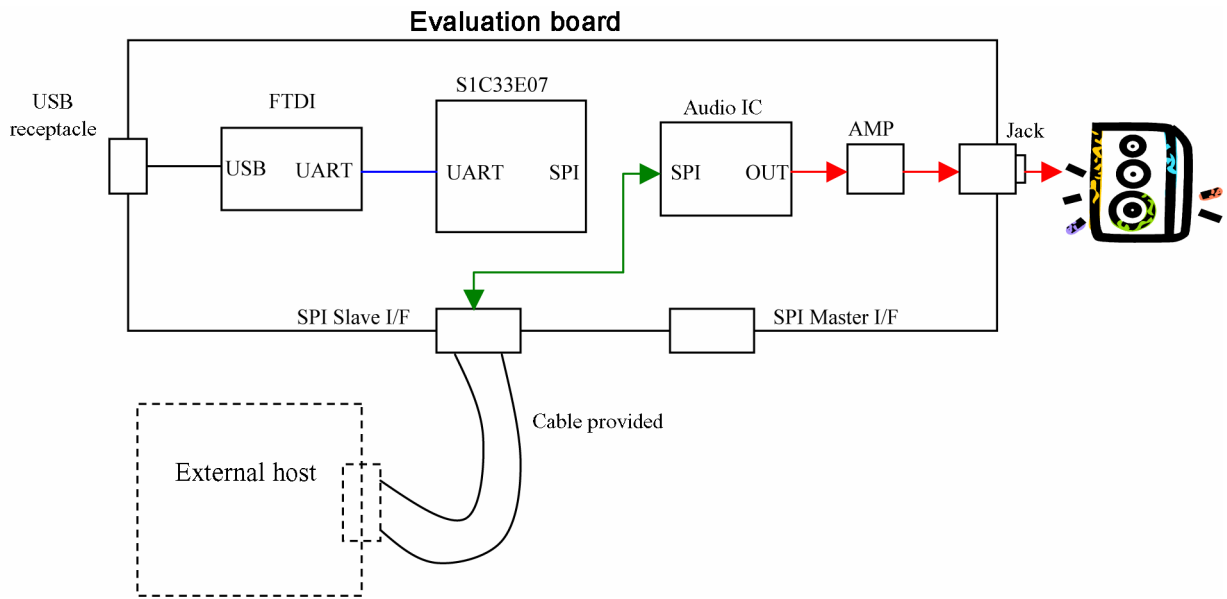


Fig. 2-3 External host connection diagram

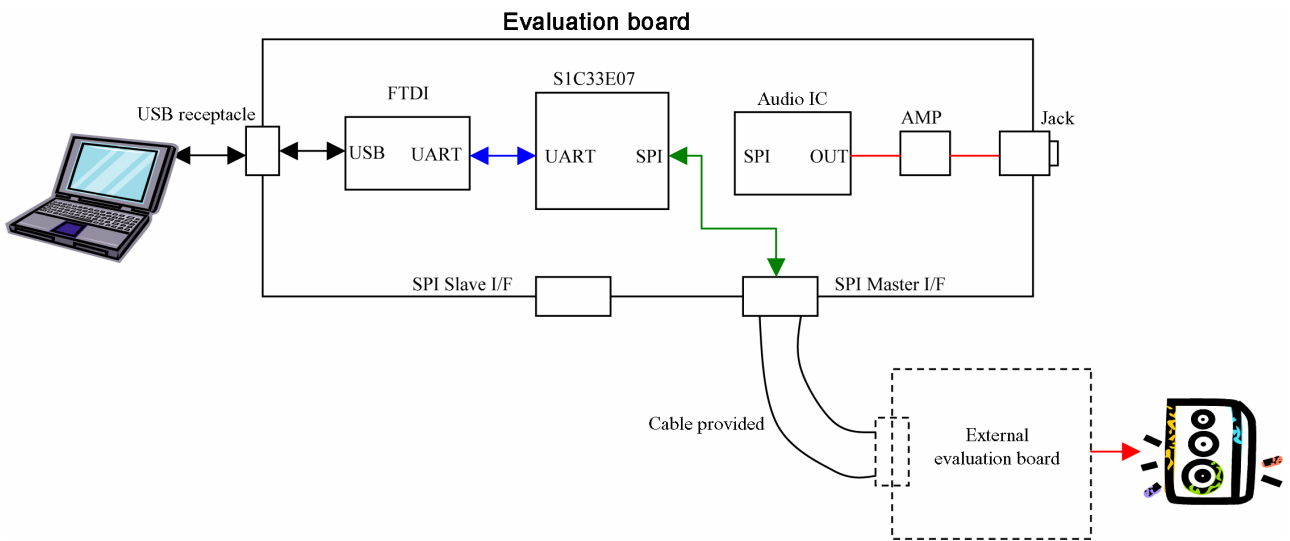


Fig. 2-4 Evaluation board host connection diagram



## 2. Function Overview

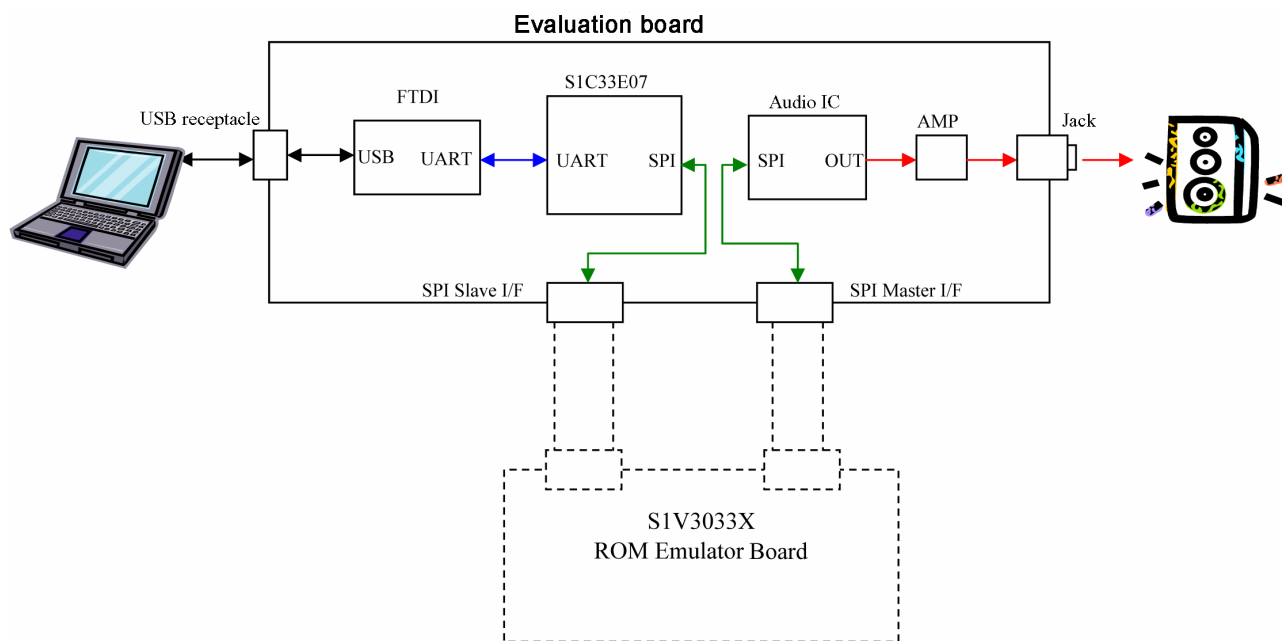


Fig. 2-5 ROM Emulator connection diagram

## 3. Detailed Description of Functions

### 3.1 Power Supply

The evaluation board generates 3.3 V and 1.8 V power supplies via a regulator from the single 5 V DC power supply received from the J5 PC USB interface connector. Space is also provided for an optional AC adapter (CENTER -, minimum rated output 1 A, DC jack external diameter 5.5 mm, internal diameter 2.1 mm). When using both the USB and AC adapter power supplies, select one of the two using the SW3 power supply selector switch designed to prevent shorting between the two power supply inputs. See Table 3-1.

LED4 indicates whether the power supply is on or off, illuminating when the power supply is on and going out when the power supply is off. See Table 3-2.

**Table 3-1 Power supply selection**

SW3 setting	Power supply	Remarks
BUS	USB power supply	Default
SELF	AC adapter power supply	Component: CLIFF FC68148 or equivalent

**Table 3-2 LED4 power supply switching**

Power supply on/off	LED4 state	Remarks
ON	Illuminated	
OFF	Off	

### 3.2 Clocks

Table 3-3 lists the different IC clocks used on the evaluation board.

**Table 3-3 Clocks**

Frequency	Use
12.288MHz	S1V30333 clock
32.768kHz	S1V30300 clock
	S1V30120 clock
	S1C33E07 RTC clock
14.7456MHz	S1C33E07 system clock

### 3. Detailed Description of Functions

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#### 3.3 Reset

Table 3-4 shows the different reset switch types and their uses. Reset switches SW4 and SW2 must always be pressed in that sequence immediately after turning on the power supply.

**Table 3-4 Reset switches**

Reset switch	Power supply
SW2	Main hard reset
SW4	FT232BL IC reset
SW17	Audio IC reset

※ SW2 resets the S1C33E07 and audio IC.

#### 3.4 SPI interface

The evaluation board includes an SPI master interface and SPI slave interface connectors. Tables 3-5 and 3-6 show the pin layout for the SPI interface connectors.

The side sending the clock (SCLK) is defined as the master. The receiving side is defined as the slave.

**Table 3-5 SPI master connectors (Code: Omron XG4M-1430-U MIL; standard product)**

J10 – SPI I / F MASTER					
Pin No.	I/O	Signal	Pin No.	I/O	Signal
1	I	VDD	2	I	GND
3	I	SIN	4	O	SCLK
5	O	SOUT	6	O	NSCSM
7	I	GND	8	I	GPIOA3/MGRDY
9	O	GPIOA4/STBY	10	O	MUTE
11	O	RSTM	12	I	GND
13	–	NC	14	–	NC

**Table 3-6 SPI slave connectors (Code: Omron XG4M-1430-U MIL; standard product)**

J11 – SPI I / F SLAVE					
Pin No.	I/O	Signal	Pin No.	I/O	Signal
1	I	VDD	2	I	GND
3	O	SOUT	4	I	SCLK
5	I	SIN	6	I	NSCSS
7	I	GND	8	O	GPIOA3/MGRDY
9	I	GPIOA4/STBY	10	I	MUTE
11	I	RSTS	12	I	GND
13	–	NC	14	–	NC
15	–	NC	16	–	NC

## 3.5 DIP Switch Functions and Settings

### 3.5.1 DIP Switch On/Off Definitions

Fig. 3-1 and 3-2 show the different DIP switch on/off states. The black section indicates the DIP switch position.

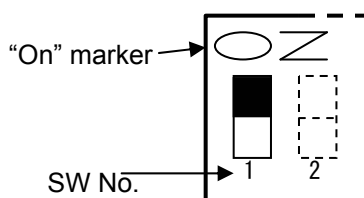


Fig. 3-1 DIP switch on

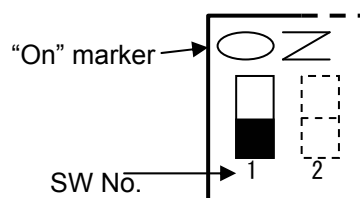


Fig. 3-2 DIP switch off

### 3.5.2 Audio IC Selection and Mode Setup

Use SW7 to select one of three different audio ICs connected. LED1 to LED3 illuminate as shown in Table 3-7 to indicate which audio IC is currently selected.

Similarly, SW8 can be used to select the configuration, as described in 2.3. Table 3-8 shows the corresponding switch positions.

The SW2 main hard reset switch must be pressed in all cases if the DIP switch settings below are changed.

Table 3-7 Audio IC selector switches and LED1 to LED3 states

Setting (binary)	SW7		LED			Description
	1	2	1	2	3	
00	OFF	OFF	On	Off	Off	S1V30120
01	ON	OFF	Off	On	Off	S1V30300
10	OFF	ON	On	On	Off	S1V30333

Table 3-8 Mode selector switch

Setting (binary)	SW8				Description
	1	2	3	4	
0000	OFF	OFF	OFF	OFF	PC host
0011	ON	ON	OFF	OFF	ROM emulation

※ Please contact Seiko Epson if used with an external host or evaluation board host.

### 3. Detailed Description of Functions

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#### 3.5.3 Multi-function Selection

Confirm that SW6 is set to the defaults, as shown in Table 3-9 below.

**Table 3-9 Multi-function selector switch**

SW6	Description	Setting
SW6-1	Audio IC I/F selection	OFF
SW6-2	UART selection	OFF
SW6-3	Mode register setting	OFF
SW6-4	Reset selection	OFF

#### 3.5.4 General Switches

SW1 is a general switch and is not currently used. Check that the switch is set to the defaults as shown in Table 3-10 below.

**Table 3-10 General switches**

SW1	Description	Setting
SW1-1	–	OFF
SW1-2	–	OFF
SW1-3	–	OFF
SW1-4	–	OFF

#### 3.5.5 Audio IC GPIO Settings

Table 3-11 shows the default settings for the S1V30120 GPIO setting DIP switch SW15.  
Table 3-12 shows the default settings for the S1V30300 GPIO setting DIP switch SW20.

**Table 3-11 S1V30120 GPIO settings**

SW15	Description	Setting
SW15-1	GPIOA0	ON
SW15-2	GPIOA1	ON
SW15-3	GPIOA2	OFF
SW15-4	GPIOA3	OFF
SW15-5	GPIOA5	OFF
SW15-6	–	OFF

**Table 3-12 S1V30300 GPIO settings**

<b>SW20</b>	<b>Description</b>	<b>Setting</b>
SW20-1	GPIOA0	ON
SW20-2	GPIOA1	ON
SW20-3	GPIOA2	OFF
SW20-4	GPIOA3	OFF

#### **3.5.6 Audio IC S1V30333 Settings**

Table 3-13 shows the default settings for the S1V30333 oscillator clock selector DIP switch SW19.

**Table 3-13 S1V30333 oscillator clock settings**

<b>SW19</b>	<b>Description</b>	<b>Setting</b>
SW19-1	–	OFF
SW19-2	Oscillator clock selection	OFF

### 3. Detailed Description of Functions

#### 3.6 Jumper Pin Functions and Settings

##### 3.6.1 External Memory Settings

Confirm that JP1 is set to the defaults, as shown in Table 3-14 below.

**Table 3-14 JP1 settings**

JP1 setting	Remarks
1 to 3pin Short, 2 to 4pin Short	Default

##### 3.6.2 Level Shifter Settings

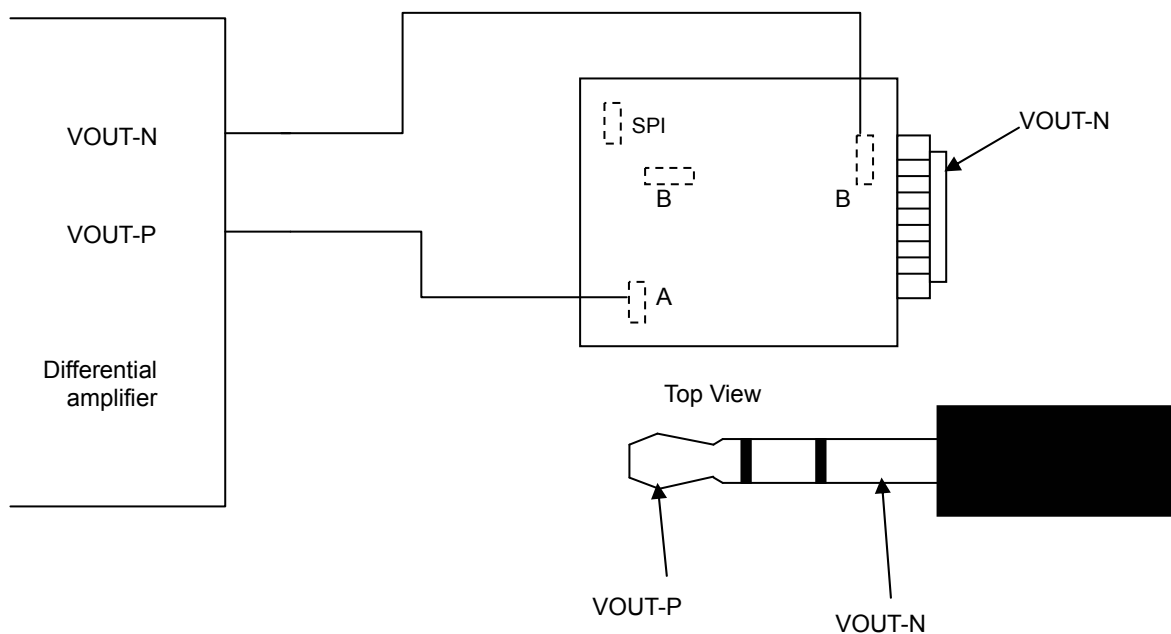
JP8 and JP9 should be set as shown in Table 3-14 when evaluating with an external host (Fig. 2-3) or evaluation board host connected (Fig. 2-4), depending on whether the power supply and signal level are both 3.3 V for the external board and evaluation board or whether they differ and are between 3.3 V and 5.5 V.

**Table 3-15 J8 and J9 settings**

Power supply/Signal level	J8/J9 settings
Both power supplies: 3.3 V	1 to 2pin Short
Different power supplies: between 3.3 V and 5.5 V	2 to 3pin Short

##### 3.6.3 Audio Output Jack Precautions

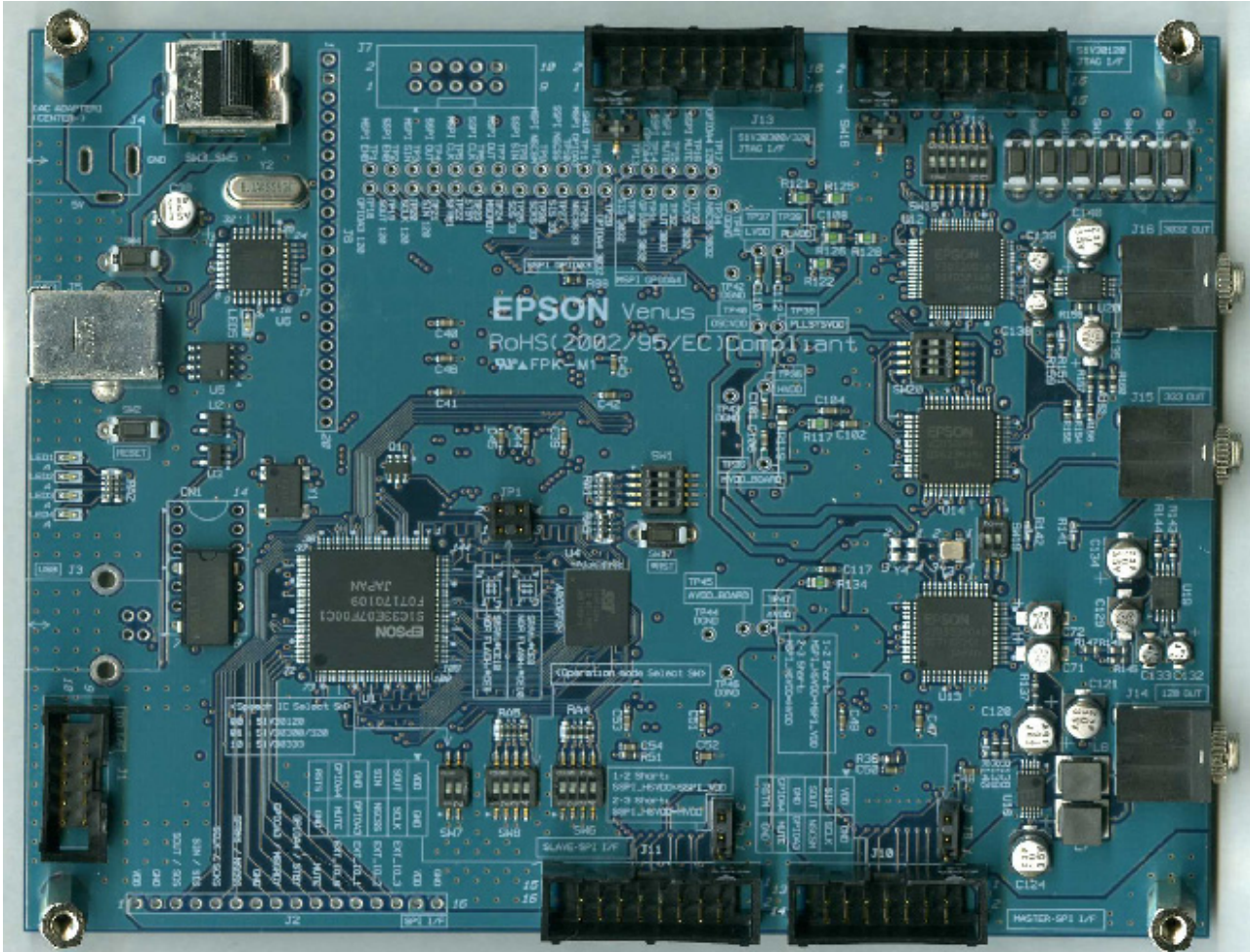
Audio output jacks J14, J15, and J16 are connected to the differential amplifier output signal. Care must be taken when connecting devices, as short-circuiting to GND or other signals will damage the amplifier.



## 4. Evaluation Board Exterior View (For reference)

### 4. Evaluation Board Exterior View (For reference)

As reference, the photo below is an external view of the evaluation board shown in Fig. 2-1.



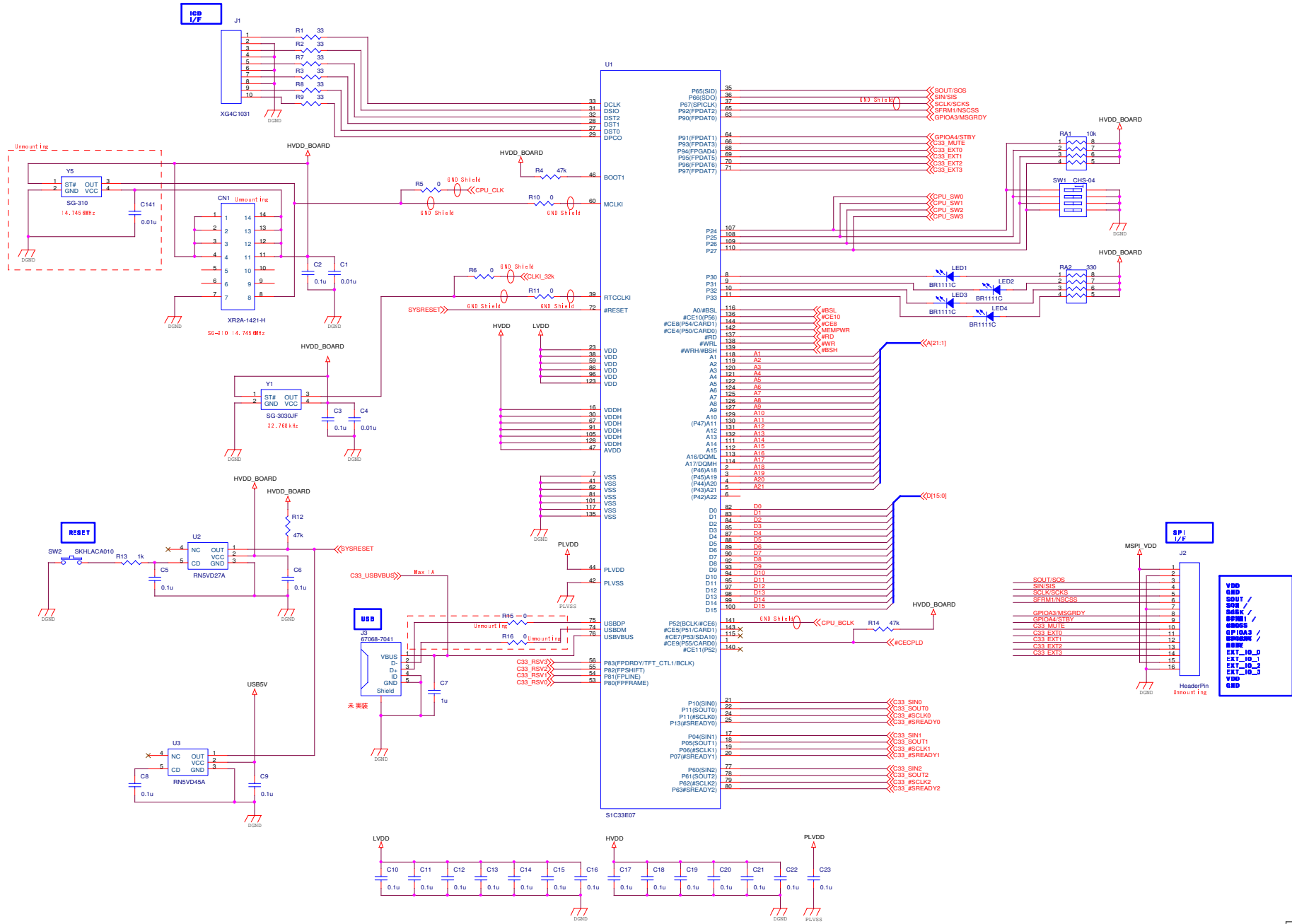


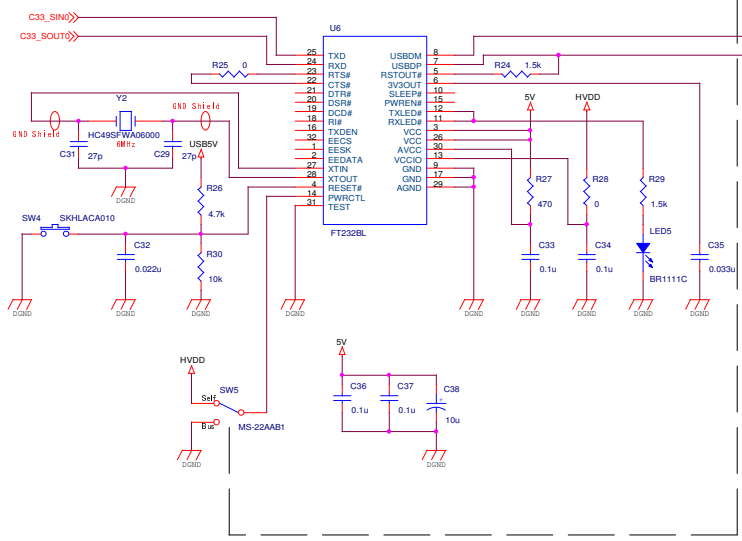
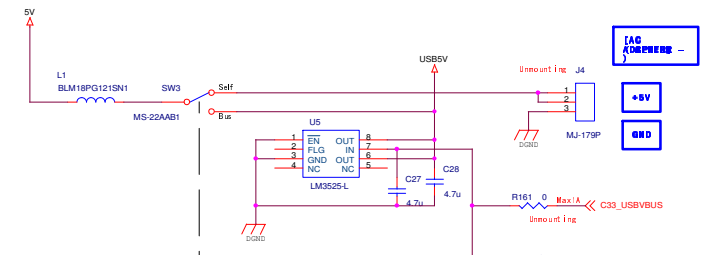
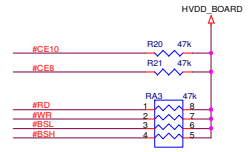
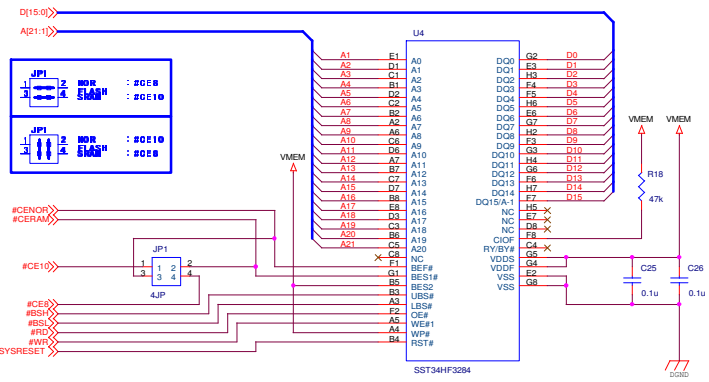
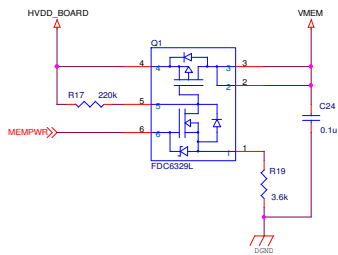
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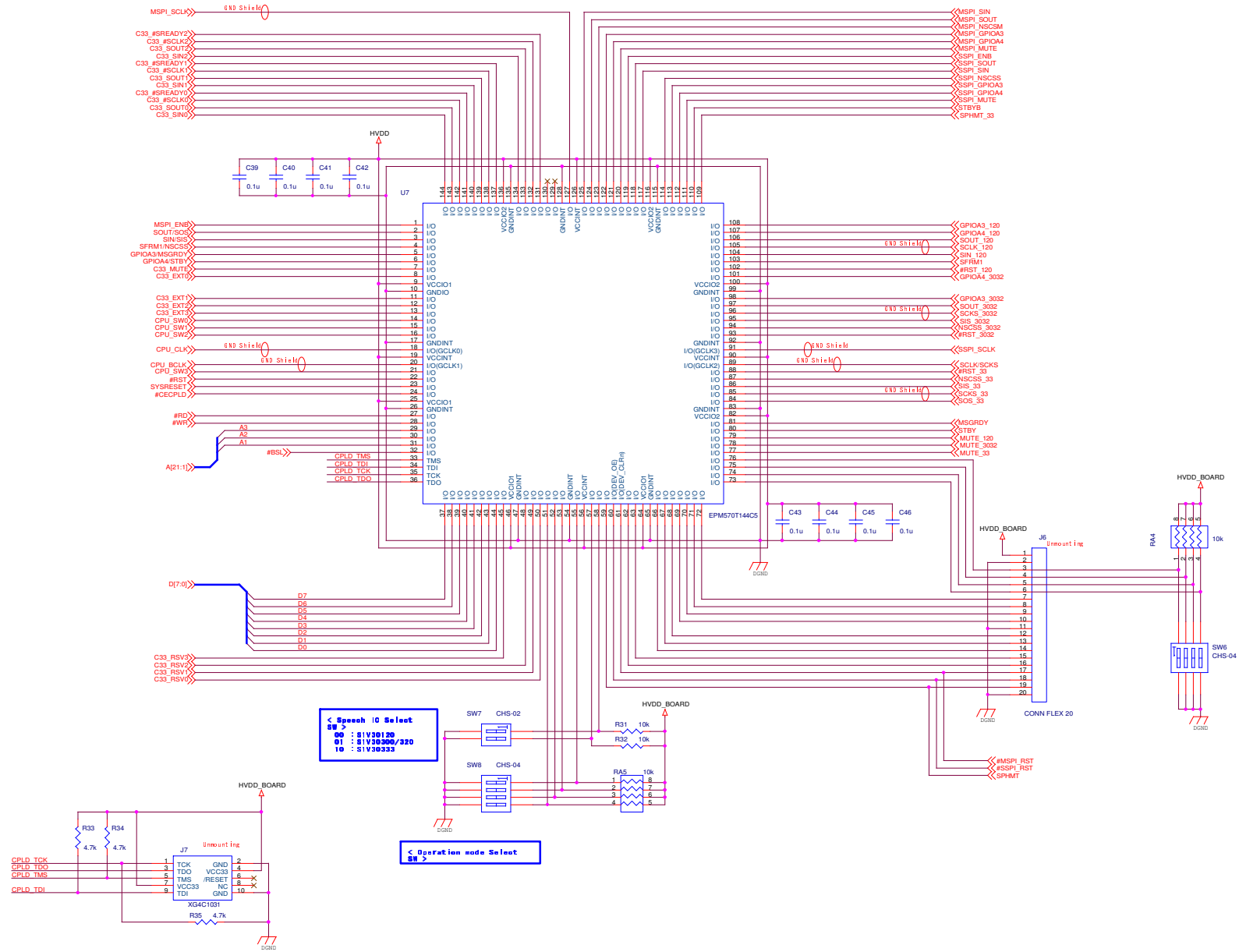
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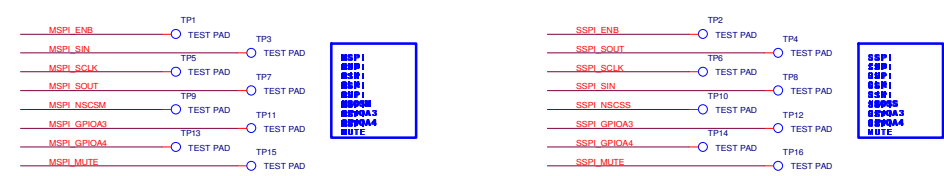
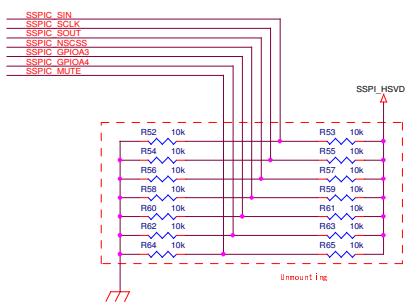
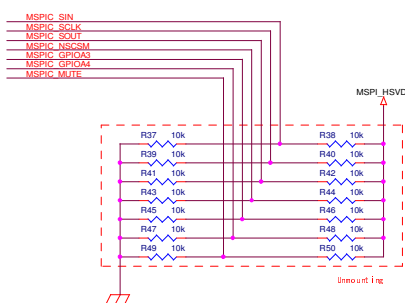
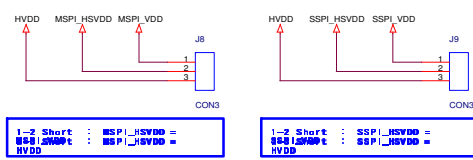
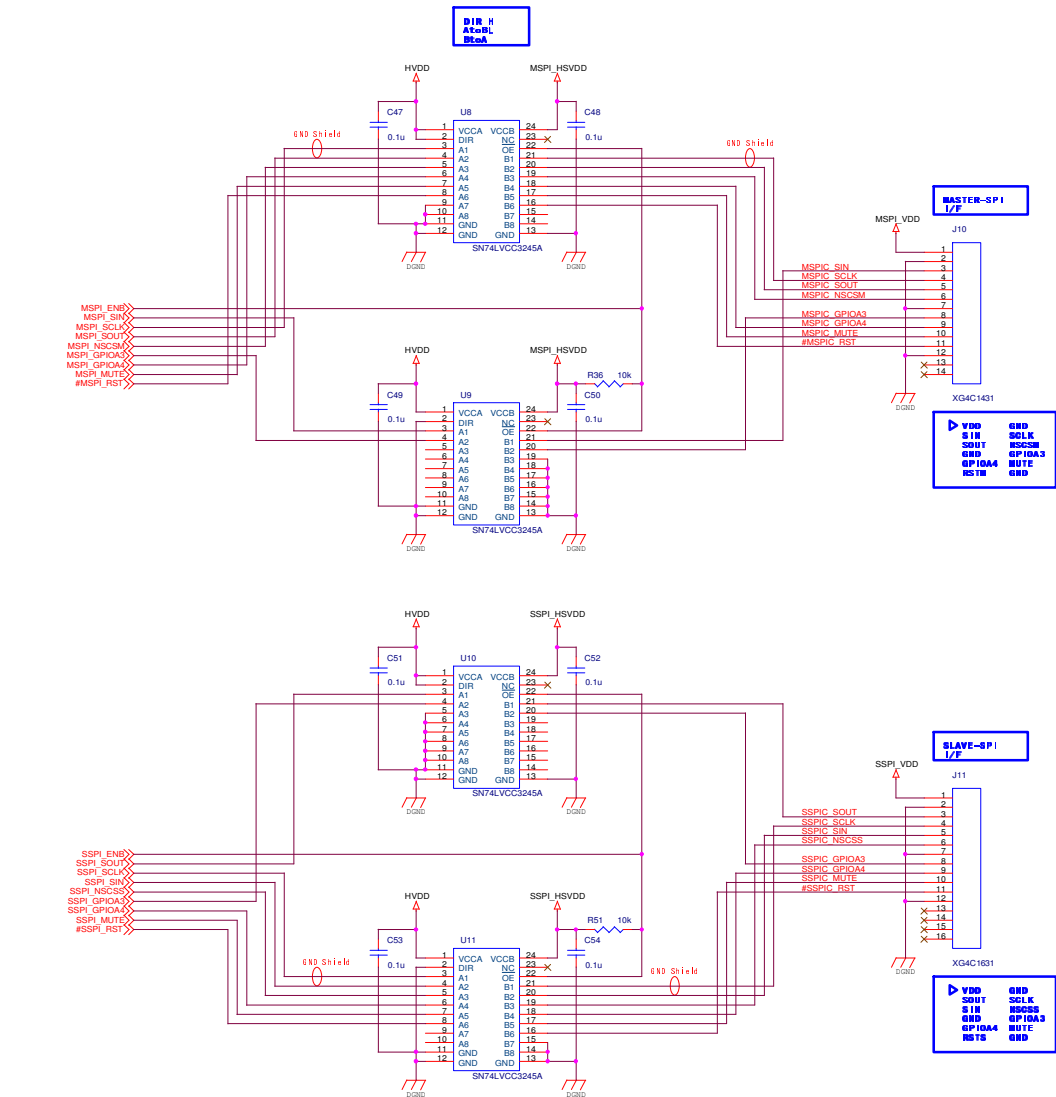
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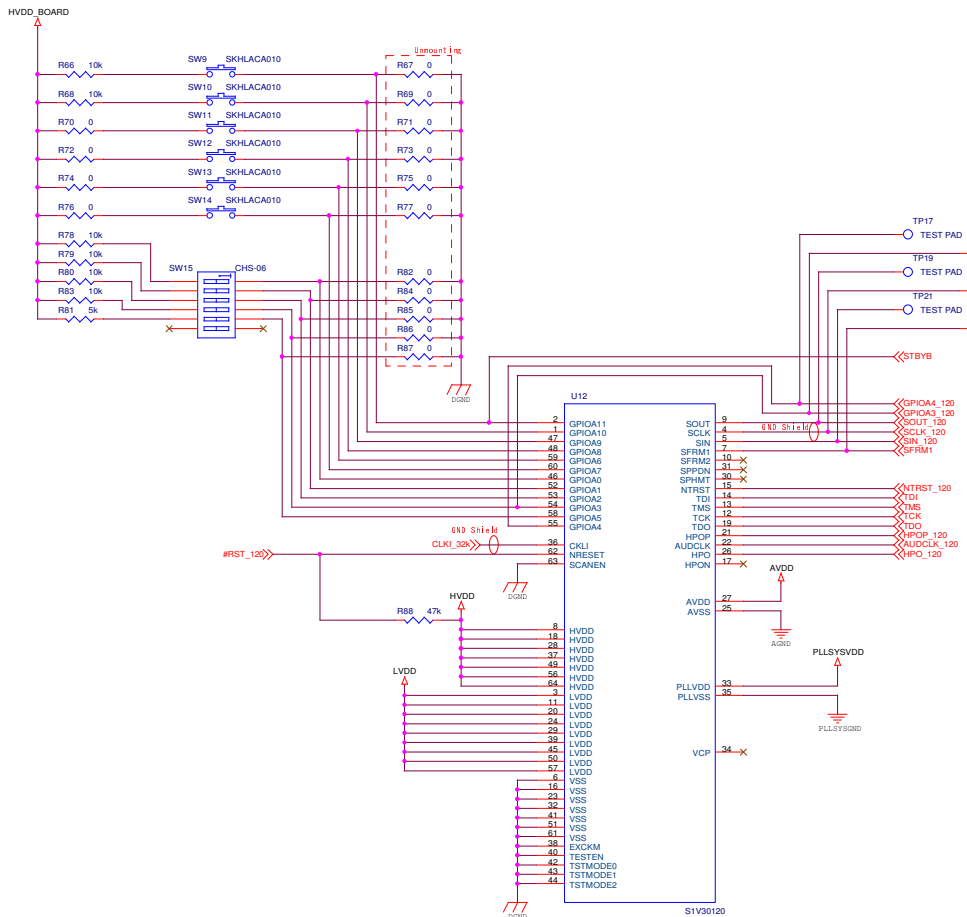
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	Rev.	Page	Type	Details
08/31/2007	1.00	All	New	Newly established
09/21/2007	1.01	All	Correct	Corrected details for Sections 1, 1.2, 2.1, 2.3, 3.1, 3.4, 3.6.2, and 4. Added Section 1.3. Updated photo in section 4.
12/05/2007	1.02	12	Add	Added Section 3.6.3.
13/05/2007	1.03	9	Correct	Table 3-7



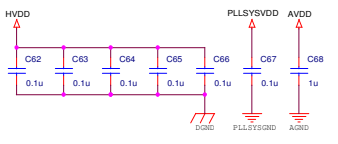
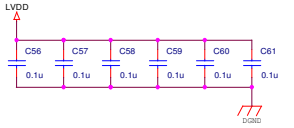
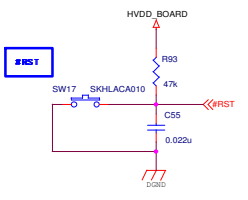
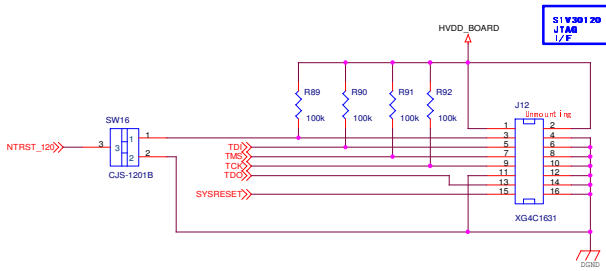


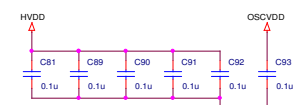
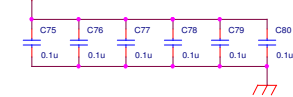
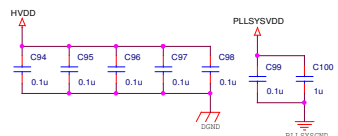
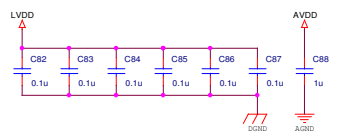
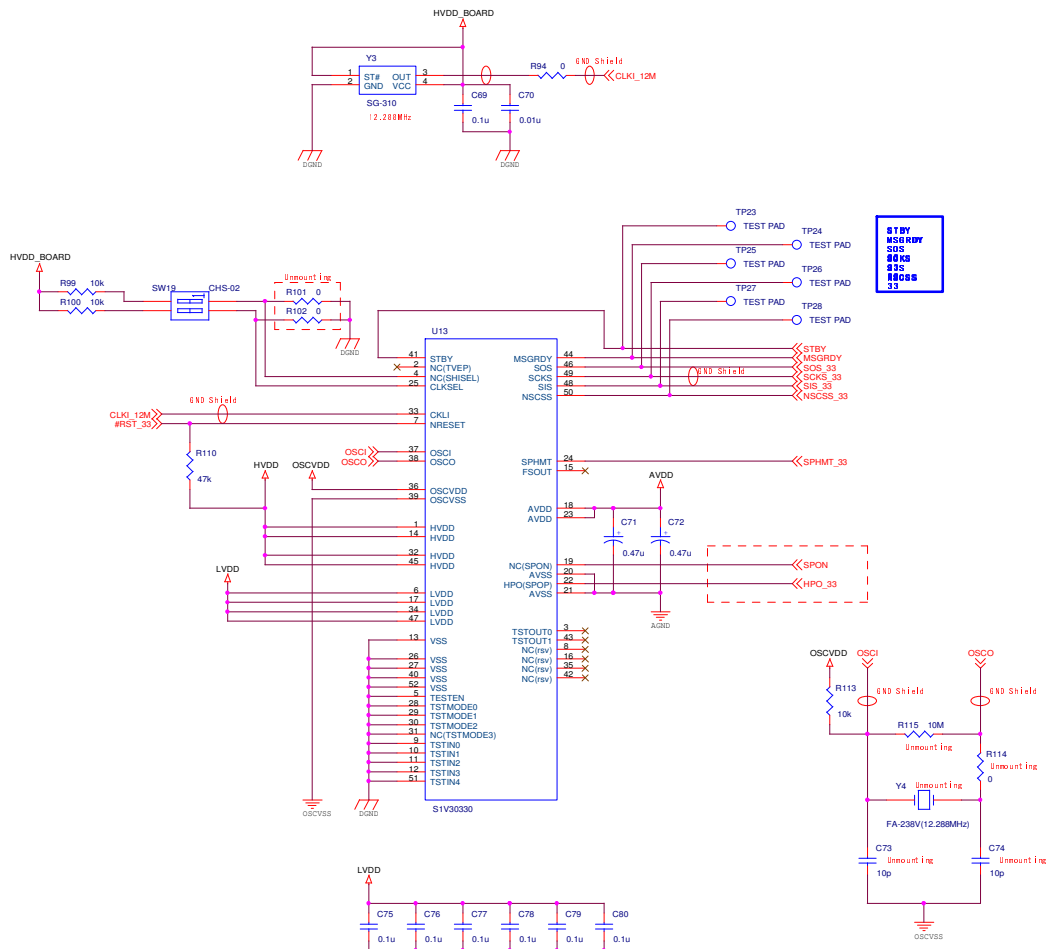
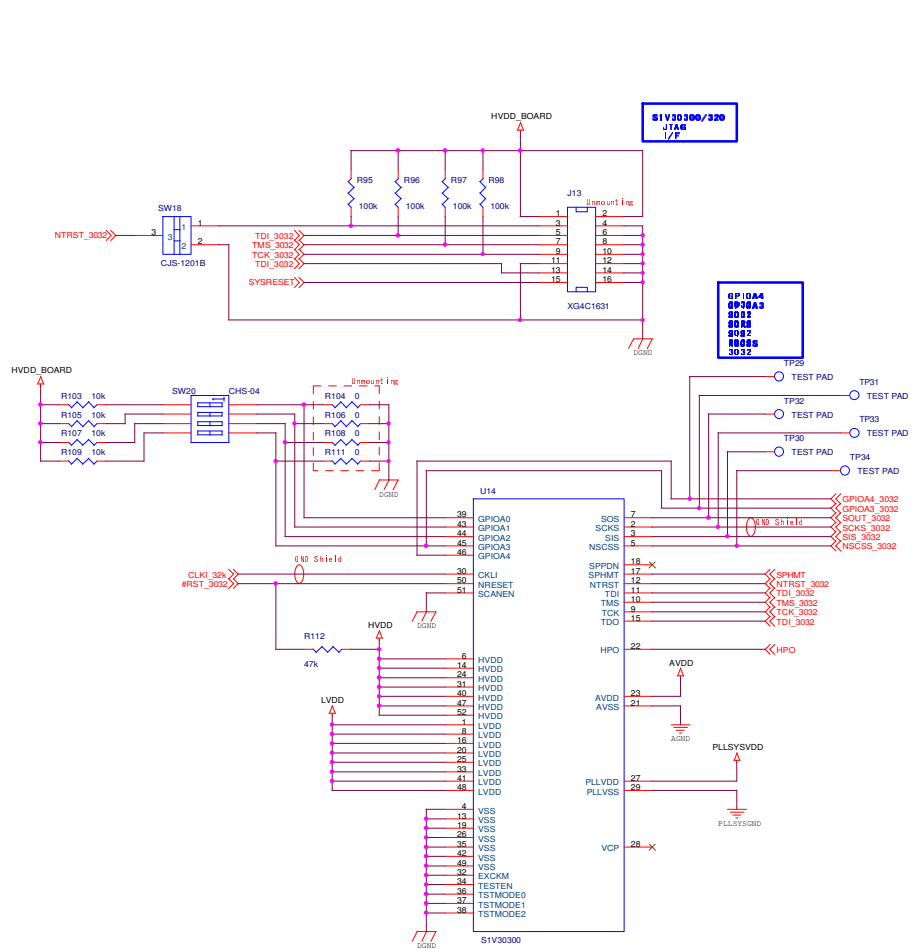


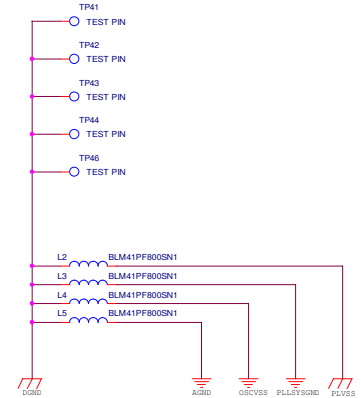
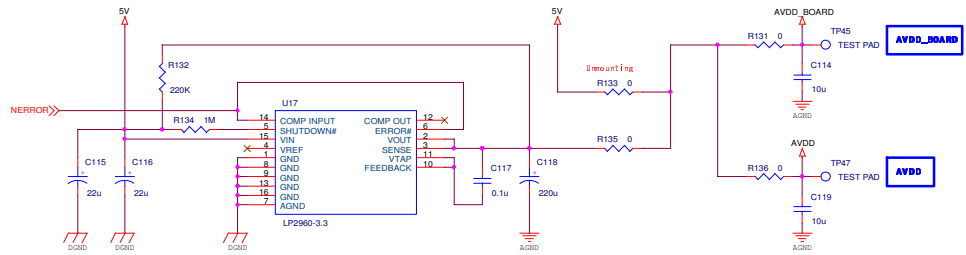
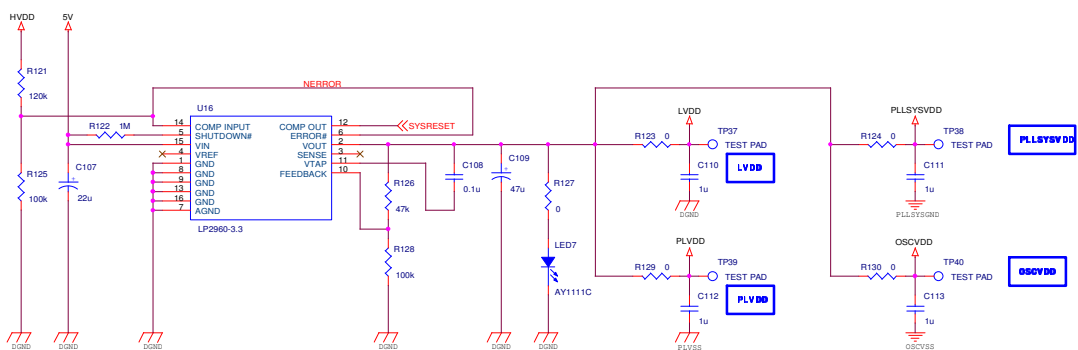
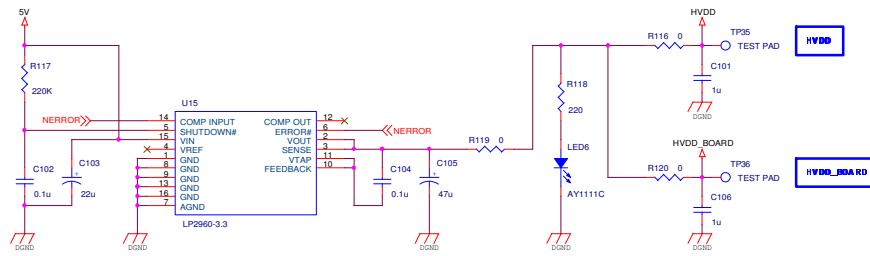




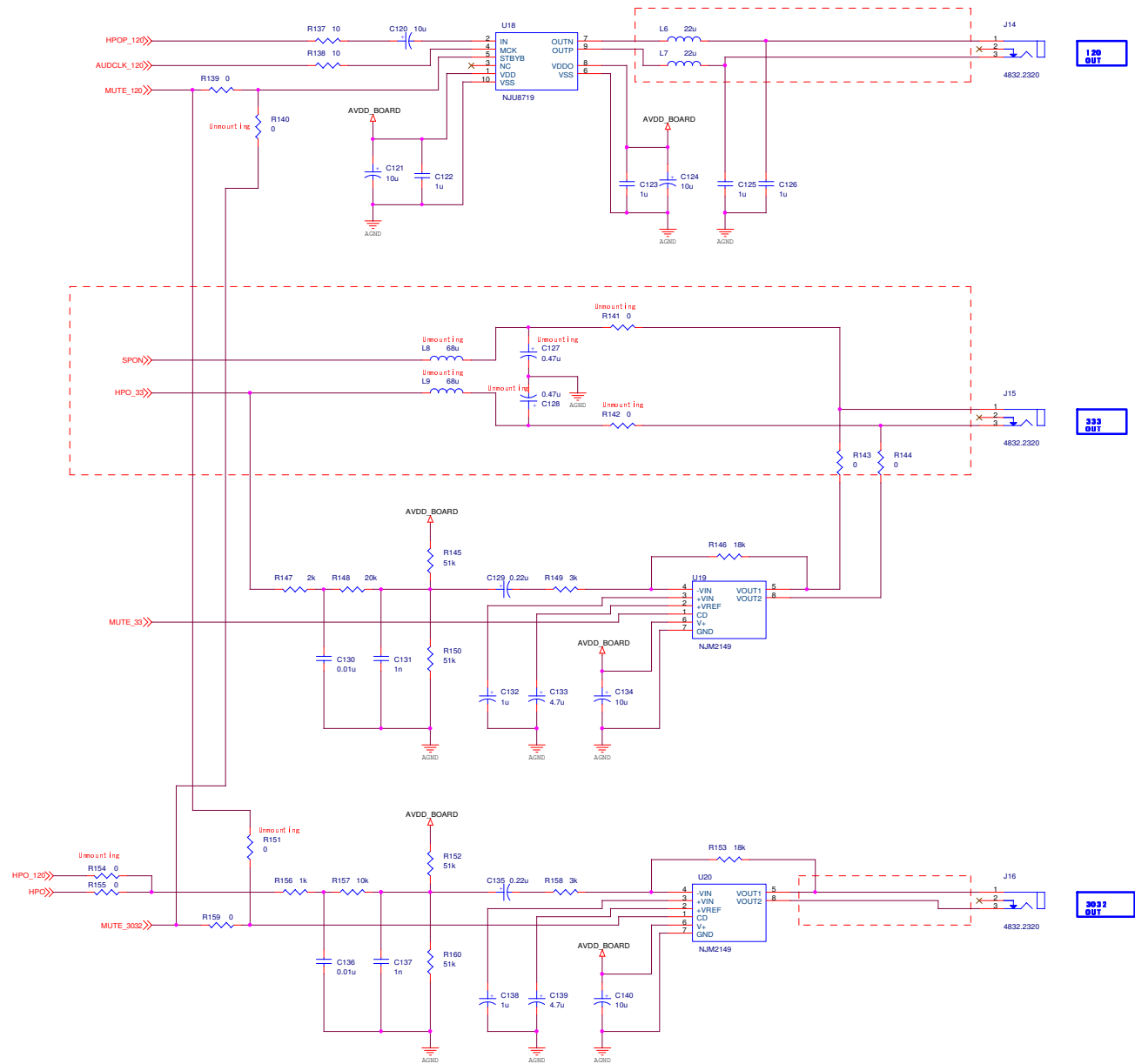
GPIOA4  
GPIOA3  
SOUT  
CLK  
IN  
SFRM1











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