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Application Manual

Real Time Clock Module

RA4000CE/RA8000CE

Product name	Product number
RA4000CE YB A0	**X1B000491A00115**
RA4000CE YB B8	**X1B000491A00915**
RA4000CE YB C0	**X1B000491A01015**
RA4000CE YB D0	**X1B000491A01115**
RA4000CE YB E8	**X1B000491A01915**
RA8000CE YB A0	**X1B000501A00115**
RA8000CE YB B8	**X1B000501A00915**
RA8000CE YB C0	**X1B000501A01015**
RA8000CE YB D0	**X1B000501A01115**

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ETM64E Revision History

Rev. No.	Date	Page	Description
01	6.Dec.2021	All	New established
02	5.Aug.2022	8	*2.2.1 Power-On Sequence.* ・Old: Before turning the power supply back on after being turned off, be sure to maintain an OFF period with the V_{DD} pin set to the GND level for at least **10 seconds** after turning off. ・New: Before turning the power supply back on after being turned off, be sure to maintain an OFF period with the V_{DD} pin set to the GND level for at least **100 ms** after turning off.
		20	Replacement : *Figure 3.11 Clock/Calendar Counter Configuration* Address was corrected of Figure3.11
		25, 26, 27	Register name corrected: *Page_25* ・Origin : SEC_BIN0_MIR to SEC_BIN4_MIR. ・Correct : SEC_BIN0 to SEC_BIN4.
		27	・Origin : Registers SEC_BIN0 to SEC_BIN4 (Addresses 0x00 to 0x04) ・Correct : Registers SEC_BIN0 to SEC_BIN4 (Addresses 0x12 to 0x16)
		65, 66	-Changed "BIN mode" of "0x00 ~ 0x04" of register list Bank0 from "SEC_BIN0 ~ 4" to "Not used". -Changed "BIN mode" of "0x12 ~ 0x16" of register list Bank1 from "SEC_BIN0_MIR ~ 4_MIR" to "SEC_BIN0 ~ 4". *Symbol meanings*
		72, 80	-Deleted "BIN mode", "SEC_BIN0-4" of "0x00 ~ 0x04" of Bank0 in the detailed register explanation. *Delete*. -Changed the register names of "BIN mode", "SEC_BIN0_MIR-4_MIR" of "0x12 ~ 0x16" of Bank1 in the detailed register description to "SEC_BIN0-4", *Rename*. Moved the function description from "SEC_BIN" of "0x00 ~ 0x04". *Move*.
		100	*Power-On Characteristics* ・old: To ensure that power-on reset takes effect, maintain the VDD = GND condition for at least **10 seconds** after power-off. ・new: To ensure that power-on reset takes effect, maintain the VDD is GND level condition for at least **100ms** after power-off.

Preface

This document is the application manual for describing the functions, control method, specifications, and electrical characteristics of Seiko Epson Real-Time Clock (RTC) modules RA4000CE and RA8000CE. This manual is provided for designers who develop products using the RA4000CE/RA8000CE.

The RA4000CE is accessed through SPI from the host; the RA8000CE is accessed through I^2C-Bus. For the operations and control methods of these interfaces, refer to a host device manual or other documents.

Notational conventions and symbols in this manual

Notation of Numbers

This manual describes numbers in decimal, binary, and hexadecimal notations.

Decimal	Examples: 1, 10, 123 (general values, date and time, etc.)
Binary	Examples: 0b0, 0b10, 0b1111 (control bit setting values, read values, etc.)
Hexadecimal	Examples: 0x0, 0xF, 0xFF (addresses, register setting values, etc.)

Notation of Register and Bit Names

This manual describes register and bit names as shown below.

Register name: Register SEC

Bit name: TSTP_INTE.STOP bit
This represents the STOP bit in Register TSTP_INTE.

TCTL.FSEL[1:0] bits
This represents two bits in Register TCTL: FSEL1 and FSEL0 bits.

Notation of Channel Numbers

The time stamp function has provided a pin and control bit for each channel that has the same function as the other channels. The pin and bit names contain a channel number (e.g., 1 and 2). This manual uses "*n*" for the channel numbers to explain the pins and bits for all channels collectively, if there is no need to be individually described. Furthermore, "***" is used as a different part of a bit name for describing plural bit names that have a same part.

Pin name: EVIN1 and EVIN2 → EVIN*n*

Bit name: EVIN*n*_EN.EVIN1EN and EVIN*n*_EN.EVIN2EN
→ EVIN*n*_EN.EVIN*n*EN

EVIN*n*_EN.EVIN1CPEN, CAP_EN.VTMPLCPEN, and others
→ ***CPEN

Table of Contents

1 Overview

The RA4000CE/RA8000CE is a real-time clock module with integrated 32.768 kHz digital temperature compensated crystal oscillator (DTCXO) and conforms to the AEC-Q100 compliant. It includes various functions such as a second-to-year clock/calendar with a leap-year correction, time alarm, wakeup timer, time update interrupts, clock output, and a time stamp function that can record two times and dates when an external or internal event occurs, and the power supply statuses that have been detected by the self-monitoring function. This product is capable of low power operation and conforms to the AEC-Q100 compliant, thus it is usable for on-vehicle applications as well as various time keeping applications.

RA4000CE YB A 0
① ② ③④

① Model CE type package 3.2 x 2.5 x 1.0 mm
② Frequency tolerance
③ Pin Option
A: Option A-E
④ Reset output function
0: No /RST pin
8: With /RST pin (V_{DD} drop detection voltage: +2.4 V Typ.)

Table 1.1 Product Lineup

Product name	Interface	Frequency accuracy *1	External event input (EVIN*n*)	Reset output (/RST)	Clock output (FOUT or /INT)	FOUT enable (FOE)	Status output (SOUT)
RA4000CE Option A YB	3-wire SPI	YB	2 inputs	–	✓	–	–
RA4000CE Option B YB		YB	2 inputs	✓	✓	–	–
RA4000CE Option C YB		YB	–	–	✓	–	–
RA4000CE Option D YB	4-wire SPI	YB	1 input	–	✓	–	✓
RA4000CE Option E YB		YB	1 input	✓	✓	–	✓
RA8000CE Option A YB	I^2C-Bus	YB	2 inputs	–	✓	–	✓
RA8000CE Option B YB		YB	2 inputs	✓	✓	–	✓
RA8000CE Option C YB		YB	–	–	✓	–	–
RA8000CE Option D YB		YB	1 input	–	✓	✓	✓

✓: Available, –: Unavailable

*1 For the accuracy (YB), refer to the frequency tolerance shown in "*5.3 Frequency Characteristics*."

Table 1.2 Features

Product lineup		RA4000CE	RA8000CE
Host interface		3-wire SPI or 4-wire SPI *1	I^2C-Bus *1
Crystal oscillator		• A 32.768 kHz digital temperature compensated crystal oscillator (DTCXO) is included.	
Clock/calendar		• BCD counters for counting seconds, minutes, hours, days, months, and years, and a day-of-week counter are included. [BCD mode] • A binary counter for counting 1/1024 seconds is included. • A binary counter for counting seconds such as UNIX time is included. [BIN mode] • An automatic leap year correction function is included and a leap second correction method is provided. [BCD mode] • Time update interrupts can be generated. (1-second, 1-minute, or 1-hour counter update intervals) [BCD mode] • A theoretical regulation function is included.	
Wakeup timer		• Can generate an interrupt in 976.56 µs to 32-year cycle. • Can be used as a time integration meter. • Can be used as a watchdog timer. • Can be used as a universal counter for counting EVIN2 pin inputs (external event inputs).	
Alarm		Can generate an interrupt at the specified day (or day of the week), hour, minute, and second. [BCD mode]	
Time stamp	**Trigger source**	• External event (EVIN*n*) input *1 • Voltage drop detection/oscillation stop detection • Command input from the host	
	Record data	• 1/1024-second data • Time data (seconds, minutes, hours, days, months, and years [BCD mode] or binary time [BIN mode]) • Trigger source • Internal status	

Product lineup		RA4000CE	RA8000CE
	Number of recordable events	Two events	
Clock output (FOUT) *1		• Selectable from 32.768 kHz, 1024 Hz, and 1 Hz outputs • Output can be controlled by a register.	
Status output (SOUT) *1		Can output the selected internal flag (interrupt flag, voltage drop detection flag) status.	
Reset output *1		Can output a reset signal when a V_{DD} voltage drop status is detected.	
Self-monitoring function		Can generate an interrupt when the oscillation stops or a V_{DD} voltage drop status is detected.	
Operating voltage (V_{DD})		1.60 V to 5.5 V	
Operating temperature		-40 °C to +125 °C	

*1 See Table 1.1.

1.1 Block Diagram

RA4000CE (3-wire SPI)

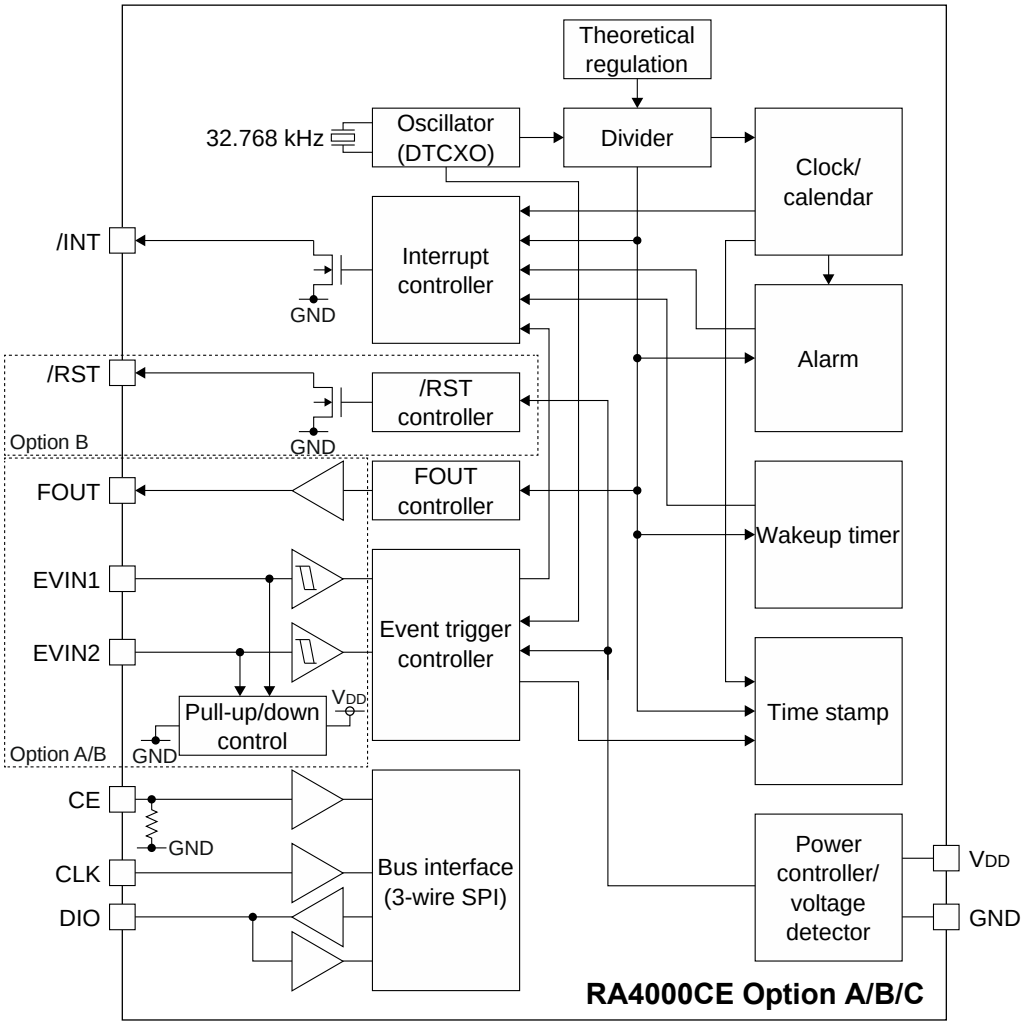


Figure 1.1 RA4000CE Option A/B/C Block Diagram

RA4000CE (4-wire SPI)

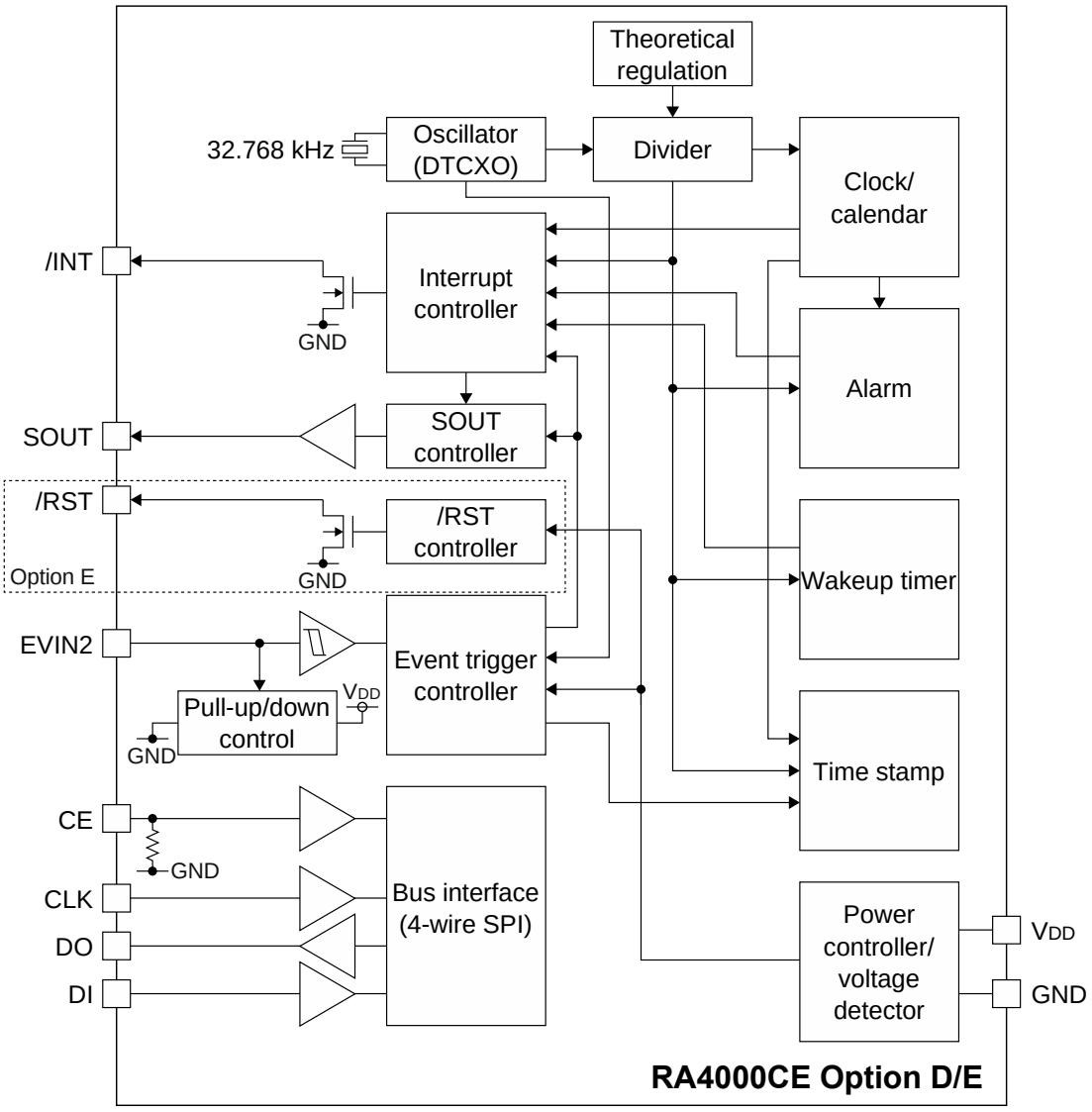


Figure 1.2 RA4000CE Option D/E Block Diagram

RA8000CE (I²C-Bus)

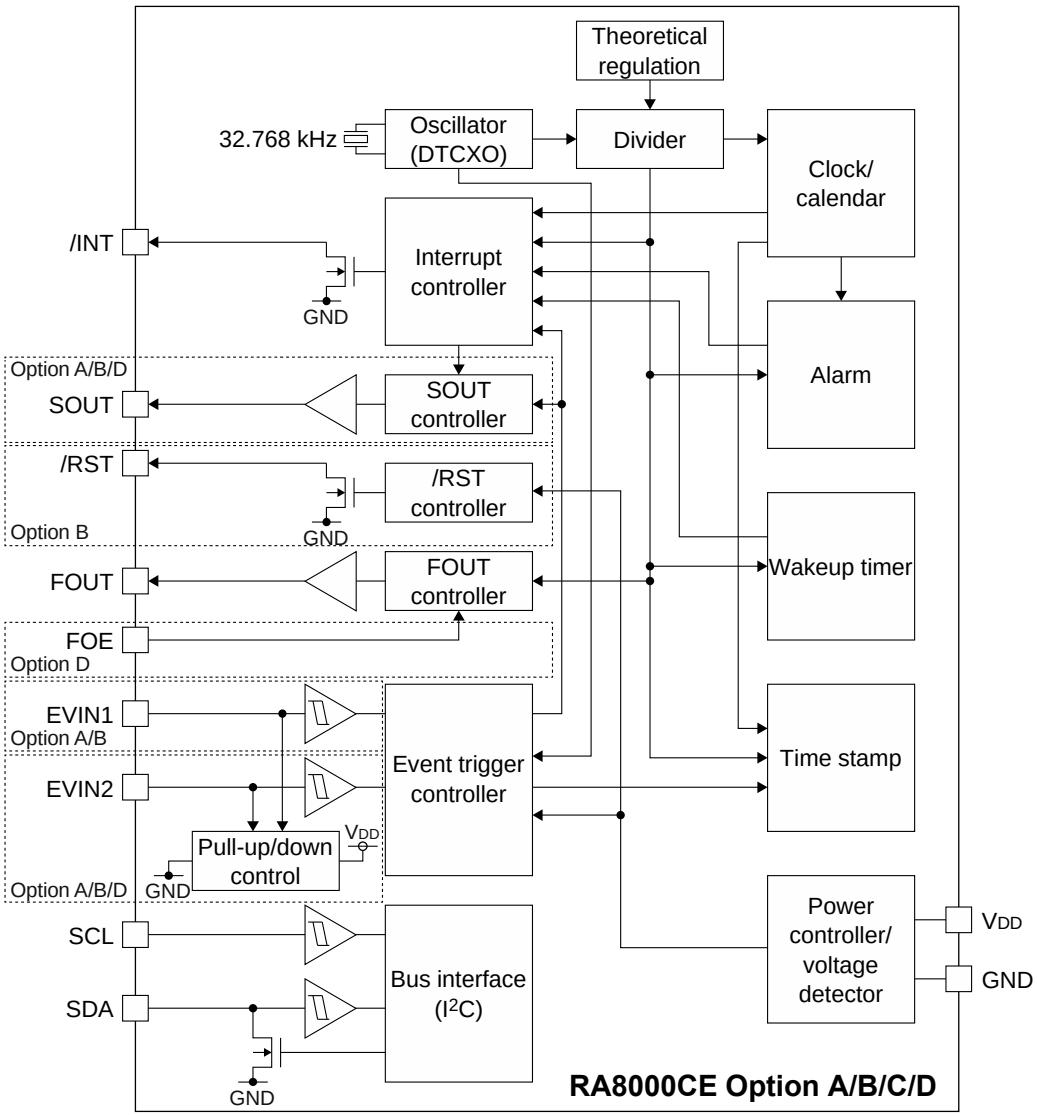


Figure 1.3 RA8000CE Option A/B/C/D Block Diagram

1.2 Pin

1.2.1 Pin Alignment Diagram

RA4000CE

Option A

Pin name	No.	No.	Pin name
EVIN1	1	10	/INT
V_{DD}	2	9	GND
CE	3	8	CLK
FOUT	4	7	DIO
N.C.	5	6	EVIN2

Option B

Pin name	No.	No.	Pin name
EVIN1	1	10	/INT
V_{DD}	2	9	GND
CE	3	8	CLK
FOUT	4	7	DIO
/RST	5	6	EVIN2

Option C

Pin name	No.	No.	Pin name
N.C.	1	10	N.C.
V_{DD}	2	9	GND
CE	3	8	CLK
/INT	4	7	DIO
N.C.	5	6	N.C.

Option D

Pin name	No.	No.	Pin name
DI	1	10	SOUT
V_{DD}	2	9	GND
CE	3	8	CLK
/INT	4	7	DO
N.C.	5	6	EVIN2

Option E

Pin name	No.	No.	Pin name
DI	1	10	SOUT
V_{DD}	2	9	GND
CE	3	8	CLK
/INT	4	7	DO
/RST	5	6	EVIN2

Figure 1.4 RA4000CE Pin Alignment Diagrams

RA8000CE

Option A

Pin name	No.	No.	Pin name
EVIN1	1	10	SOUT
V_{DD}	2	9	GND
/INT	3	8	SCL
FOUT	4	7	SDA
N.C.	5	6	EVIN2

Option B

Pin name	No.	No.	Pin name
EVIN1	1	10	SOUT
V_{DD}	2	9	GND
/INT	3	8	SCL
FOUT	4	7	SDA
/RST	5	6	EVIN2

Option C

Pin name	No.	No.	Pin name
N.C.	1	10	N.C.
V_{DD}	2	9	GND
/INT	3	8	SCL
FOUT	4	7	SDA
N.C.	5	6	N.C.

Option D

Pin name	No.	No.	Pin name
FOE	1	10	SOUT
V_{DD}	2	9	GND
/INT	3	8	SCL
FOUT	4	7	SDA
N.C.	5	6	EVIN2

Figure 1.5 RA8000CE Pin Alignment Diagrams

* The N.C. pins (Pins 1, 5, and 6) of the models in Option A, C, or D are always pulled down with a built-in pull-down resister. Therefore, these pins should be left open (do not electrically connect anything).

1.2.2 Pin Descriptions

Symbol Meanings

I/O	I:	Input pin
	O:	Output pin
	I/O:	Input/output pin
Initial state	Hi-Z:	High impedance
	PU:	Pulled up
	PD:	Pulled down
Model-specific column	✓:	Available
	–:	Unavailable

Table 1.3 Pin Descriptions

Pin name	I/O	Initial state	Function	RA4000CE					RA8000CE			
				A	B	C	D	E	A	B	C	D
EVIN1	I	PU (1 MΩ)	External event input pins These pins are used to input time stamp trigger signals (detectable even in reset output state (Safe mode)). Programmable pull-up and pull-down resistors and noise filters are included.	✓	✓	–	–	–	✓	✓	–	–
EVIN2				✓	✓	–	✓	✓	✓	✓	–	✓
CLK	I	Hi-Z	3-wire/4-wire SPI serial clock input pin In Normal mode, placing this pin into a floating state is not allowed. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	✓	✓	✓	✓	✓	–	–	–	–
DIO	I/O	Hi-Z	3-wire SPI serial data input/output pin In Normal mode and when this pin is in input state, placing this pin into a floating state is not allowed. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	✓	✓	✓	–	–	–	–	–	–
DO	O	Hi-Z	4-wire SPI serial data output pin In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to output and set into a Hi-Z state.	–	–	–	✓	✓	–	–	–	–
DI	I	Hi-Z	4-wire SPI serial data input pin In Normal mode, placing this pin into a floating state is not allowed. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	–	–	–	✓	✓	–	–	–	–
CE	I	PD (300 kΩ)	3-wire/4-wire SPI slave select input pin A pull-down resistor is included. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	✓	✓	✓	✓	✓	–	–	–	–
SCL	I	Hi-Z	I^2C-Bus serial clock input pin In Normal mode, placing this pin into a floating state is not allowed. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed. This pin can be externally pulled up to a voltage up to 5.5 V.	–	–	–	–	–	✓	✓	✓	✓
SDA	I/O	Hi-Z	I^2C-Bus serial data input/output pin (N-ch. open drain) This pin inputs or outputs addresses, data, acknowledgement and other bits in sync with the SCL signal. This pin is an N-ch open drain output and can be externally pulled up to a voltage up to 5.5 V. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	–	–	–	–	–	✓	✓	✓	✓
FOUT	O	Hi-Z	Clock output pin (CMOS) 32.768 kHz, 1024 Hz or 1 Hz clock output is selectable. Can be switched to the wakeup timer interrupt output (CMOS). In Safe mode with the WTICFG.RSTOPT0 bit set to 0, this pin is disabled to output and set into a Hi-Z state.	✓	✓	–	–	–	✓	✓	✓	✓
FOE	I	Hi-Z	FOUT output enable input pin When an H level is input, the FOUT pin outputs a square wave with the frequency set by a register. When an L level is input, the FOUT pin is set into a Hi-Z state. In Safe mode with the WTICFG.RSTOPT1 bit set to 0, this pin is disabled to input, thus a floating state is allowed.	–	–	–	–	–	–	–	–	✓

Pin name	I/O	Initial state	Function	RA4000CE					RA8000CE			
				A	B	C	D	E	A	B	C	D
/INT	O	Hi-Z	Interrupt output pin (N-ch. open drain) The wakeup timer, time update, alarm, and/or event detection interrupt signals can be selected to output from this pin. When two or more interruptions are selected, they are ORed before being output.(Equal to NOR gate) In Safe mode with the WTICFG.RSTOPT0 bit set to 0, this pin is disabled to output and set into a Hi-Z state. This pin can be externally pulled up to a voltage up to 5.5 V.	✓	✓	✓	✓	✓	✓	✓	✓	✓
SOUT	O	Hi-Z	Status output pin One of the internal flags (TF/AF/UF/EF/VTMPLF/VLF) can be selected to output its status from this pin. The output signal polarity can also be selected. In Safe mode with the WTICFG.RSTOPT0 bit set to 0, this pin is disabled to output and set into a Hi-Z state.	–	–	–	✓	✓	✓	✓	–	✓
/RST	(I) /O	Hi-Z	Reset output pin (N-ch open drain) A reset signal can be output to external devices when a V_{DD} voltage drop below the predefined value is detected. When the V_{DD} voltage is restored (a V_{DD} voltage rise to the predefined value is detected), the reset output is cancelled (set to a Hi-Z state) after 60 ms from the detection. This pin is an N-ch open drain output. Connect an appropriate pull-up resistor according to the capacity of the signal line. The external pull-up voltage should be the V_{DD} level of the RTC or higher. When the reset output function is not used in the model with the /RST pin (RA4000CE-B, E, RA8000CE-B), this pin should be fixed at a GND level.	–	✓	–	–	✓	–	✓	–	–
V_{DD}	–	–	Main power supply pin	✓	✓	✓	✓	✓	✓	✓	✓	✓
GND	–	–	Ground pin	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes:
- Do not leave the unused input and input/output pins open nor apply an intermediate potential to them if the internal pull-up or -down resistor is not enabled.
- Leave the output pins (FOUT, SOUT, /INT, and DO) open when they are not used.
- When the reset output function is not used in the model with the /RST pin function, the /RST pin should be fixed at a GND level.
- The input pins allow applying a voltage up to 5.5 V regardless of the V_{DD} voltage level.
- The /INT output pin can be pulled up to a voltage up to 5.5 V regardless of the V_{DD} voltage level.
- The /RST output pin can be pulled up to a voltage within the range from V_{DD} to 5.5 V.
- Pin 5 of the models without the /RST pin function should be left open, as it outputs an L level.

2 Power Supply and Initialization

2.1 Power Supply

The table below lists the RA4000CE/RA8000CE power supply pins.

Table 2.1 List of Power Supply Pins

Pin name	Function
V_{DD}	Main power supply pin
GND	Ground pin

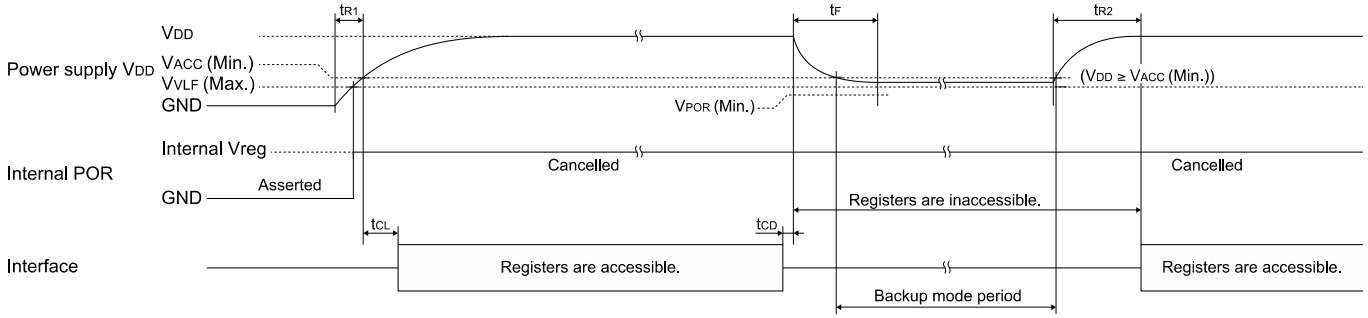
The RA4000CE/RA8000CE operates with the power supply voltage applied to the V_{DD} pin.
For the operating power supply range, refer to "*5.2 Recommended Operating Conditions*."

Note: Design the PCB pattern so that a bypass capacitor will be placed as close to the V_{DD} pin as possible.

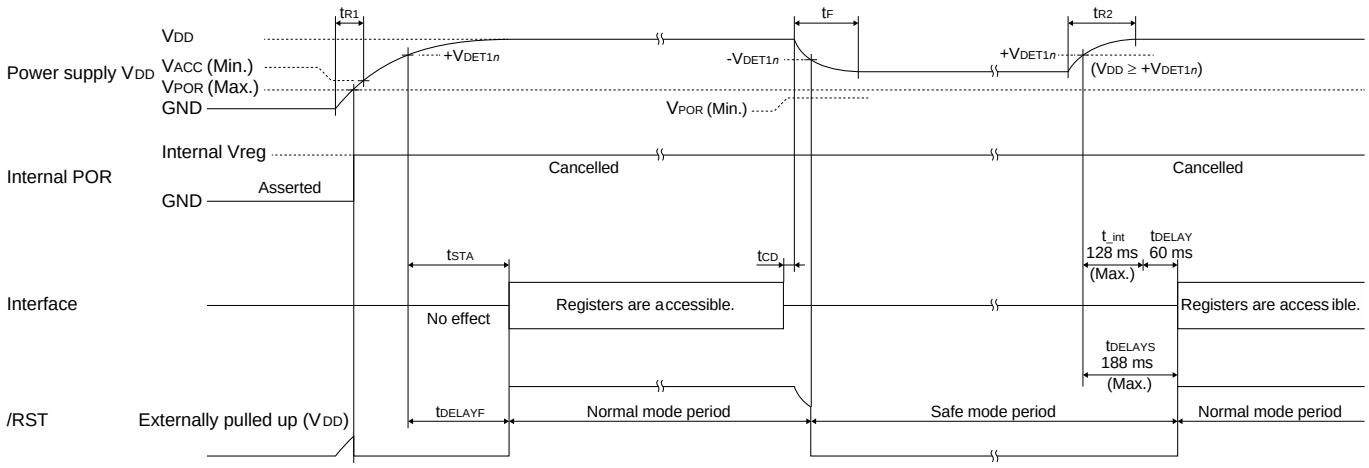
2.2 Initialization

2.2.1 Power-On Sequence

The RA4000CE/RA8000CE executes a power-on reset processing when the V_{DD} voltage is supplied. To make certain that the RA4000CE/RA8000CE executes a power-on reset, satisfy the power-on specifications (t_{R1}, refer to "*5.6 Power-On Characteristics*"). The t_{CL} in Figure 2.1 shows the time for canceling power-on reset.
Before turning the power supply back on after being turned off, be sure to maintain an OFF period with the V_{DD} pin set to the GND level for at least 100 ms after turning off. Then turn the power supply back on again with the power supply initial rise time specification satisfied.



(1) In the case of a model without the /RST output function



(2) In the case of a model with the /RST output function

Figure 2.1 Power-On Sequence

2.2.2 Oscillation Start-UP Time

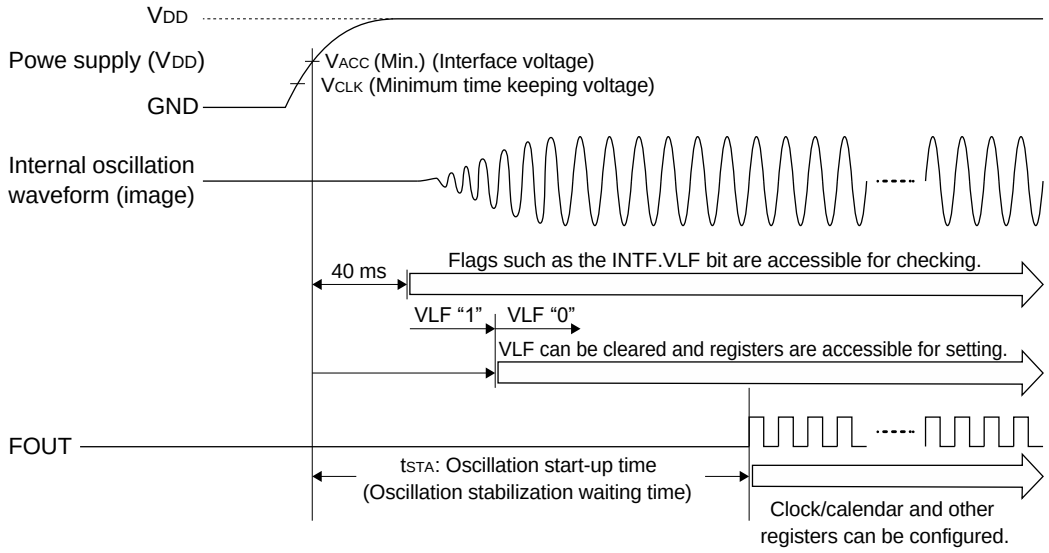
When the V_{DD} voltage is applied, the crystal oscillation circuit starts oscillating. The host interface becomes usable after 40 ms from turning V_{DD} on. However, a wait time is required until the internal crystal oscillation waveform has a sufficient amplitude before the clock/calendar counter value can be set and read. This refers to the oscillation start-up time (t_{STA}, refer to "*5.3 Frequency Characteristics*").

There are two methods to secure the wait time in the models without the /RST output function: one is the method for repeatedly trying to clear the INTF.OSCSTPF and INTF.VLF bits, another is the method for waiting by the host until t_{STA} has elapsed after applying V_{DD}. The former can shorten the wait time until the clock/calendar counter value will be able to set and read. On the other hand, the latter can set the clock/calendar counter with higher time accuracy, as the crystal oscillation frequency becomes more stable although the wait time becomes longer

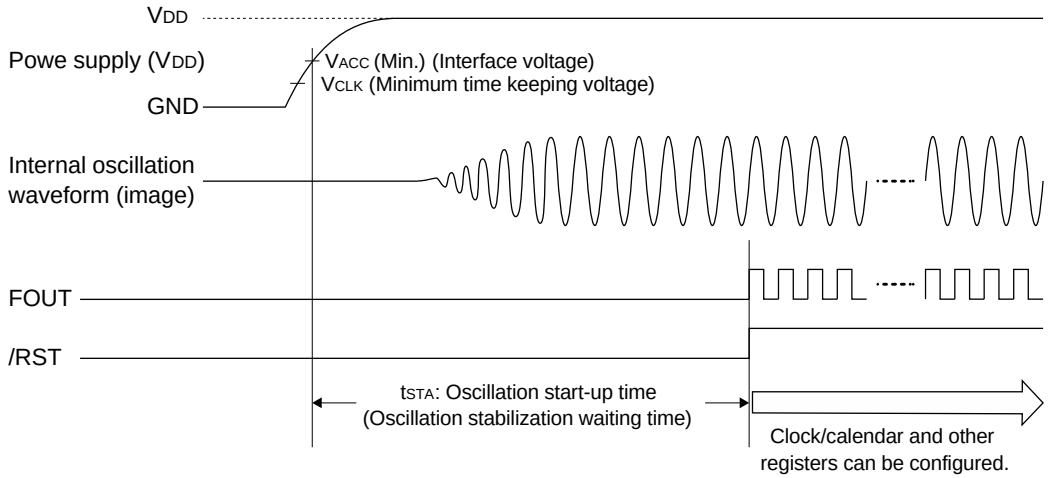
The INTF.OSCSTPF and INTF.VLF bits are set to 1 by the oscillation stop detection function immediately after the crystal oscillation circuit starts oscillating. While the oscillation stop status is being detected, these bits cannot be cleared to 0 even if 0 is written to these bits through the host interface. When the oscillation stop status is cancelled by the grown internal oscillation waveform amplitude, the INTF.OSCSTPF and INTF.VLF bits can be cleared. Therefore, try to clear these bits at arbitrary time intervals until they are actually cleared. After that the clock/calendar counter value can be set and read.
Make sure that the INTF.VLF bit has been cleared before the host configures the operational settings of the functions shown below (*).

On the other hand in the models with the /RST output function, the host interface is disabled until the V_{DD} voltage rises to $+V_{DET1n}$ or higher. When t_{STA} has elapsed as well as the condition of $V_{DD} \geq +V_{DET1n}$ has been satisfied, the /RST output is cancelled and communication can be established allowing access to all registers.

* Functions that should be configured after the INTF.VLF bit is cleared:
  - Selecting the multi-function pin functions (WTICFG.PINMUX[1:0] bit settings)
  - Setting the required timer functions
  - Controlling the FOUT output (TCTL.FSEL[1:0] bit settings)
  - Setting the temperature compensation execution interval (TSTP_INTE.CSEL[1:0] bit settings)



(1) In the case of a model without the /RST output function



(2) In the case of a model with the /RST output function

Figure 2.2 Oscillation Start Sequence

2.2.3 Initial Settings

It is necessary to initially set the registers after initial power on or when a supply voltage drop with the INTF.VLF bit set to 1 from 0 has occurred. This section shows an example of initial settings.

Initial Setting Procedure (for models without the /RST output function)

1. Wait for at least 40 ms after the power is initially turned on.
2. Cancelling POR and detecting oscillation start-up (polling of the INTF.VLF bit)
   The INTF.VLF bit is set to 1 when a power-on reset is issued due to a power supply voltage drop or an oscillation stop is detected.
   2.1. Read the INTF.VLF bit and go to Step 3 when the read value = 0.
   If the INTF.VLF bit = 1, perform Steps 2.2 to 2.4.
   2.2. Write 0x00 to Register INTF to try and clear the INTF.VLF bit and to clear the interrupt flags.
   - PORF bit (Power-on reset detection flag)
   - OSCSTPF bit (Oscillation stop detection flag)
   - UF bit (Time update interrupt flag)
   - TF bit (Wakeup timer interrupt flag)
   - AF bit (Alarm interrupt flag)
   - EVF bit (Event detection interrupt flag)
   - VLF bit (RTC initialize interrupt flag)
   - VTMPLF bit (Temperature compensation update stop interrupt flag)

   2.3. Take a waiting time.
   2.4. Return to Step 2.1.
3. Disable interrupts/counters. (Write 0x00 to Register TSTP_INTE.)
   - CSEL[1:0] bits (Temperature sensor measurement operation interval)
   - UIE bit (Disable time update interrupt)
   - TIE bit (Disable wakeup timer interrupt)
   - AIE bit (Disable alarm interrupt)
   - EIE bit (Disable event detection interrupt)
   - STOP bit (Stop counters)
4. Set the current time.
   For more information, refer to "*3.2 Clock and Calendar Function*."
5. Set alarm.
   For more information, refer to "*3.6 Alarm Function*."
6. Set wakeup timer.
   For more information, refer to "*3.7 Wakeup Timer Function*."

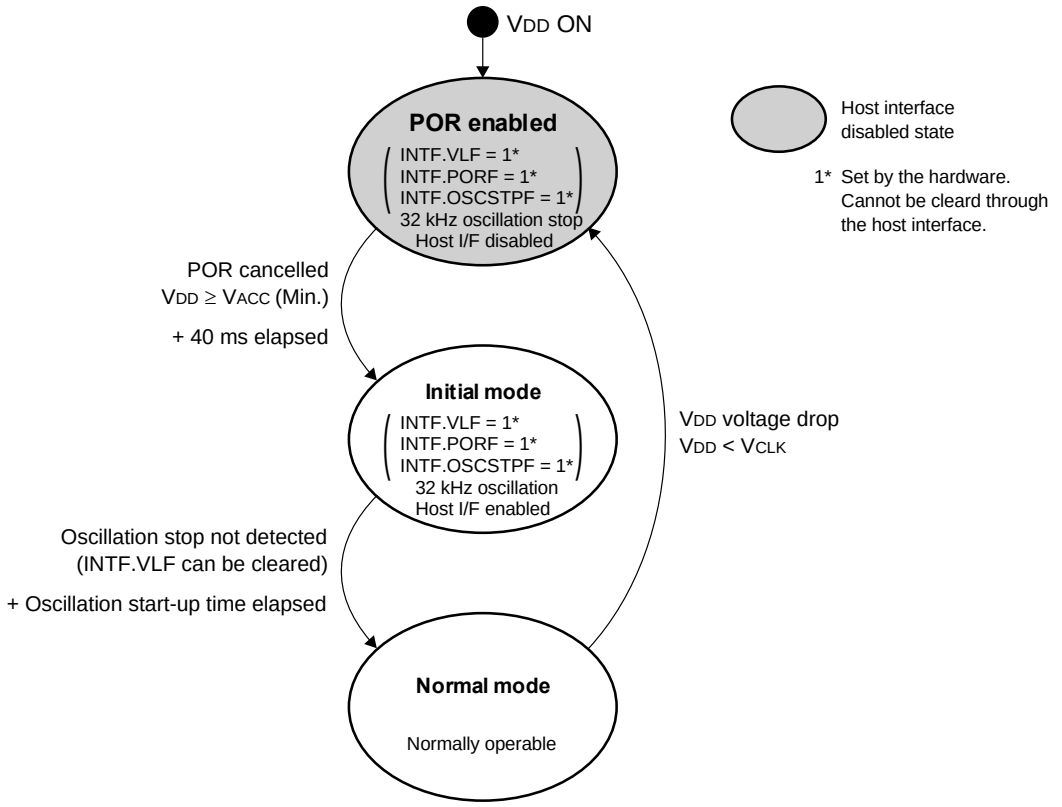
Initial Setting Procedure (for models with the /RST output function)

1. Wait for at least t_{STA} after the power is initially turned on. Or confirm that the /RST output is cancelled.
2. Cancelling POR and detecting oscillation start-up (polling of the INTF.VLF bit)
   The INTF.VLF bit is set to 1 when a power-on reset is issued due to a power supply voltage drop or an oscillation stop is detected.
   2.1. Read the INTF.VLF bit and go to Step 3 when the read value = 0.
   If the INTF.VLF bit = 1, perform Steps 2.2 to 2.4.
   2.2. Write 0x00 to Register INTF to try and clear the INTF.VLF bit and clearing the interrupt flags.
   - PORF bit (Power-on reset detection flag)
   - OSCSTPF bit (Oscillation stop detection flag)
   - UF bit (Time update interrupt flag)
   - TF bit (Wakeup timer interrupt flag)
   - AF bit (Alarm interrupt flag)
   - EVF bit (Event detection interrupt flag)
   - VLF bit (RTC initialize interrupt flag)
   - VTMPLF bit (Temperature compensation update stop interrupt flag)

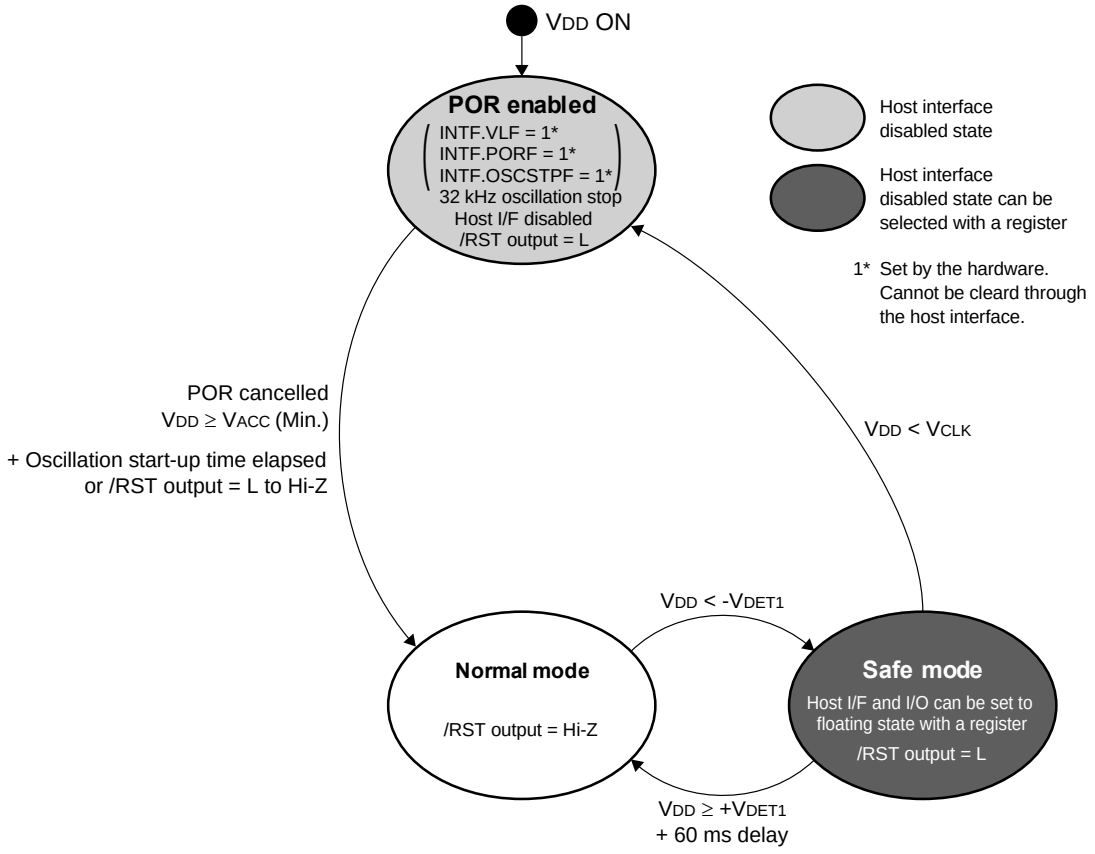
   2.3. Take a waiting time.
   2.4. Return to Step 2.1.
3. Disable interrupts/counters. (Write 0x00 to Register TSTP_INTE.)
   - CSEL[1:0] bits (Temperature sensor measurement operation interval)
   - UIE bit (Disable time update interrupt)
   - TIE bit (Disable wakeup timer interrupt)
   - AIE bit (Disable alarm interrupt)
   - EIE bit (Disable event detection interrupt)
   - STOP bit (Stop counters)
4. Set the current time.
   For more information, refer to "*3.2 Clock and Calendar Function*."
5. Set alarm.
   For more information, refer to "*3.6 Alarm Function*."
6. Set wakeup timer.
   For more information, refer to "*3.7 Wakeup Timer Function*."

2.3 Operating Mode

Figure 2.3shows the state transition diagram of the RA4000CE/RA8000CE.



(1) In the case of a model without the /RST output function



(2) In the case of a model with the /RST output function

Figure 2.3 State Transition Diagram

POR enabled

The RA4000CE/RA8000CE is in a reset state. It cannot be accessed by the host.
POR is enabled and the INTF.VLF bit is set to 1.
When the operating mode has transited from Normal or Safe mode described later to this mode due to a V_{DD} voltage drop below V_{CLK}, POR (Power-On Reset) is executed. In this case, the internal crystal oscillator operation and holding clock/calendar and other data into registers are not guaranteed. If the INTF.VLF bit is set to 1 while operating in Normal mode, it is necessary to initially set the registers again after POR has been cancelled and VLF is cleared in Initial mode.

Initial mode

This is an oscillation start-up state after POR has been cancelled and it transits to Normal mode when the oscillation starting operation has completed. Whether transition to Normal mode has completed or not can be determined by checking that the oscillation stop detection result has changed to a non-detected state and the INTF.VLF bit could be cleared to 0.

Normal mode

The RA4000CE/RA8000CE is in a normal operating state. The host can access the RA4000CE/ RA8000CE registers including the clock/calendar counters.

Safe mode

RA4000CE Option B/D, RA8000CE Option B (available in the models with the /RST output function)

These models output a reset signal from the /RST pin when the power supply voltage V_{DD} drops below the V_{DD} drop detection voltage $-V_{DET1n}$. After that, the reset output is cancelled when the V_{DD} voltage restores to the V_{DD} rise detection voltage $+V_{DET1n}$ or higher. The reset signal output period refers to Safe mode. In Safe mode, the host interface is disabled and the FOE, CE, CLK, DI, DIO, SDA, and SCL inputs can be set into a floating state. The DO, /INT, FOUT, and SOUT outputs go into a Hi-Z state. This pin state control can be enabled or disabled with the WTICFG. RSTOPT[1:0] bits. For more information, refer to "*3.9 Reset Output Function*."

3 Functions

3.1 Host Interface

The RA4000CE includes SPI as the host interface; RA8000CE includes an I^2C-Bus interface. Both models work as a slave device.

3.1.1 Accessing to RA4000CE Registers (SPI)

The RA4000CE registers can be accessed via an SPI bus. The following shows the specifications of the RA4000CE SPI interface:

- Interface type: RA4000CE Option A/B/C: 3-wire SPI, RA4000CE Option D/E: 4-wire SPI
- Slave device
- Data length: 8 bits
- Data format: MSB first
- Clock polarity: High at idle
- Clock phase: Data sampled at the rising edge and shifted out at the falling edge
- Maximum communication speed: 4 Mbits/s
- Address auto-increment function included
- The CE (Slave Select) input pin has a built-in pull-down resistor.

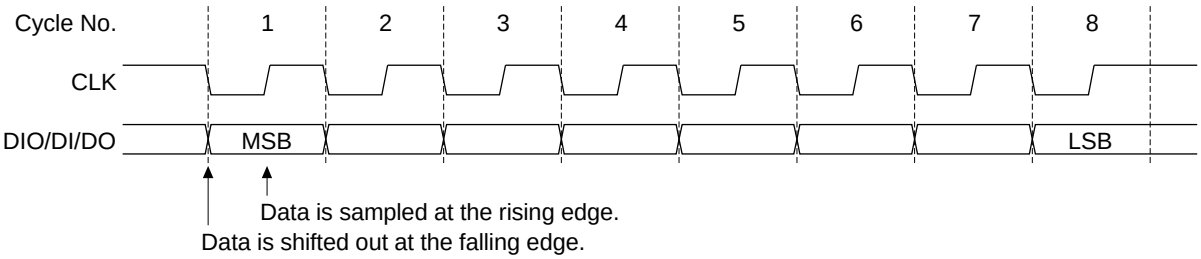


Figure 3.1 SPI Data Format

SPI Interface Pins

The RA4000CE has the SPI interface pins listed in the table below.

Table 3.1 RA4000CE Option A/B/C SPI Interface Pins

Pin name	I/O	Initial state	Function
CLK	I	Hi-Z	SPI serial clock input pin
DIO	I/O	Hi-Z	SPI serial data input/output pin
CE	I	PD	SPI slave select input pin (A pull-down resistor is included.)

Table 3.2 RA4000CE Option D/E SPI Interface Pins

Pin name	I/O	Initial state	Function
CLK	I	Hi-Z	SPI serial clock input pin
DI	I	Hi-Z	SPI serial data input pin
DO	O	Hi-Z	SPI serial data output pin
CE	I	PD	SPI slave select input pin (A pull-down resistor is included.)

Connection with the host

Figure 3.2 shows examples of connection with the host.

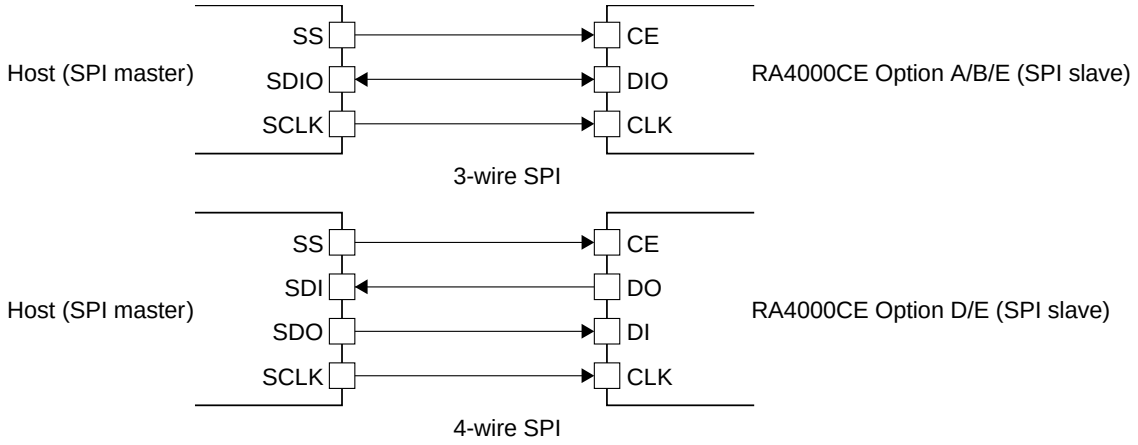


Figure 3.2 Example of Connection Between Host and RA4000CE

Pull-down resistor (CE pin)

The RA4000CE includes a pull-down resistor on the CE pin. It cannot be disconnected via software. The CE pin is always pulled down.

Writing Data to Registers

The host sets the CE signal to high to select the RA4000CE as the slave device to be accessed. Then it starts outputting the synchronous clock (CLK). In sync with this clock, the host first sends an 8-bit address data (register address to which the first data is written) including a bit to specify write mode to the RA4000CE DIO (Option A/B/C) or DI (Option D/E) pin, and write data follows in eight-bit units. Figure 3.3 shows the bit configuration of the address data to be sent first when writing data.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	7-bit address (0b000 0000–0b111 1111)						

↑ Setting 0 specifies write mode.

Figure 3.3 SPI Data Write Address Data

Figure 3.4 shows RA4000CE register data write operations. Every time an 8-bit data is written, it is stored to the specified register and at the same time only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0. The high-order 3 bits of the register address are not automatically incremented, therefore, to change them, negate the CE signal (CE signal = low) to cancel the slave select status once, and then restart communication by sending new address data.

Be sure to avoid negating the CE signal until the last eight-bit data has been sent completely. If the CE signal is negated in the middle of a transfer, the data that has not be sent for 8 bits yet is discarded and not written to the registers.

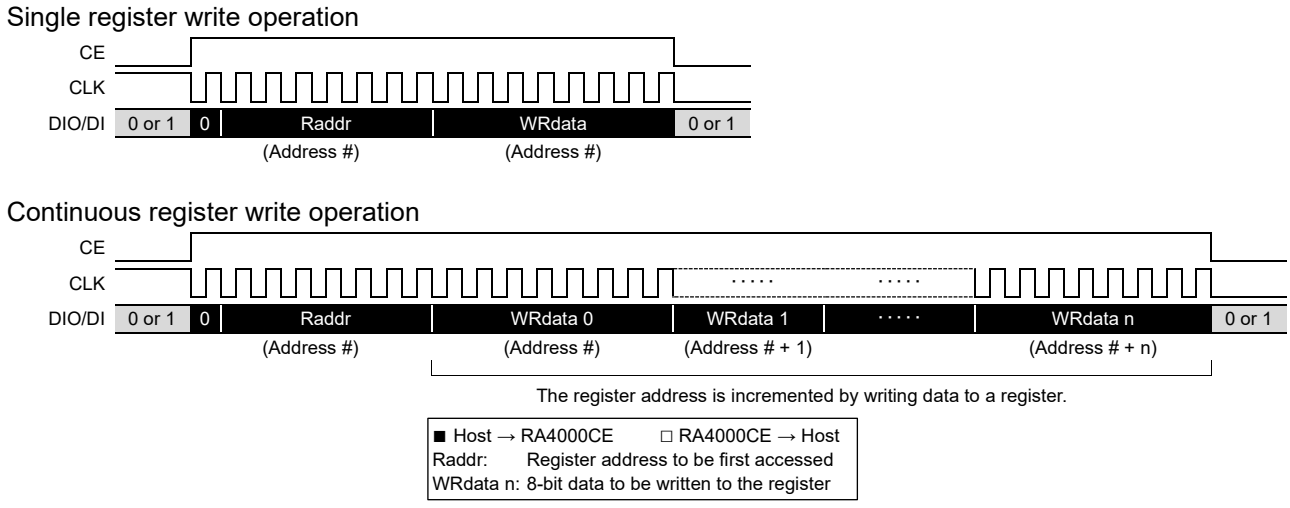


Figure 3.4 SPI Register Write Operation

Reading Data from Registers

The host sets the CE signal to high to select the RA4000CE as the slave device to be accessed. Then it starts outputting the synchronous clock (CLK). In sync with this clock, the host first sends an 8-bit address data (register address from which the first data is read) including a bit to specify read mode to the RA4000CE DIO (Option A/B/C) or DI (Option D/E) pin. Once the address data is received, the RA4000CE sends read data from the DIO (Option A/B/C) or DO (Option D/E) pin to the host in eight-bit units until the host stops outputting the clock. The D1 pin inputs are ineffective in this period. Figure 3.5 shows the bit configuration of the address data to be sent first when reading data.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	7-bit address (0b000 0000–0b111 1111)						

↑ Setting 1 specifies read mode.

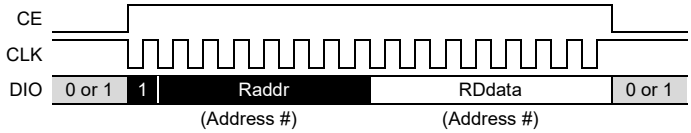
Figure 3.5 SPI Data Read Address Data

Figure 3.6 shows RA4000CE register data read operations. Every time an 8-bit data is read, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

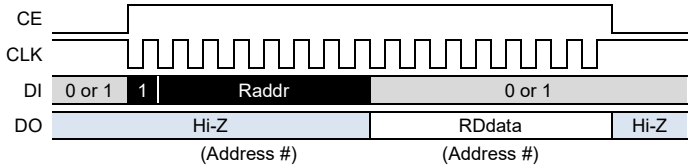
To change the high-order 3 bits of the address to be accessed, negate the CE signal to cancel the slave select status once, and then restart communication by sending new address data.

Single register read operation

RA4000CE Option A/B/C

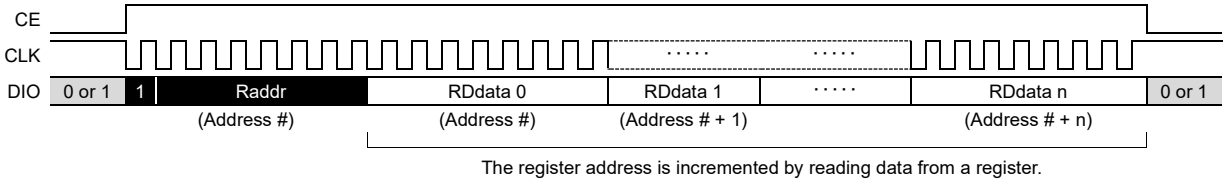


RA4000CE Option D/E

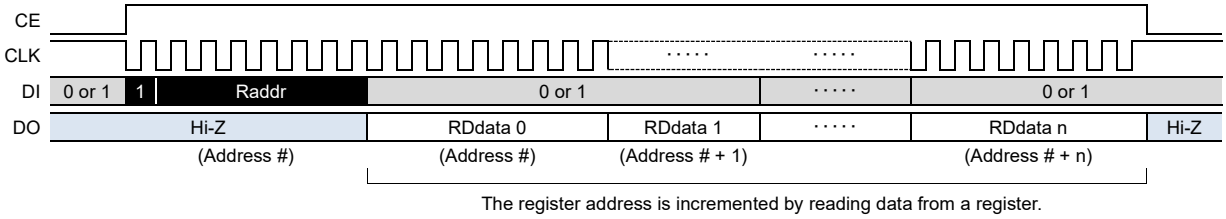


Continuous register read operation

RA4000CE Option A/B/C



RA4000CE Option D/E



■ Host → RA4000CE □ RA4000CE → Host
Raddr: Register address to be first accessed
RDdata n: 8-bit data read from the register

Figure 3.6 SPI Register Read Operation

3.1.2 Accessing to RA8000CE Registers (I²C-Bus)

The RA8000CE registers can be accessed via an I²C-Bus. The following shows the specifications of the RA8000CE I²C-Bus interface circuit:

- Slave device
- Standard mode (up to 100 kbits/s) and fast mode (up to 400 kbits/s) supported
- 7-bit slave address 0x32

I²C-Bus Interface Pins

The RA8000CE has the I²C-Bus interface pins listed in the table below.

Table 3.3 I²C-Bus Interface Pins

Pin name	I/O	Initial state	Function
SCL	I	Hi-Z	I²C-Bus serial clock input pin
SDA	I/O	Hi-Z	I²C-Bus serial data input/output pin (N-ch. open drain)

Connection with the host

Figure 3.7 shows an example of connection with the host.

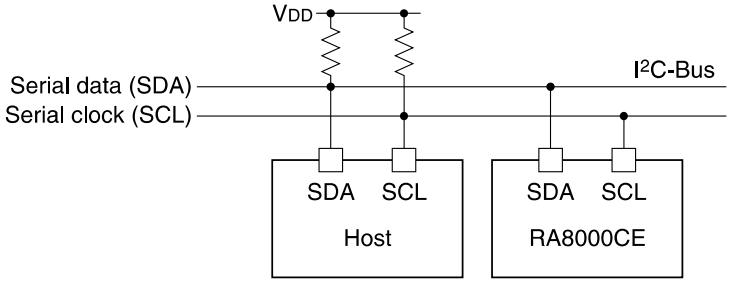


Figure 3.7 Example of Connection Between I²C-Bus Host and RA8000CE

Slave Address

The slave address of the RA8000CE is the 7-bit value shown below.

←			Slave address			→	R/W
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	1	0	*

* 0: Write mode, 1: Read mode

Figure 3.8 RA8000CE I²C-Bus Slave Address

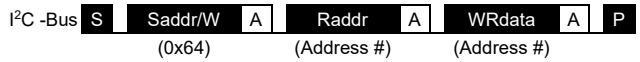
Writing Data to Registers

A communication starts when the host generates a START condition on the I²C-Bus and outputs a slave address with the R/W bit that specifies write mode. The host then outputs the 8-bit register address to which the first data is written. After that the host outputs write data in eight-bit units for the required number, finally it generates a STOP condition. The RA8000CE returns ACK every time it receives an eight-bit data and gets ready to receive data that follows.
Figure 3.9 shows RA8000CE register data write operations. Every time an 8-bit data is written, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

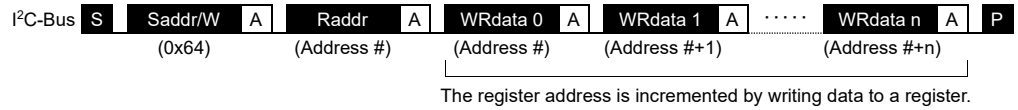
To change the high-order 4 bits of the address to be accessed, generate a Repeated START condition or STOP and START conditions, and then restart by sending new read address.

If a STOP condition is not input and the I²C-Bus has stayed in busy state even when 1 second or more has elapsed from reception of the slave address, to prevent a malfunction, the RA8000CE automatically initializes the I²C-Bus interface circuit to generate a bus timeout. As a result, SDA goes into Hi-Z to wait for a START condition. Therefore, to resume communication, generate a START condition and perform transmission again.

Single register write operation



Continuous register write operation



■ Operation by the host □ Operations by RA8000CE
S: START condition, Sr: Repeated START condition,
P: STOP condition, A: ACK, N: NACK,
Saddr/W: Slave address + W (0), Raddr: Register address to be first accessed,
WRdata n: 8-bit data to be written to the register

Figure 3.9 Register Write Operation through I²C-Bus

Reading Data from Registers

A communication starts when the host generates a START condition on the I²C-Bus and outputs a slave address with the R/W bit that specifies write mode. The host then outputs the 8-bit register address from which the first data is read. After that the host generates a Repeated START condition and outputs a slave address with the R/W bit that specifies read mode. Once this slave address is received, the RA8000CE sends read data in eight-bit units until the host returns NACK.

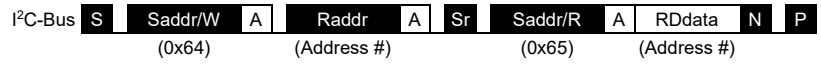
The host returns ACK every time it receives an eight-bit data and requests to send data that follows. When the last data is received, the host returns NACK and generates a STOP condition to terminate communication.
Figure 3.10 shows RA8000CE register data read operations. Every time an 8-bit data is read, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

To change the high-order 4 bits of the address to be accessed, generate a Repeated START condition or STOP and START conditions, and then restart by sending new read address.

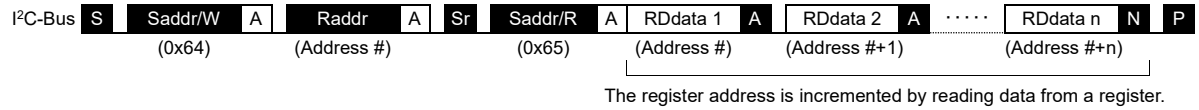
The RA8000CE retains the address from which data has been read at the end of communication. If the host starts the subsequent reading by sending the slave address with the R/W bit that specifies read mode without specifying a read address, the RA8000CE starts reading from the address that follows the last time.

If a STOP condition is not input and the I²C-Bus has stayed in busy state even when 1 second or more has elapsed from reception of the slave address, to prevent a malfunction, the RA8000CE automatically initializes the I²C-Bus interface circuit to generate a bus timeout. As a result, SDA goes into Hi-Z to wait for a START condition. If the data reading is continued in this state, the data is all read as 0xFF.
To resume communication, generate a START condition and perform transmission again.

Single register read operation



Continuous register read operation



■ Operation by the host □ Operations by RA8000CE
S: START condition, Sr: Repeated START condition,
P: STOP condition, A: ACK, N: NACK, Saddr/W: Slave address + W (0),
Saddr/R: Slave address + R (1), Raddr: Register address to be first accessed,
RDdata n: 8-bit data read from the register

Figure 3.10 Register Read Operation through I²C-Bus

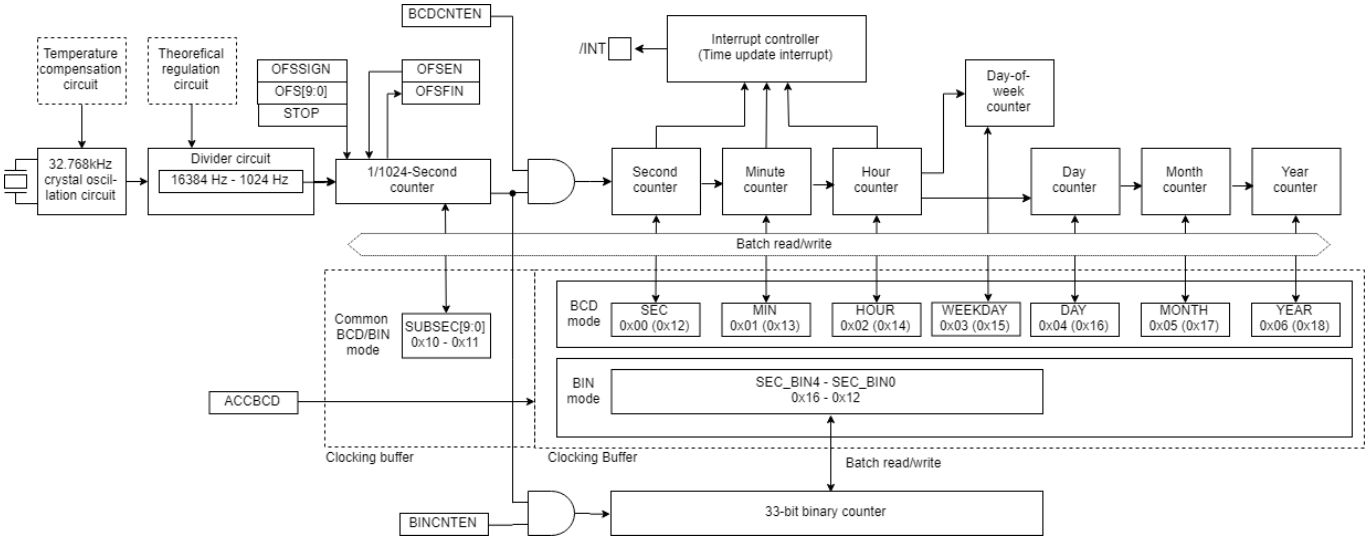
3.2 Clock and Calendar Function

3.2.1 Overview

The following shows the features of the clock and calendar function:

- BCD counters for counting seconds, minutes, hours, days, months and years, and a day-of-week counter are included. [BCD mode]
- A binary counter for counting UNIX and other time system is included. [BIN mode]
- An automatic leap year correction function is included (automatically corrected years are within 01 to 99) and a leap second correction method is provided. [BCD mode]
- 1/1024-second counter values can be read or written.
- A clocking buffer is included allowing access to the clock/calendar counter data in any timing regardless of the counter operation.

Figure 3.11 shows the configuration of the counters.



The block surrounded by a dotted line is the clocking buffer that performs batch read/write from/to the counters.
The values in parentheses represent the mirror register addresses.

Figure 3.11 Clock/Calendar Counter Configuration

Crystal oscillator circuit — This is a digital temperature compensated crystal oscillator circuit (DTCXO) that generates a 32.768 kHz clock.

Divider circuit — This circuit generates 1024 Hz signals by dividing the 32.768 kHz clock.

1/1024-second counter — This is a binary counter to count from 0 to 1023/1024 seconds using the 1024 Hz signal as the source clock. The initial value of the counter at the start of clocking can be set by writing the value directly to this counter or can be cleared to 0 by writing second counter setting data to Register SEC. This counter also allows a time adjustment during clocking period in 1/1024-second units by setting the time offset value to be adjusted to Registers OFS_SUBSEC_H and L. This counter stops counting operation by setting the TSTP_INTE.STOP bit to 1.

Second counter — This is a BCD counter to count seconds from 0 to 59 using the 1 Hz signal as the source clock. A time update interrupt can be generated when the second value in this counter is updated. The counter value can be set and read through Register SEC or SEC_MIR (Address 0x00 or 0x12).

Minute counter — This is a BCD counter to count minutes from 0 to 59 using the second counter overflow signal as the source clock. A time update interrupt can be generated when the minute value in this counter is updated. The counter value can be set and read through Register MIN or MIN_MIR (Address 0x01 or 0x13).

Hour counter

This is a BCD counter to count hours from 0 to 23 using the minute counter overflow signal as the source clock (supports 24-hour system only). A time update interrupt can be generated when the hour value in this counter is updated. The counter value can be set and read through Register HOUR or HOUR_MIR (Address 0x02 or 0x14).

Day counter

This is a BCD counter to count days from 1 to 28, 29, 30, or 31 according to the month and leap year conditions using the hour counter overflow signal as the source clock. The counter starts counting from 1 and 0 is skipped. The counter value can be set and read through Register DAY or DAY_MIR (Address 0x04 or 0x16).

Day-of-week counter

This is a 7-bit counter in which the bits are shifted interlocking with the day counter. Each of Bit 0 to Bit 6 corresponds to a day of the week. The bit assignment to the day of the week is optional. However, each bit must be assigned so that the bit shift direction will match with the order of the days of the week. The counter value can be set and read through Register WEEKDAY or WEEKDAY _MIR (Address 0x03 or 0x15).

Table 3.4 Example of Day-of-Week Assignment

Day of week	(Bit 7)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex. value
Sunday	-	0	0	0	0	0	0	1	0x01
Monday	-	0	0	0	0	0	1	0	0x02
Tuesday	-	0	0	0	0	1	0	0	0x04
Wednesday	-	0	0	0	1	0	0	0	0x08
Thursday	-	0	0	1	0	0	0	0	0x10
Friday	-	0	1	0	0	0	0	0	0x20
Saturday	-	1	0	0	0	0	0	0	0x40

Month counter

This is a BCD counter to count months from 1 to 12 using the day counter overflow signal as the source clock. The counter value is one from 1 to 12 and 0 is skipped. The counter value can be set and read through Register MONTH or MONTH_MIR (Address 0x05 or 0x17).

Year counter

This is a BCD counter to count years from 0 to 99 using the month counter overflow signal as the source clock. The counter value can be set and read through Register YEAR or YEAR_MIR (Address 0x06 or 0x18).

33-bit binary counter

This is a binary counter to count seconds such as a UNIX time using the 1 Hz signal as the source clock. When using it as a UNIX time counter, it can count up to 2242/03/16 12:56:31 based on the assumption that count 0 is the UNIX epoch time (1970/01/01 0:00:00 UTC). When using it as a NTP time stamp counter, it can count up to 2172/03/14 12:56:31 based on the assumption that count 0 is the NTP epoch time (1900/01/01 0:00:00 UTC).

* For the temperature compensation circuit, theoretical regulation circuit, and time update interrupt, refer to "*3.3 Temperature Compensation Function*," "*3.4 Theoretical Regulation Function*," and "*3.5 Time Update Interrupt Function*," respectively.

3.2.2 Operations

BCD Mode and BIN Mode

This RTC includes BCD counters that show the current date and time from seconds to years, and a binary counter (BIN counter) that counts the 1Hz clock to show the accumulated seconds since the epoch. These BCD and binary counters can be operated individually or simultaneously. However, the clocking buffer is common to both counters, so it is necessary to specify one of these counters to be read/written. When the CNTSEL.ACCBCD bit = 1 (default), the BCD counters are read/written. Hereinafter this state is referred to as BCD mode. When the CNTSEL.ACCBCD bit = 0, the binary counter is read/written and this state is referred to as BIN mode.

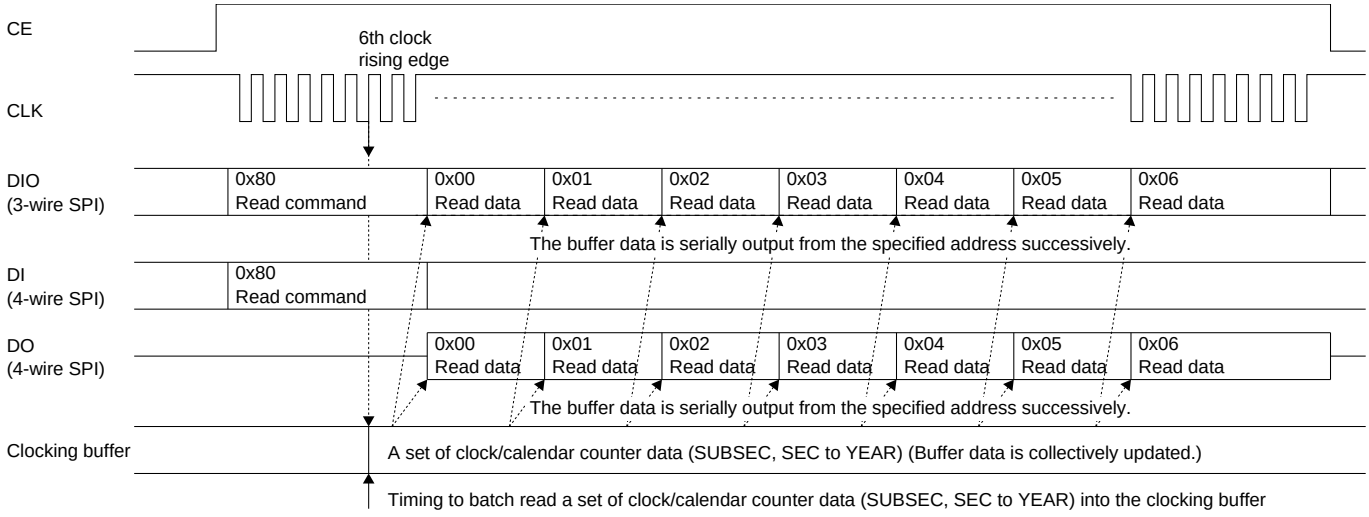
Accessing Clock/Calendar Counter through Clocking Buffer

The clock/calendar counters (1/1024-second, second, minute, hour, day-of-week, day, month, and year counters) are batch read/written into/from the clocking buffer. The host accesses the clocking buffer through Registers SEC to YEAR (Addresses 0x00 to 0x06), which allow reading/writing clock/calendar information in 1-second units, or Registers SUBSEC_L to YEAR_MIR (Addresses 0x10 to 0x18), which allow reading/writing information in 1/1024-second units. The clocking buffer accesses all the clock/calendar counters simultaneously to read/write their information that occupies multiple addresses. This allows reading/writing accurate time information. Furthermore, the conflict between the clocking buffer operation and a time update according to the internal 32.768 kHz clock is automatically arbitrated. Thus, the host can access the clocking buffer at any time.

The timings of the batch write from the clocking buffer to the clock/calendar counters and the batch read in reverse direction depend on the host interface as described below.

In the model with an SPI interface, the information written in the clocking buffer is collectively loaded to the clock/calendar counters at the falling edge of the CE signal. On the other hand, the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of the 6th clock within a clock/calendar read command after the CE signal has risen.

Clock/calendar counter read by SPI model (continuous register read from SEC to YEAR)



Clock/calendar counter write by SPI model (continuous register write from SEC to YEAR)

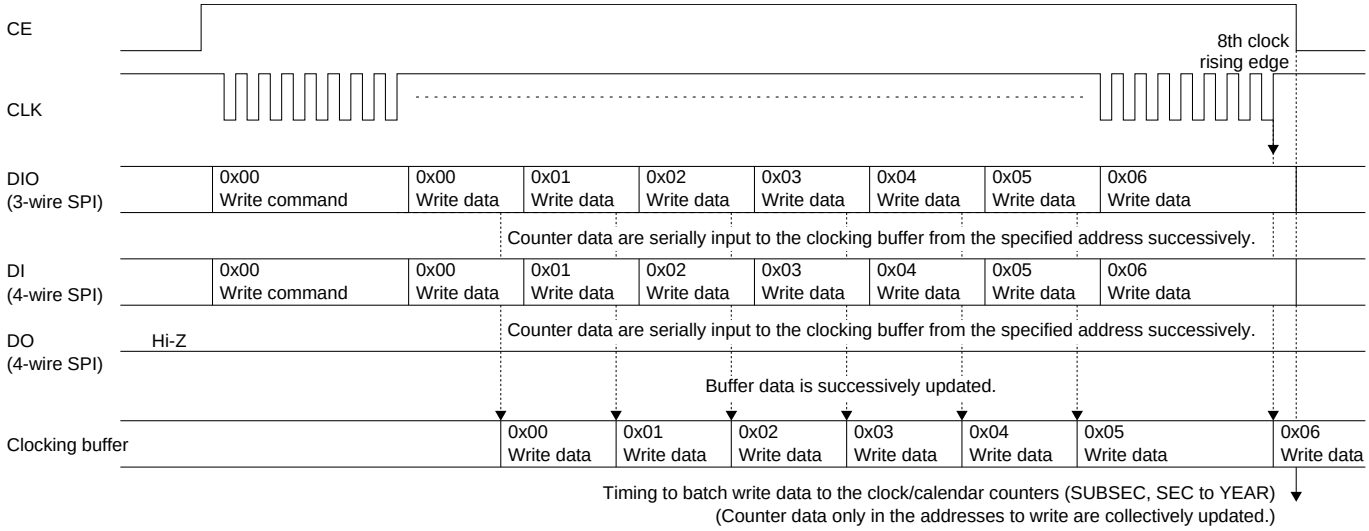
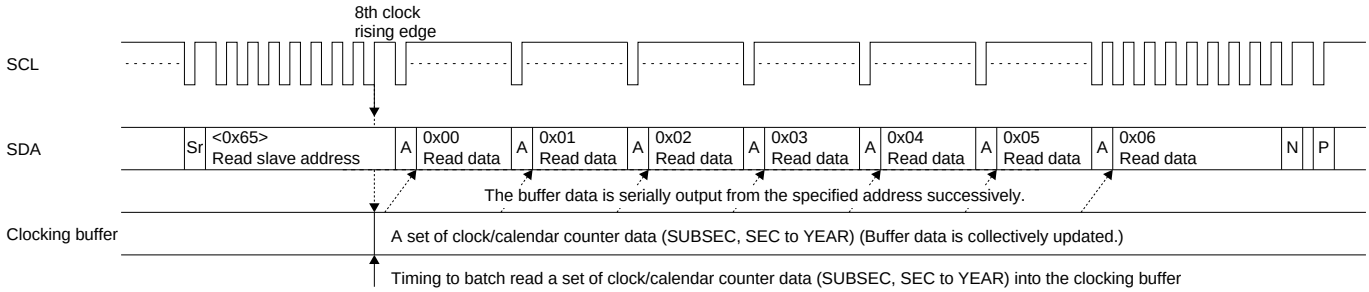


Figure 3.12 SPI Interface Clock/Calendar Counters Access Timing

In the model with an I²C-Bus interface, the information written in the clocking buffer is collectively loaded to the clock/calendar counters when a STOP or Repeated START condition has been received. On the other hand, the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of SCL while an ACK is being sent after the 7-bit slave address with the 8th bit set to 1 (read) have been received.

Clock/calendar counter read by I²C-Bus model (continuous register read from SEC to YEAR)



Clock/calendar counter write by I²C-Bus model (continuous register write from SEC to YEAR)

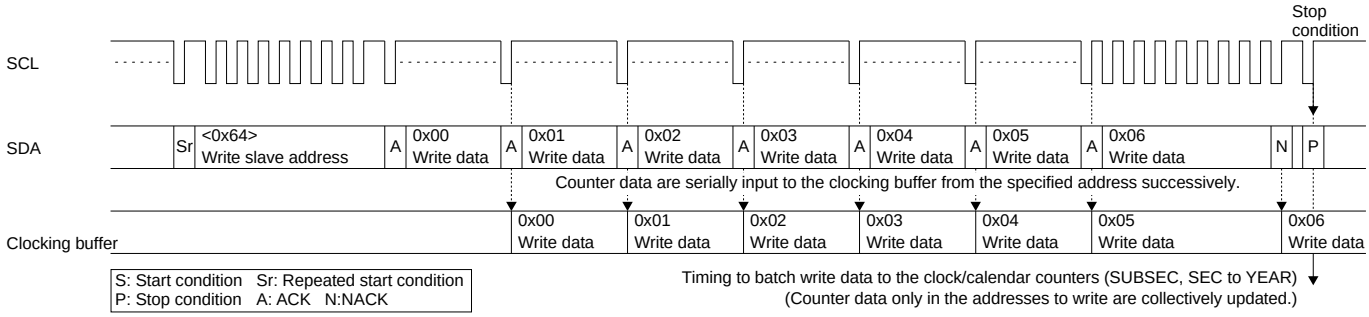


Figure 3.13 I²C-Bus Interface Clock/Calendar Counters Access Timing

Therefore, when writing or reading the clock/calendar data, perform continuous access for the required number of bytes using the automatic address increment function regardless of the interface included. Note that one continuous access for multiple bytes must be completed within 1 second in the model with an I²C-Bus interface, as it has a timeout function.

Initial Setting and Starting Clock/Calendar

There are two methods for the clock/calendar initial settings: setting the clock/calendar in 1-second units and setting in 1/1024-second units. When setting in 1-second units, write the clock/calendar counter initial values to Register SEC (Address 0x00) through Register YEAR (Address 0x06). When setting in 1/1024-second unit, write the initial values to Register SUBSC_L (Address 0x10) through Register YEAR_MIR (Address 0x18).

There are two methods to start clocking: terminating the communication by the host and clearing the TSTP_INTE.STOP bit by the host. Both methods have no difference in the time accuracy.
The following shows the procedure to set the time and to start the clock/calendar counters. The examples shown below are procedures when using the RTC by selecting either BCD mode or BIN mode.

Example: To set the clock/calendar in 1-second units and to start clocking at the end of communication when using in BCD mode

1. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 1. (Select BCD mode)
   - Set the CNTSEL.BINCNTEN bit to 0. (Disable BIN counter)
   - Set the CNTSEL.BCDCNTEN bit to 1. (Enable BCD counters)
2. Set a time and date to the following registers:
   - Register SEC (Second)
   - Register MIN (Minute)
   - Register HOUR (Hour)
   - Register WEEKDAY (Day of week)
   - Register DAY (Day)
   - Register MONTH (Month)
   - Register YEAR (Year)
3. Clocking starts when the continuous writing in Step 2 has completed (at the falling edge of the CE signal in the model with an SPI interface or when a STOP condition or a Repeated START condition has received in the model with an I^2C-Bus interface).

4a. <When time update interrupts are used>
   - Configure the TCTL.USEL0 and UPDISEL.USEL1 bits. (Set time update interrupt condition)
   - Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
   - Write 0 to the TSTP_INTE.UIE bit. (Negate /INT output)
   - Write 1 to the TSTP_INTE.UIE bit. (Enable time update interrupt)

4b. <When time update interrupts are not used>
   - Set both the TCTL.USEL0 and UPDISEL.USEL1 bits to 0. (Disable time update interrupt condition)
   - Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
   - Write 0 to the TSTP_INTE.UIE bit. (Negate /INT output, disable output)

Example: To set the clock/calendar in 1-second units and to start clocking by clearing the TSTP_INTE.STOP bit when using in BCD mode

1. Write 1 to the TSTP_INTE.STOP bit. (Stop clock/calendar counters)
2. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 1. (Select BCD mode)
   - Set the CNTSEL.BINCNTEN bit to 0. (Disable BIN counter)
   - Set the CNTSEL.BCDCNTEN bit to 1. (Enable BCD counters)
3. Set a time and date to the following registers:
   - Register SEC (Second)
   - Register MIN (Minute)
   - Register HOUR (Hour)
   - Register WEEKDAY (Day of week)
   - Register DAY (Day)
   - Register MONTH (Month)
   - Register YEAR (Year)

4a. <When time update interrupts are used>
- Configure the TCTL.USEL0 and UPDISEL.USEL1 bits. (Set time update interrupt condition)
- Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
- Write 0 to the TSTP_INTE.UIE bit. (Negate /INT output)
- Write 1 to the TSTP_INTE.UIE bit. (Enable time update interrupt)

4b. <When time update interrupts are not used>
- Set both the TCTL.USEL0 and UPDISEL.USEL1 bits to 0. (Disable time update interrupt condition)
- Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
- Write 0 to the TSTP_INTE.UIE bit. (Negate /INT output, disable output)

5. Write 0 to the TSTP_INTE.STOP bit at the time set in Step 3. (Start clock/calendar counters)

6. Clocking starts at the rising edge of the clock for writing Bit 0 (STOP bit) of Register TSTP_INTE in the model with an SPI interface or at the rising edge of the SCL for writing Bit 0 (STOP bit) of Register TSTP_INTE in the model with an I^2C-Bus interface.

Note: In BCD mode, rewriting Register SEC at Address 0x00 clears the sub-second counter (1/1024-second counter) to 0. For example, when the second counter is frequently read and written with a read-modify-write operation, time errors caused by clearing the counter are accumulated and a long delay will occur as a result.
Example: If a read-modify-write operation is performed to the second counter at 9.9 seconds, the counters will be reset to 9.0 seconds.

Rewriting Register SEC_MIR at Address 0x12 or rewriting in BIN mode does not clears the sub-second counter to 0.

Example: To set the clock/calendar in 1/1024-second units and to start clocking at the end of communication when using in BIN mode

1. Configure the following CNTSEL register bits:
- Set the CNTSEL.ACCBCD bit to 0. (Select BIN mode)
- Set the CNTSEL.BINCNTEN bit to 1. (Enable BIN counter)
- Set the CNTSEL.BCDCNTEN bit to 0. (Disable BCD counters)

2. Set the number of seconds since the epoch to Registers SUBSEC_L, SUBSEC_H, and SEC_BIN0 to SEC_BIN4.

* Data should be written continuously using the address auto-increment function.

3. Clocking starts when the continuous writing in Step 2 has completed (at the falling edge of the CE signal in the model with an SPI interface or when a STOP condition or a Repeated START condition has received in the model with an I^2C-Bus interface).

4. Disable time update and alarm interrupts.
- Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
- Set all the ALM_***.*ALM_H/L bits to 1. (Set invalid alarm date and time)
- Write 0 to the INTF.AF bit. (Clear alarm interrupt flag)
- Set both the TCTL.USEL0 and UPDISEL.USEL1 bits to 0. (Disable time update interrupt condition)
- Write 0 to the TSTP_INTE.UIE bit. (Disable time update interrupt)
- Write 0 to the TSTP_INTE.AIE bit. (Disable alarm interrupt)

* When the BCD counters are disabled, time update and alarm interrupts cannot be used.

Example: To set the clock/calendar in 1/1024-second units and to start clocking by clearing the TSTP_INTE.STOP bit when using in BIN mode

1. Write 1 to the TSTP_INTE.STOP bit. (Stop clock/calendar counters)

2. Configure the following CNTSEL register bits:
- Set the CNTSEL.ACCBCD bit to 0. (Select BIN mode)
- Set the CNTSEL.BINCNTEN bit to 1. (Enable BIN counter)
- Set the CNTSEL.BCDCNTEN bit to 0. (Disable BCD counters)

3. Set the number of seconds since the epoch to Registers SUBSEC_L, SUBSEC_H, and SEC_BIN0 to SEC_BIN4.

   * Data should be written continuously using the address auto-increment function.

4. Disable time update and alarm interrupts.
   - Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
   - Set all the ALM_***.*ALM_H/L bits to 1. (Set invalid alarm date and time)
   - Write 0 to the INTF.AF bit. (Clear alarm interrupt flag)
   - Set both the TCTL.USEL0 and UPDISEL.USEL1 bits to 0. (Disable time update interrupt condition)
   - Write 0 to the TSTP_INTE.UIE bit. (Disable time update interrupt)
   - Write 0 to the TSTP_INTE.AIE bit. (Disable alarm interrupt)

   * When the BCD counters are disabled, time update and alarm interrupts cannot be used.

5. Write 0 to the TSTP_INTE.STOP bit. (Start clock/calendar counters)

6. Clocking starts at the rising edge of the clock for writing Bit 0 (STOP bit) of Register TSTP_INTE in the model with an SPI interface or at the rising edge of the SCL for writing Bit 0 (STOP bit) of Register TSTP_INTE in the model with an I^2C-Bus interface.

Reading Clock/Calendar Data

The clock/calendar information in 1-second units should be continuously read from Register SEC (Address 0x0) to Register YEAR (Address 0x06) or the information in 1/1024-second units should be continuously read from Register SUBSEC_L (Address 0x10) to Register YEAR_MIR (Address 0x18). In either case, the read address range can be limited to a required part of the clock/calendar information.
When the BCD mode counters and BIN mode counter are both enabled, either one can be selected for reading the clocking data in advance.

BCD mode (reading in 1-second units)

1. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 1. (Select BCD mode)
   - Retain the current settings of the CNTSEL.BINCNTEN and CNTSEL.BCDCNTEN bits (clocking is continued).

2. Read the required register range continuously.
   (The following is an example for reading a complete set of counter data.)
   - Register SEC or SEC_MIR (Address 0x00 or 0x12) (Second)
   - Register MIN or MIN_MIR (Address 0x01 or 0x13) (Minute)
   - Register HOUR or HOUR_MIR (Address 0x02 or 0x14) (Hour)
   - Register WEEKDAY or WEEKDAY_MIR (Address 0x03 or 0x15) (Day of week)
   - Register DAY or DAY_MIR (Address 0x04 or 0x16) (Day)
   - Register MONTH or MONTH_MIR (Address 0x05 or 0x17) (Month)
   - Register YEAR or YEAR_MIR (Address 0x06 or 0x18) (Year)

BCD mode (reading in 1/1024-second units)

1. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 1. (Select BCD mode)
   - Retain the current settings of the CNTSEL.BINCNTEN and CNTSEL.BCDCNTEN bits (clocking is continued).

2. Read the required register range continuously.
   (The following is an example for reading a complete set of counter data.)
   - Registers SUB_SEC_L and SUN_SEC_H (Addresses 0x10 and 0x11) (1/1024-second counter data)
   - Register SEC_MIR (Address 0x12) (Second)
   - Register MIN_MIR (Address 0x13) (Minute)
   - Register HOUR_MIR (Address 0x14) (Hour)
   - Register WEEKDAY_MIR (Address 0x15) (Day of week)
   - Register DAY_MIR (Address 0x16) (Day)
   - Register MONTH_MIR (Address 0x17) (Month)
   - Register YEAR_MIR (Address 0x18) (Year)

BIN mode (reading in 1-second units)

1. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 0. (Select BIN mode)
   - Retain the current settings of the CNTSEL.BINCNTEN and CNTSEL.BCDCNTEN bits (clocking is continued).
2. Read the required register range continuously.
   (The following is an example for reading a complete set of counter data.)
   - Registers SEC_BIN0 to SEC_BIN4 (Addresses 0x12 to 0x16) (Binary second value[32:0] since the epoch)

BIN mode (reading in 1/1024-second units)

1. Configure the following CNTSEL register bits:
   - Set the CNTSEL.ACCBCD bit to 0. (Select BIN mode)
   - Retain the current settings of the CNTSEL.BINCNTEN and CNTSEL.BCDCNTEN bits (clocking is continued).
2. Read the required register range continuously.
   (The following is an example for reading a complete set of counter data.)
   - Registers SUB_SEC_L and SUB_SEC_H (Addresses 0x10 and 0x11) (1/1024-second counter binary value[9:0] since the epoch)
   - Registers SEC_BIN0 to SEC_BIN4 (Addresses 0x12 to 0x16) (Binary second value[32:0] since the epoch)

In the model with an SPI interface, all the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of the 6th clock within a clock/calendar read command after the CE signal has risen. The clock/calendar information loaded into the clocking buffer should be read continuously from Register SEC (Address 0x0) to Register YEAR (Address 0x06) or from Register SUBSEC_L (Address 0x10) to Register YEAR_MIR (Address 0x18) by the host.

In the model with an I^2C-Bus interface, the host first writes the read area start address, either Register SEC (Address 0x0) or Register SUBSEC_L (Address 0x10), then writes the 7-bit slave address with the 8th bit set to 1 (read). When this data is received, the RA8000CE sends an ACK back to the host and reads all the clock/calendar values simultaneously into the clocking buffer at the rising edge of the SCL input while an ACK is being sent. After that, the host continuously reads the buffered clock/calendar information.

When reading clock/calendar data, do not stop the clock/calendars by writing 1 to the TSTP_INTE.STOP bit, as it increases time error.

Reading/Writing 1/1024-Second Data

The RA4000CE/RA8000CE provides the SUBSEC_L.SUBSEC[1:0] and SUBSEC_H.SUBSEC[9:2] bits to read/write the 1/1024-second counter value. The table below shows the relationship between the bits and count values.

Table 3.5 SUBSEC[9:0] bits

Bit	SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2	SUBSEC1	SUBSEC0
Count value (1024 Hz cycle)	512	256	128	64	32	16	8	4	2	1

This counter is assigned to Addresses 0x10 (Register SUBSEC_L) and 0x11 (Register SUBSEC_H). To obtain or modify 1/1024-second data, read from or write to these two addresses successively. The clock/calendar counter data can also be read/written continuously by accessing Addresses 0x12 to 0x18 following these two addresses.

1/1024-Second Offset Time Adjustment

The 1/1024 binary counter can be set by writing a 1023 count to 1 count data directly to the Registers SUBSEC_L and SUBSEC_H. However, a time difference may occur between the sub-second data read from these registers and the clocking data in the host device. To correct this time difference, the RA4000CE/RA8000CE has an offset time adjustment function (hereinafter referred to offset processing). The following shows the usage:

1. Adjust the time in the BCD or BIN counter so that the time error will be less than one second.
2. Determine the sub-second data offset value (to be added/subtracted to/from data) by converting the difference between the sub-second data read from this RTC and the clocking data managed by the host into a 2's complement (data length = 11 bits).
3. Check if the OFS_SUBSEC_L.OFSFIN bit = 1 (ready for offset processing).
4. Write Bit 10 of the 11-bit offset value obtained in Step2 to the OFS_SUBSEC_H.OFS_SUBSEC[10] bit and Bit 9 to Bit 0 to the OFS_SUBSEC_H.OFS_SUBSEC[9:5] and OFS_SUBSEC_L.OFS_SUBSEC[4:0] bits.
5. Write 1 to the OFS_SUBSEC_L.OFSEN bit. (Start offset processing)

   The offset value will be reflected to the 1/1024-second counter when the second counter is updated immediately after this writing. This processing is performed only once and will not be performed at the subsequent updates of the second counter.
6. Check that the OFS_SUBSEC_L.OFSFIN bit reverts to 1 from 0 (offset processing completed).

   The OFS_SUBSEC_L.OFSFIN bit is cleared by writing 1 to the OFS_SUBSEC_L.OFSEN bit and is set to 1 upon completion of the offset processing.

Table 3.6 shows the relationship between the offset values and the amount of time adjustment.

Table 3.6 Offset Value and Amount of Time Adjustment

Offset value *		1/1024-second counter correction value	Offset processing result
0x3FF	0b011 1111 1111	Current value + 1023	Gains 1023/1024 seconds.
0x3FE	0b011 1111 1110	Current value + 1022	Gains 1022/1024 seconds.
:	:	:	:
0x003	0b000 0000 0011	Current value + 3	Gains 3/1024 seconds.
0x002	0b000 0000 0010	Current value + 2	Gains 2/1024 seconds.
0x001	0b000 0000 0001	Current value + 1	Gains 1/1024 seconds.
0x000	0b000 0000 0000	Current value + 0	No correction
0x7FF	0b111 1111 1111	Current value - 1	Loses 1/1024 seconds.
0x7FE	0b111 1111 1110	Current value - 2	Loses 2/1024 seconds.
0x7FD	0b111 1111 1101	Current value - 3	Loses 3/1024 seconds.
:	:	:	:
0x402	0b100 0000 0010	Current value - 1022	Loses 1022/1024 seconds.
0x401	0b100 0000 0001	Current value - 1023	Loses 1023/1024 seconds.
0x400	0b100 0000 0000	Cannot be set. (Prohibited)	–

* Offset value (11 bits) = {OFS_SUBSEC[10], OFS_SUBSEC[9:5], OFS_SUBSEC[4:0]}

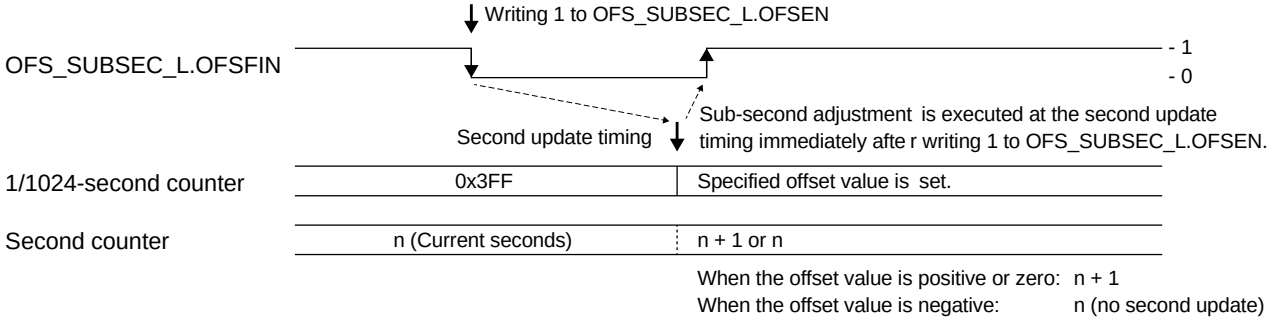


Figure 3.14 Offset Processing Timing

Clock/Calendar Counter Stop Procedure

To stop the clock/calendar counters, write 1 to the TSTP_INTE.STOP bit.
Setting the TSTP_INTE.STOP bit stops the1/1024-second counter, BCD counters (second, minute, hour, day of week, day, month, and year), and binary counter.

Leap Year Determination

In BCD mode, the RA4000CE/RA8000CE determines the years divisible by 4 as leap years, and others as common years. The count range of the day counter is automatically reconfigured in February.
Note that software must change the number of days in February as common years in 2100, 2200, and 2300 A.D.

Leap Second Correction Procedure

In BCD mode, a leap second can be inserted by writing 0x60 to Register SEC_MIR (Address 0x12). This operation must be performed between 00 seconds and 01 second at the time in which a leap second will be inserted.
The second counter goes to 60 seconds by writing 0x60 and it is updated to 00 seconds from 60 seconds at the second update timing immediately after the writing. The Register SEC or SEC_MIR (Address 0x00 or 0x12) is read as 60 seconds from writing 0x60 to it being updated to 00 seconds. The second counter then performs normal counting operation from 00 seconds to 59 seconds.

Note: Be aware that writing 0x60 to Register SEC (Address 0x00) resets the 1/1024-second counter. Register SEC_MIR (Address 0x12) must be used for the leap second correction. Writing 0x60 to Register SEC_MIR (Address 0x12) except for between 00 seconds and 01 second is prohibited.

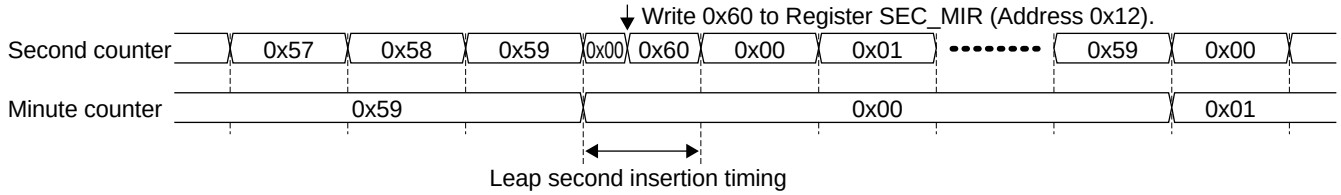


Figure 3.15 Leap Second Insertion Timing

3.3 Temperature Compensation Function

The RA4000CE/RA8000CE includes a high-precision temperature compensation circuit. Seiko Epson records an oscillation frequency correction value that depends on the embedded temperature sensor characteristics to the internal memory of each RA4000CE/RA8000CE individually at shipping inspection. Based on this value, the temperature compensation circuit compensates the oscillation frequency fluctuation caused by temperature change.

3.3.1 Operations

Setting Temperature Compensation Interval

The temperature compensation circuit always operates if the power supply voltage is within the range of the temperature compensation operable voltage (V_{TMP}). To reduce current consumption, the temperature sensor measurement operation is performed intermittently. The execution interval can be set using the TSTP_INTE.CSEL[1:0] bits as shown in Table 3.7.

Table 3.7 Temperature Compensation Data Update Interval

TSTP_INTE.CSEL[1:0]	Update interval
0b00	0.5 seconds
0b01	2.0 seconds (default)
0b10	10.0 seconds
0b11	30.0 seconds

The temperature compensation circuit measures operating temperature using the embedded temperature sensor and suppresses frequency fluctuation according to the measured temperature.
In an environment with a rapid ambient temperature change, selecting a short temperature compensation data update interval can quickly follow a temperature change.
In an environment with a relatively slow ambient temperature change like a room, selecting a long temperature compensation data update interval can suppress current consumption.

The temperature compensation circuit cannot be disabled by a register operation. However, the temperature compensation update operation is suspended with the last captured temperature compensation data retained when the power supply voltage drops below the temperature compensation update stop detection voltage V_{DET2}. If the power supply voltage is restored to V_{TMP} or more after that, the temperature compensation update operation resumes. An event interrupt can be generated when a V_{DET2} voltage drop is detected (for more information, refer to "*3.11 Time Stamp Function*").

Temperature Compensation Operation Flag: VTMPLF flag (0x0E)

The VTMPLF flag is set to 1 when the power supply voltage drops below the temperature compensation update stop detection voltage (V_{DET2}). In this case, the temperature compensation circuit stops and the oscillation continues under the last frequency correction condition before being stopped. The VTMPLF flag is cleared by writing 0 after the power supply voltage has been restored to above V_{TMP}.

3.4 Theoretical Regulation Function

The RA4000CE/RA8000CE is equipped with a theoretical regulation function that corrects the gaining or losing of time using the divider circuit.

- Correction cycle: 32-second cycles (fixed)
- Correctable range: -243.186 ppm to +243.186 ppm
- Minimum correction resolution: 0.954 ppm

3.4.1 Operations

Theoretical Regulation Operation

The theoretical regulation function starts operating by setting the DIG_TRIM_L.DTRIMEN bit to 1 and corrects the time with the specified amount of regulation within 32 seconds as one cycle. The 32-second correction period contains 256 correction execution points in 125 ms intervals and the correction processing is executed at the correction execution points according to the correction value set to the 9 bits of the DIG_TRIM_H.DTRIM[8:1] and DIG_TRIM_L .DTRIM[0] bits (hereinafter simply referred to as DIG_TRIM_H/L.DTRIM[8:0] bits). The correction processing prolongs or shortens the one 16.384 kHz clock cycle time for one 32.768 kHz clock cycle in the dividing stage that generates the 16.384 clock.
Therefore, the minimum correction period is 1/32.768 kHz ÷ 32s × 1 time = 0.954 ppm.

Setting Correction Amount

The correction value of the oscillation frequency deviation (value to be set to the DIG_TRIM_H/L.DTRIM[8:0] bits) can be obtained in the two methods shown below.

(1) To obtain a correction amount for theoretical regulation from the measured internal oscillation frequency

Enable the FOUT pin to output a 32 kHz clock and measure its actual frequency using an external universal counter or other equipment. Calculate the correction value from the measured value as follows:

$$DTRIM[8:0] = round(-\frac{f - 32768}{32768 \times 0.954} \times 10^6) \qquad (-255 \sim +255)$$

f: Oscillation frequency of the embedded oscillator obtained by measuring the FOUT output [Hz]

The correction value calculated from the frequency deviation and the minimum correction resolution should be set to the DIG_TRIM_H/L.DTRIM[8:0] bits after converting into 2's complement value as shown in Table 3.8. The valid range of setting values are -255 to +255.

(2) To obtain a correction amount for theoretical regulation by getting cumulative count error for 1024 seconds from time stamp data (TIMESTAMP_SUBSEC_H/L.SUBSEC[9:0] bits, range within 0x3FF (1023 counts) to 0x000 (0 counts))

Input an external reference 1 Hz square wave (e.g. GSNN 1PPS time pulse) to an EVIN*n* pin and obtain two sub-second time stamp data in a 1024-second interval. Calculate the correction value from the difference value as follows:

DTRIM[8:0] = 0x200 - ΔSubSecCnt_1024s, ΔSubSecCnt_1024s = B(SubSec) - A(SubSec)

A(SubSec):Time stamp data (Bank 6, SUBSEC[9:0]*) obtained by the 1st 1PPS pulse
B(SubSec):Time stamp data (Bank 7, SUBSEC[9:0]*) obtained by the 1025th 1PPS pulse

* For the contents of the time stamp data and the obtaining method, refer to Figure 3.33 and "3.*11 Time Stamp Function*," respectively.

The range of the ΔSubSecCnt_1024s is -255 to +255.
Note that the correction value obtained by this method contains a measurement error for a maximum of one count = ±0.954 ppm.

Supposing that the measurement time is shortened from 1024 seconds to 32 seconds, the obtained difference value (0x200 - ΔSubSecCnt_1024s) can be used as the DTRIM[8:0] setting value by multiplying by 32. Although the minimum correction resolution becomes rough about 30.518 ppm (0.954 ppm × 32), the measurement time can be shortened. When this shortening method is used, the correction value contains a measurement error for a maximum of one count = ±30.518 ppm.

Table 3.8 lists examples of the correction amounts corresponding to the DIG_TRIM_H/L.DTRIM[8:0] bit settings.

Table 3.8 DIG_TRIM_H/L.DTRIM[8:0] Bit Settings and Correction Amount

DIG_TRIM_H/L.DTRIM[8:0] setting value (1 unit = 0.954 ppm)	Theoretical regulation result (Regulation amount in 32-second cycles)
0x0FF = +255	+243.186 ppm Clock gains.
0x0FE = +254	+242.232 ppm Clock gains.
:	:
0x003 = +3	+2.861 ppm Clock gains.
0x002 = +2	+1.907 ppm Clock gains.
0x001 = +1	+0.954 ppm Clock gains.
0x000 = ±0	No correction
0x1FF = -1	-0.954 ppm Clock loses.
0x1FE = -2	-1.907 ppm Clock loses.
0x1FD = -3	-2.861 ppm Clock loses.
:	:
0x102 = -254	-242.232 ppm Clock loses.
0x101 = -255	-243.186 ppm Clock loses.
0x100 (Setting prohibited)	–

Enabling Theoretical Regulation

The theoretical regulation operation starts by the following procedure:

1. Set the correction amount in the 2's complement to the 9 bits of the DIG_TRIM_H/L.DTRIM[8:0] bits.
2. Set the DIG_TRIM_L.DTRIMEN bit to 1. (Enable theoretical regulation)

Disabling Theoretical Regulation

Setting the DIG_TRIM_L.DTRIMEN bit to 0 immediately stops the theoretical regulation operation.

3.4.2 Influence of Theoretical Regulation to Other Functions

The theoretical regulation function does not affect the 32.768 kHz, note, however, that the following functions are influenced as they use a dividing clock of 16.384 kHz or less.

(1) FOUT function

- When 1024 Hz or 1 Hz is selected as the output clock, the clock cycle fluctuates up to ±0.954 ppm.
  However, the output clock cycle does not fluctuate when 1 Hz is selected as the output clock and the DIG_TRIM_H/L.DTRIM[8:0] bit setting value is a multiple of 32.
- When 32.768 kHz is selected as the output clock, the output clock cycle is not fluctuated.

(2) Wakeup timer function

- When 1024 Hz, 64 Hz, or 1 Hz is selected as the source clock, the clock cycle fluctuates up to ±0.954 ppm.

3.5 Time Update Interrupt Function

3.5.1 Overview

The RA4000CE/RA8000CE has a function to generate an interrupt at clock counter update timings. Its features are shown below.

- The interrupt timing can be selected from three update timings: every second, every minute, and every hour.
- The interrupt signal output from the /INT pin to the host is automatically cleared after a certain time.

Figure 3.16 shows the configuration of the time update interrupt circuit.

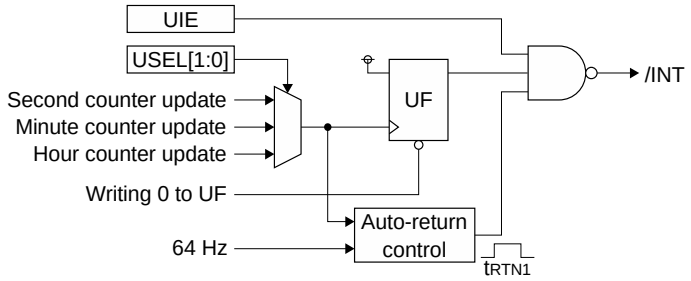


Figure 3.16 Configuration of Time Update Interrupt Circuit

Note: This function cannot operate normally if the BCD counters in the clock/calendar function are disabled. When using this function, the BCD counters must be enabled (CNTSEL.BCDCNTEN bit = 1).

3.5.2 Operations

Selecting Interrupt Period

Time update interrupts can be generated at the timing when a carry update occurs in one of the second, minute, and hour counters selected using the TCTL.USEL0 and UPDISEL.USEL1 bits (can generate an interrupt in 1-second, 1-minute, or 1-hour intervals, or can be disabled to generate interrupts). The interrupt signal output from the /INT pin to the host is automatically cleared after the prescribed time (t_{RTN1}) has elapsed.

Table 3.9 Selecting Time Update Interrupt Event

UPDISEL.USEL1	TCTL.USEL0	Interrupt event	/INT auto-return time (t_{RTN1})
0	0	Second counter update (default)	7.812 ms
0	1	Minute counter update	
1	0	Hour counter update	
1	1	No interrupt event	-

Interrupt Enabling/Disabling Procedure

The time update interrupt should be enabled/disabled as in the procedure below.

Enabling time update interrupts

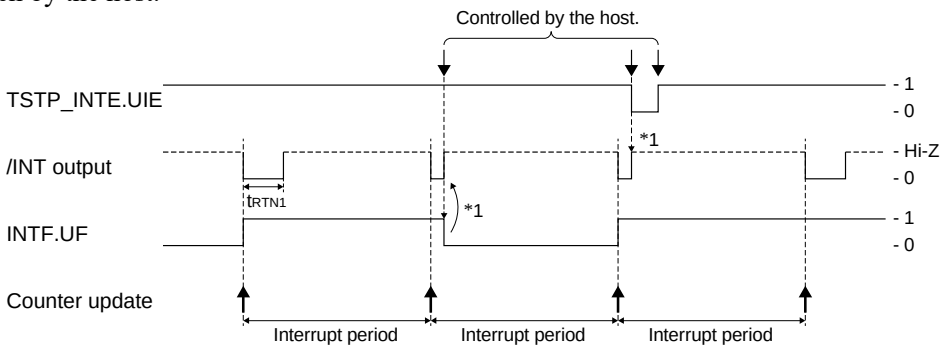
1. Write 0 to the TSTP_INTE.UIE bit. (Cancel /INT output)
2. Configure the TCTL.USEL0 and UPDISEL.USEL1 bits. (Select time update interrupt event)
3. Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
4. Write 1 to the TSTP_INTE.UIE bit. (Enable time update interrupt)

Disabling time update interrupts

1. Write 0 to the TSTP_INTE.UIE bit. (Cancel /INT output, disable output)
2. Write 0 to the INTF.UF bit. (Clear time update interrupt flag)

Interrupt Operations

When an interrupt generation timing selected via software is reached, INTF.UF bit is set to 1. If the TSTP_INTE.UIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. After that, the /INT pin goes into a Hi-Z state when 0 is written to the TSTP_INTE.UIE bit or automatically goes into a Hi-Z state after t_{RTN1} (7.812 ms) has elapsed from the beginning of a low output from the /INT pin. The INTF.UF bit is not cleared even if the /INT pin goes into a Hi-Z state after t_{RTN1} has elapsed from occurrence of an interrupt request. It is cleared when 0 is written by the host.



*1 Clearing the INTF.UF bit or TSTP_INTE.UIE bit by writing 0 puts the /INT pin into an open (Hi-Z) state without waiting t_{RTN1}.

Figure 3.17 Time Update Interrupt Timing Chart

3.6 Alarm Function

3.6.1 Overview

The following shows the features of the alarm function:

- Days of the week or a day, an hour, a minute, and a second can be combined to specify alarm times.
- Allows various alarm settings simply by combining date and time conditions arbitrarily, such as 10 A.M. every Friday and Saturday, and 7 P.M. on the 25th of every month.

Figure 3.18 shows the configuration of the alarm circuit.

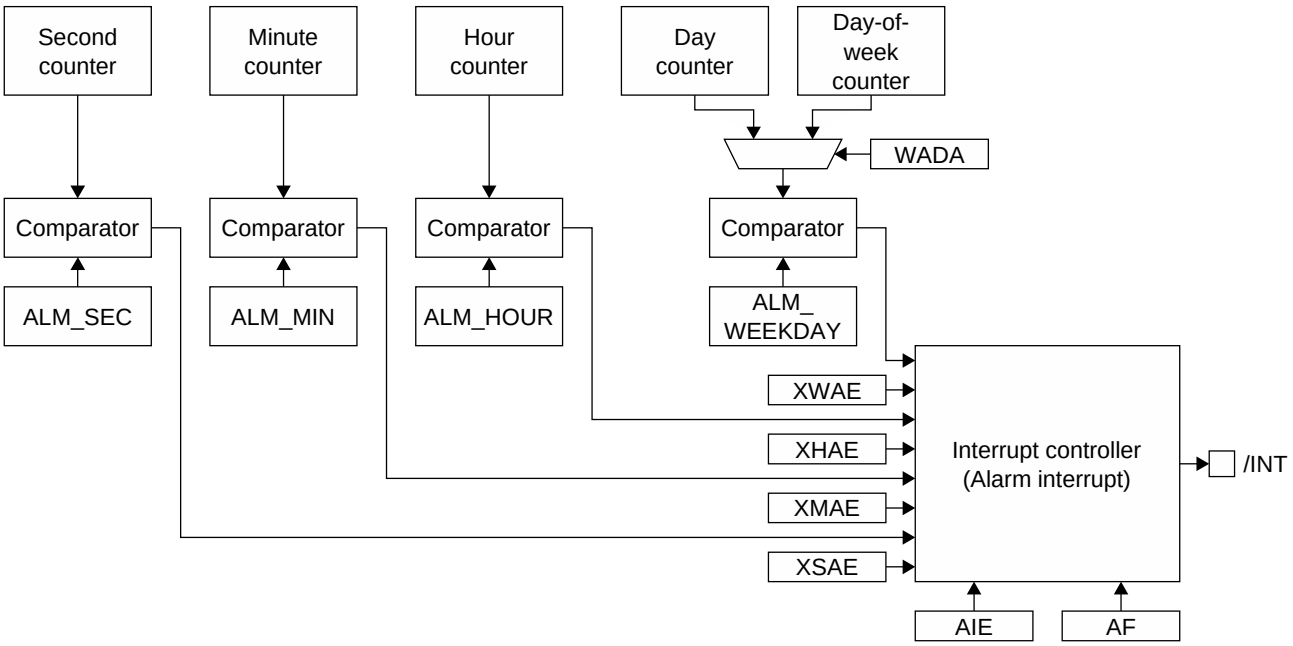


Figure 3.18 Configuration of Alarm Circuit

Note: When using this function, the BCD counters must be enabled (CNTSEL.BCDCNTEN bit = 1).

3.6.2 Operations

Alarm Setting Procedure

The following shows a procedure to set an alarm to generate an interrupt:

1. Write 0 to the TSTP_INTE.AIE bit. (Disable alarm interrupts)
2. Set the alarm second to Register ALM_SEC.
   - XSAE bit (Enable/disable alarm second)
   - SALM_H[2:0] bits (Specify 10-second digit)
   - SALM_L[3:0] bits (Specify 1-second digit)
3. Set the alarm minute to Register ALM_MIN (or ALM_MIN_MIR).
   - XMAE bit (Enable/disable alarm minute)
   - MALM_H[2:0] bits (Specify 10-minute digit)
   - MALM_L[3:0] bits (Specify 1-minute digit)
4. Set the alarm hour to Register ALM_HOUR (or ALM_HOUR_MIR).
   - XHAE bit (Enable/disable alarm hour)
   - HALM_H[1:0] bits (Specify 10-hour digit)
   - HALM_L[3:0] bits (Specify 1-hour digit)

5. Set the alarm day-of-week or alarm day to Register ALM_WEEKDAY (or ALM_WEEKDAY_MIR).
   - XWAE bit (Enable/disable alarm day-of-week/day)

   When specifying alarm day-of-week (TCTL.WADA bit = 0)
   - WKALM[6:0] bits (Specify days of week)

   These bits allow specification of more than one day a week, such as Monday to Friday.

   When specifying alarm day (TCTL.WADA bit = 1)
   - DALM_H[1:0] bits (Specify 10-day digit)
   - DALM_L[3:0] bits (Specify 1-day digit)
6. Set the TCTL.WADA bit. (Select day-of-week/day alarm)
7. Write 0 to the INTF.AF bit. (Clear alarm interrupt flag)
8. Write 1 to the TSTP_INTE.AIE bit. (Enable alarm interrupts)

* Setting the X*AE bit to 1 excludes its register setting from the alarm condition. For example, when ALM_WEEKDAY.XWAE bit = 1, day-of-week/day setting is disabled so that an alarm will occur at the specified time every day. However, if all the X*AE bits are set to 1, an alarm will occur every second.

Alarm Setting Examples

Alarm setting examples with day of the week specified (TCTL.WADA bit = 0)

Setting example 1

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	0	1	1	1	1	1	0	0x07	0x00	XSAE = 1

An alarm will occur repeatedly in one second intervals from 7:00:00 to 7:00:59 A.M., Monday to Friday every week.

Setting example 2

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	1	0	0	0	0	0	1	XHAE = 1	0x30	0x00

An alarm will occur at the 30-minute mark of every hour, Saturday and Sunday every week.

Setting example 3

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	1	1	1	1	1	1	1	0x18	0x59	0x30
1	X	X	X	X	X	X	X			

An alarm will occur at 6:59:30 P.M. every day.

Alarm setting examples with day specified (TCTL.WADA bit = 1)

Setting example 4

ALM_WEEKDAY (Day alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Hour alarm)	(Minute alarm)	(Second alarm)
0	X	0	0	0	0	0	1	0x07	XMAE = 1	XSAE = 1

An alarm will occur repeatedly in one second intervals from 7:00:00 to 7:00:59 A.M., on the first day of every month.

Setting example 5

ALM_WEEKDAY (Day alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Hour alarm)	(Minute alarm)	(Second alarm)
0	X	0	1	0	1	0	1	XHAE = 1	0x30	0x00

An alarm will occur at 30:00 every hour, on the 15th of every month.

Setting example 6

ALM_WEEKDAY (Day alarm)								ALM_HOUR (Hour alarm)	ALM_MIN (Minute alarm)	ALM_SEC (Second alarm)
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
1	X	X	X	X	X	X	X	0x18	0x59	0x30

An alarm will occur at 6:59:30 P.M. every day.

X: Don't care.

Alarm Interrupt

Figure 3.19 shows the configuration of the alarm interrupt circuit.

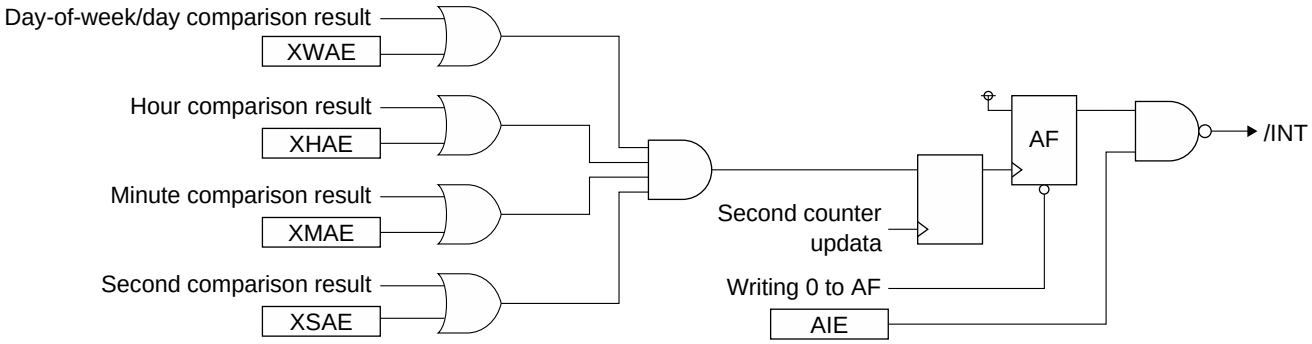
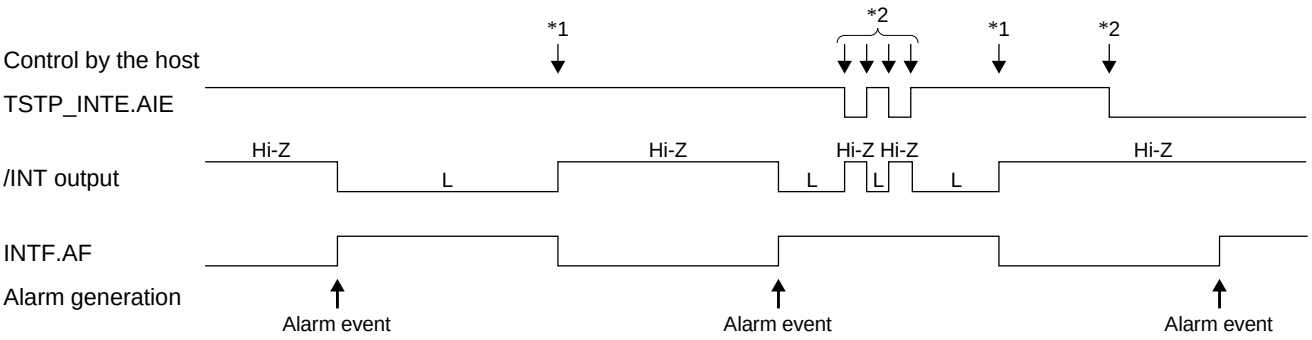


Figure 3.19 Configuration of Alarm Interrupt Circuit

Alarm interrupts can be generated when the time/calendar counters reach the date and time specified using Registers ALM_SEC, ALM_MIN, ALM_HOUR, and ALM_WEEKDAY.
The INTF.AF bit is set to 1 at the specified time and day of week/day. If the TSTP_INTE.AIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. The INTF.AF bit that has been set to 1 is cleared by writing 0. At the same time, the /INT pin goes into a Hi-Z state.



*1 Clearing the INTF.AF bit by writing 0 puts the /INT pin into an open (Hi-Z) state.
*2 Setting the TSTP_INTE.AIE bit to 0 puts the /INT pin into an open (Hi-Z) state regardless of the INTF.AF bit setting.

Figure 3.20 Alarm Interrupt Timing Chart

3.7 Wakeup Timer Function

3.7.1 Overview

The following shows the features of the wakeup timer function:

- The timer consists of a 24-bit resettable up/down counter.
- The source clock is selectable from 1024 Hz, 64 Hz, 1 Hz, 1/60 Hz, and an external clock (EVIN2 input).
- An interrupt can be generated in an optional cycle from 976 µs to 32 years.
- The interrupt output can also be assigned to the FOUT pin.
- Can be used as a watchdog timer.
- Can be used as an operating time integration meter.

Figure 3.21 shows the configuration of the wakeup timer.

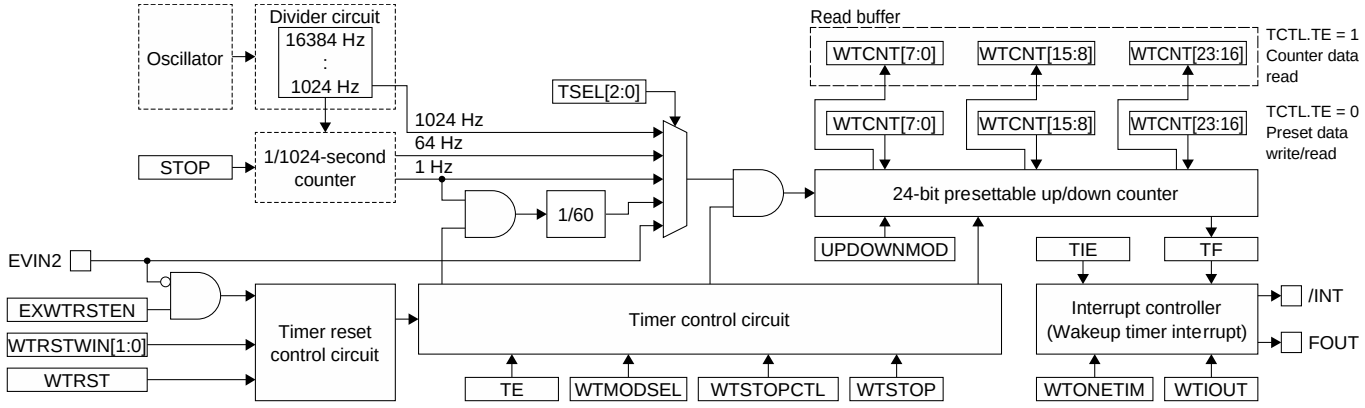


Figure 3.21 Configuration of Wakeup Timer

3.7.2 Operations

Source Clock

The source clock can be selected from the five clocks listed in Table 3.10 using the TCTL.TSEL[1:0] and WTICFG.TSEL2 bits.

Table 3.10 Wakeup Timer Source Clock Selection

WTICFG.TSEL2	TCTL.TSEL[1:0]	Source clock		/INT auto-return time (t_{RTN2}) *
		Frequency	Cycle	
0	0b00	1024 Hz	976 µs	488 µs
	0b01	64 Hz	15.625 ms	7.812 ms
	0b10	1 Hz	1 second	7.812 ms
	0b11	1/60 Hz	60 seconds	7.812 ms
1	–	EVIN2 pin input (external event)		No auto-return

* t_{RTN2} is the time after the /INT pin goes low until it is automatically placed into open (Hi-Z) state.

When EVIN2 pin input is specified as the wakeup timer source clock, input the clock to the EVIN2 pin. To use it as the count clock, the maximum clock frequency is 1024 Hz and the clock waveform must have a 488 µs or more H pulse width.

Note: When the WTICFG.TSEL2 bit = 1, the EVIN2 pin input signal is used as the wakeup timer source clock. In this case, the pull-up/down resistor setting is effective, however, the noise filter and input detection edge settings are ineffective.

Count-Up/Down Mode

The counter in this function has two count modes, Count-up mode and Count-down mode, and either one to be used is selected using the WTICFG.UPDOWNMOD bit.

WTICFG.UPDOWNMOD bit = 1: Count-up mode
WTICFG.UPDOWNMOD bit = 0: Count-down mode

Preset Data (wakeup timer interrupt period)

Preset data specifies the count upper limit value to determine the wakeup timer interrupt period. The wakeup timer generates an interrupt when the count value exceeds the preset data in Count-up mode or when the counter reaches 0 in Count-down mode. Write preset data to Registers WTCNT_L, WTCNT_M, and WTCNT_H when the TCTL.TE bit = 0 (timer disabled).

Notes:
- Be sure to avoid writing preset data to Registers WTCNT_L, WTCNT_M, and WTCNT_H while the timer is operating (TCTL.TE bit = 1).
- The preset data cannot be set to 0x000000. If 0x000000 is written to Registers WTCNT_L, WTCNT_M, and WTCNT_H, the wakeup timer cannot perform counting up/down and an interrupt does not occur.

Table 3.11 lists examples of wakeup timer interrupt periods according to combinations of the preset data and source clock settings.

Table 3.11 Examples of Wakeup Timer Interrupt Periods

Preset data	Source clock			
	1024 Hz TCTL.TSEL[1:0] = 0b00 WTICFG.TSEL2 = 0b0	64 Hz TCTL.TSEL[1:0] = 0b01 WTICFG.TSEL2 = 0b0	1 Hz TCTL.TSEL[1:0] = 0b10 WTICFG.TSEL2 = 0b0	1/60 Hz TCTL.TSEL[1:0] = 0b11 WTICFG.TSEL2 = 0b0
0	–	–	–	–
1	976 µs	15.625 ms	1 second	60 seconds
:	:	:	:	:
410 (0x00019A)	400.39 ms	6.406 seconds	410 seconds	410 minutes
:	:	:	:	:
3840 (0x000F00)	3.7500 seconds	60 seconds	3840 seconds	3840 minutes
:	:	:	:	:
4096 (0x001000)	4 seconds	64 seconds	4096 seconds	4096 minutes
:	:	:	:	:
16777215 (0xFFFFFF)	4.55 hours	72.81 hours	4660 hours	31.9 years

Counting Condition (only for the models with the /RST output function)

Setting the WTCTL.WTSTOPCTL bit to 1 enables the WTCTL.WTMODSEL bit setting to select whether the wakeup timer count operation will be performed only in Normal mode (while the reset output is cancelled) or Safe mode (while the reset signal is being output).

Table 3.12 Setting Wakeup Timer Counter Operation Condition in Normal Mode/Safe Mode

WTCTL.WTSTOPCTL	WTCTL.WTMODSEL	Counting condition
0	X	Enables counting in both Normal and Safe modes.
1	0	Enables counting in Normal mode (while the reset output is cancelled) only.
	1	Enables counting in Safe mode (while the reset signal is being output) only.

For example, when counting is enabled in Normal mode only, the counting stops when the RA4000CE/RA8000CE enters Safe mode. The RA4000CE/RA8000CE retains the counter value at this point and resumes counting from that value after returning to Normal mode again. This makes it possible to use the wakeup timer as an integrating meter that measures the operating time during Normal mode.

Wakeup Timer Setting Procedure

The following shows the procedure to set the wakeup timer to generate an interrupt:

1. Write 0 to the TCTL.TE bit. (Disable wakeup timer)
2. Write 0 to the TSTP_INTE.TIE bit. (Disable wakeup timer interrupts)
3. Configure the TCTL.TSEL[1:0] and WTICFG.TSEL2 bits. (Select source clock)
4. Configure Registers WTCNT_L, WTCNT_M, and WTCNT_H. (Set wakeup timer interrupt period)
5. Configure Register WTICFG. (Configure interrupt output)
   - WTONETIM bit (Set /INT auto-return function)
   - WTIOUT bit (Select interrupt output pin)
   - UPDOWNMOD bit (Select Count-up/down mode)
6. Configure Register WTCTL. (Set timer operating condition)
   - WTMODSEL and WTSTOPCTL bits (Select Normal/Safe mode operating condition)
   - Write 0 to the WTSTOP bit. (Cancel suspending)
7. Write 0 to the INTF.TF bit. (Clear wakeup timer interrupt flag)
8. Write 1 to the TSTP_INTE.TIE bit. (Enable wakeup timer interrupts)
9. Write 1 to the TCTL.TE bit. (Enable wakeup timer)

   This starts counting.

Starting Count

Count-up mode

The wakeup timer loads the initial value (1) to the counter and starts counting up when the TCTL.TE bit is set to 1. However, the counting starts in async with the source clock, so a maximum of one source clock cycle of delay occurs until the first counting up.

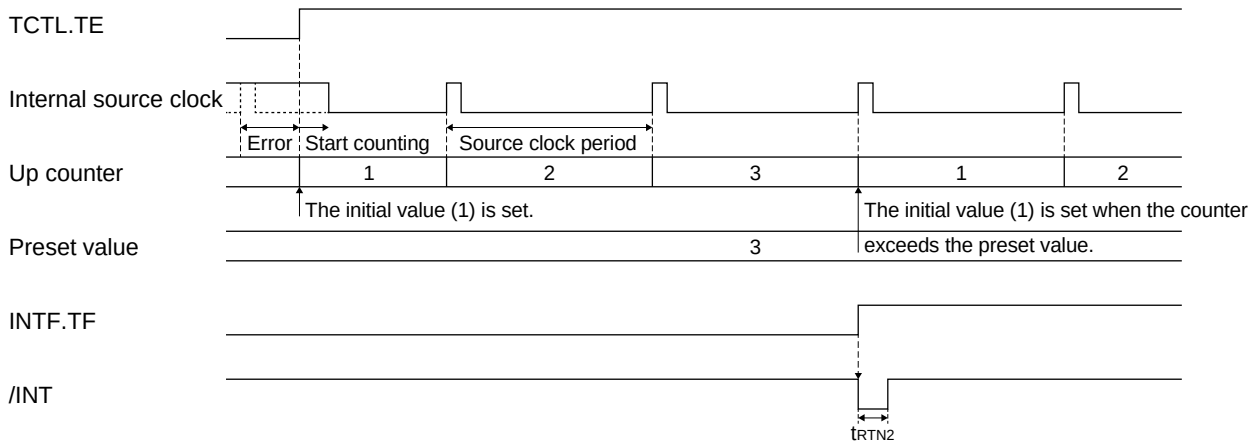


Figure 3.22 Wakeup Timer Count-Up Operation

When the counter exceeds the preset value by counting up, the initial value (1) is loaded to the counter and the counting continues.

Count-down mode

The wakeup timer presets the value stored in Registers WTCNT_L, WTCNT_M, and WTCNT_H and then starts counting down when the TCTL.TE bit is set to 1. However, the counting starts in async with the source clock, so a maximum of one source clock cycle of delay occurs until the first counting down.

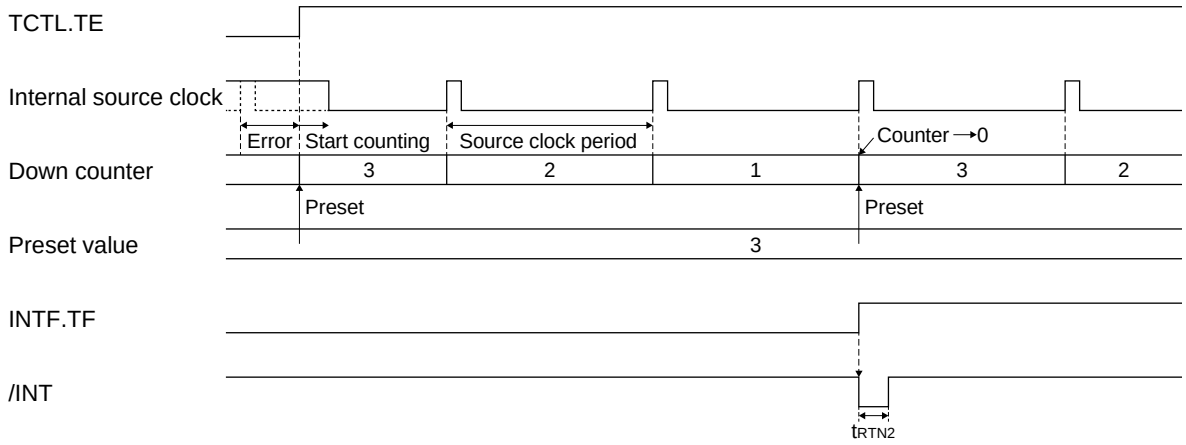


Figure 3.23 Wakeup Timer Count-Down Operation

When the counter reaches 0 by counting down, the value stored in Registers WTCNT_L, WTCNT_M, and WTCNT_H is loaded to the counter and the counting continues.

Figure 3.24 shows the count start timing after 1 is written to the TCTL.TE bit.

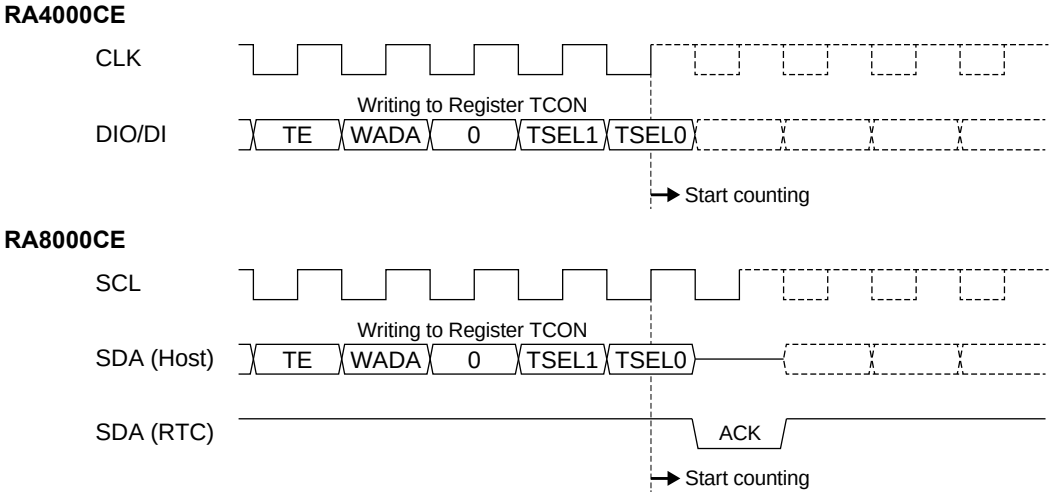


Figure 3.24 Wakeup Timer Count Start Timing

Suspension

To suspend the wakeup timer counting operation, write 1 to the WTCTL.WTSTOP bit. The wakeup timer stops with the counter value at that point retained. When 0 is written to the WTCTL.WTSTOP bit, the wakeup timer resumes counting from the retained value. This suspending/resuming is performed in async with the source clock, a same error as the time of starting occurs.

Note that the counter will not stop by the WTCTL.WTSTOP bit depending on the setting status of other bits. Table 3.13 shows the wakeup timer operating status according to the related control bit settings.

Table 3.13 Control of Wakeup Timer Operation

TCTL.TE	TSTP_INTE.STOP	WTCTL.WTSTOPCTL	WTCTL.WTSTOP	Operating status
1	0	0	0	Counting is in progress.
			1	Counting is suspended.
		1	X	The WTCTL.WTSTOP bit setting is disabled; setting it to 1 does not suspend counting.
	1	X	X	The counter stops. However, when the source clock = 1024 Hz or an external clock, the timer performs the same operation as when the TSTP_INTE.STOP bit = 0.
0	X	X	X	The counter is idle.

Reading Counter Data

When the TCTL.TE bit = 1

The counter data can be read from Registers WTCNT_L, WTCNT_M, and WTCNT_H while it is counting.

This counter has a read buffer similar to the clocking buffer for reading clock/calendar data, so the exact counter value can be read anytime even while the counter is operating.

In the model with an SPI interface, all the wakeup timer counter values are simultaneously read into the read buffer at the rising edge of the 6th clock within a wakeup timer counter read command after the CE signal has risen. The count information loaded into the read buffer should be read continuously from Register WTCNT_L, WTCNT_M, and WTCNT_H (Addresses 0x0A to 0x0C) by the host.

In the model with an I^2C-Bus interface, the host first writes the read area start address, Register WTCNT_L (Address 0x0A), then it writes the 7-bit slave address with the 8th bit set to 1 (read). When this data is received, the RA8000CE sends an ACK back to the host and reads all the wakeup timer counter values simultaneously into the read buffer at the rising edge of the SCL input while an ACK is being sent. After that, the host continuously reads the buffered count information.

When the TCTL.TE bit = 0

The wakeup timer preset value is read from Registers WTCNT_L, WTCNT_M, and WTCNT_H.

Resetting Counter

The wakeup timer has a function to reset the counter being operated by a register operation or an external signal input. When a reset is input to the wakeup timer, it loads the initial value (1 in Count-up mode or preset value in Count-down mode) to the counter and continues the counting operation. However, a wakeup timer interrupt does not occur at this time.

With this function, the wakeup timer can be used as a watchdog timer.

Reset by register operation

Writing 1 to the WTCTL.WTRST bit resets the counter being operated.

Reset by external signal input

Setting the WTCTL.EXWTRSTEN bit to 1 enables the external reset input. Input a high pulse having a 977 µs or more width as a reset signal to the EVIN2 pin.

When the WTCTL.EXWTRSTEN bit = 0, the counter is not reset even if a pulse is input from the EVIN2 pin.

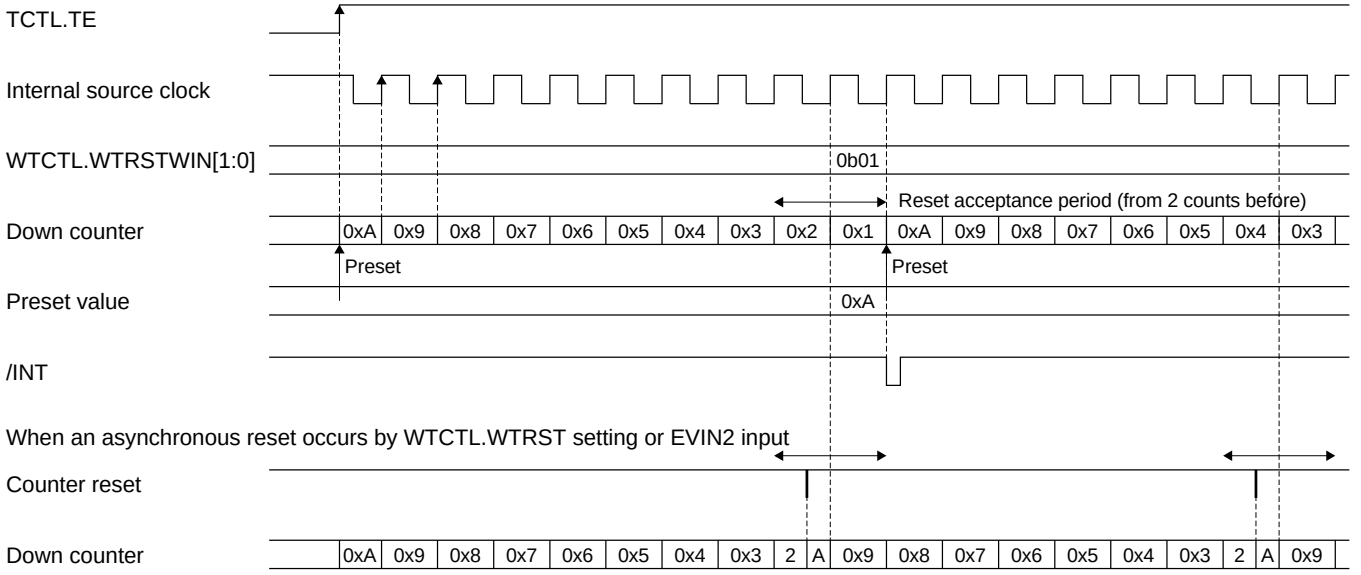
A reset by writing 1 to the WTCTL.WTRST bit takes effect regardless of how the WTCTL.EXWTRSTEN bit is set.

Reset window

The reset window restricts the acceptance of a counter reset in Count-down mode to within the period specified with the WTCTL.WTRSTWIN[1:0] bits as shown in Table 3.14. This setting is effective for both resets by register operation and external signal input. Note, however, that the preset value for the down counter must be larger than this acceptance period.

Table 3.14 Reset Window Settings

WTCTL.WTRSTWIN[1:0]	Reset acceptance period (Count-down mode)
0b00	Whole period (default)
0b01	Counter value = 2 to 1
0b10	Counter value = 16 to 1
0b11	Counter value = 64 to 1



* When Count-down mode and preset value = 0x00000A are set

Figure 3.25 Timer Reset Timing when Reset Window is Set (asynchronous timer reset timing)

Wakeup Timer Interrupt

Figure 3.26 shows the configuration of the wakeup timer interrupt circuit.

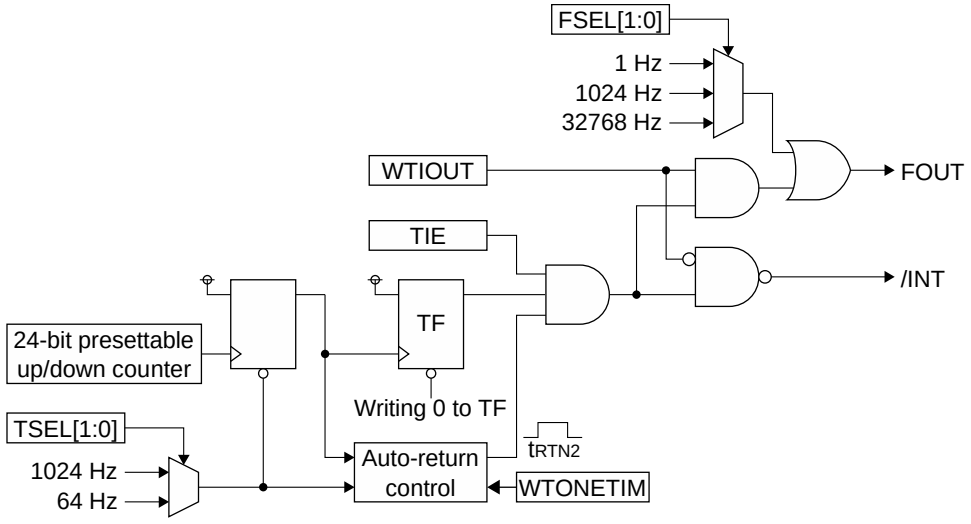
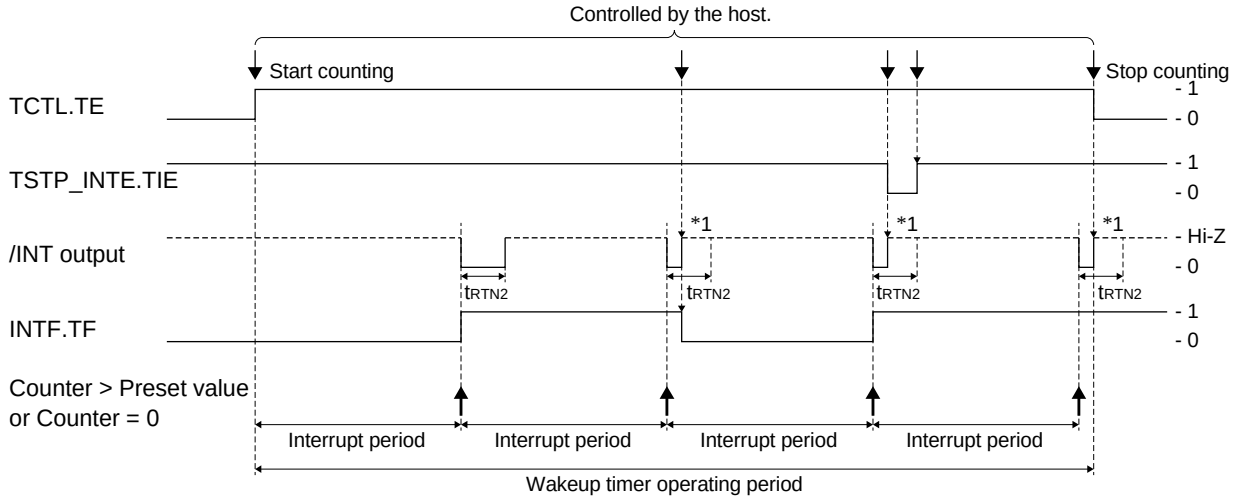


Figure 3.26 Configuration of Wakeup Timer Interrupt Circuit

Wakeup timer interrupts can be generated in the preset count cycle.
In Count-up mode, a wakeup timer interrupt occurs with the INTF.TF bit set to 1 as the moment the counter exceeds the preset value by counting up; in Count-down mode, it occurs as the moment the counter reaches 0 by counting down. If the TSTP_INTE.TIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host and returns into a Hi-Z state after the /INT auto-return time (t_{RTN2}, see Table 3.10) has elapsed. The /INT auto-return function can be disabled by setting the WTICFG.WTONETIM bit to 1.
Although the /INT pin automatically returns into a Hi-Z state, the INTF.TF bit that has been set retains 1 until 0 is written by the host. When 0 is written to the INTF.TF or TSTP_INTE.TIE bit, the /INT pin returns into a Hi-Z state regardless whether the /INT auto-return time has elapsed or not. When EVIN2 pin input is selected as the timer source clock, the /INT auto-return function is ineffective regardless of how the WTICFG.WTONETIM bit is set.



*1 Clearing the INTF.TF, TSTP_INTE.TIE, or TCTL.TE bits to 0 puts the /INT pin into an open (Hi-Z) state without waiting t_{RTN2}.

Figure 3.27 Wakeup Timer Interrupt Timing Chart

When the WTICFG.WTIOUT bit = 0, the wakeup timer interrupt request signal is NORed with other interrupt request signals and output from the /INT pin.
When the WTICFG.WTIOUT bit = 1, it is output from the FOUT pin in the model with the FOUT pin enabled.

Note: When the WTICFG.WTIOUT bit = 1, the wakeup timer interrupt request signal is NORed with the FOUT signal and output from the FOUT pin. To output the wakeup timer interrupt request signal only, set the TCTL.FSEL[1:0] bits to 0b11 to disable the FOUT output.

3.8 FOUT Output Function

3.8.1 Overview

The features of the FOUT output function are shown below.

- A clock generated in the RA4000CE/RA8000CE can be output externally.
- The output clock can be selected from 32.768 kHz, 1024 Hz, and 1 Hz.
- The FOUT output can be controlled using a register or an external input signal (FOE).

Figure 3.28 shows the configuration of the FOUT output circuit.

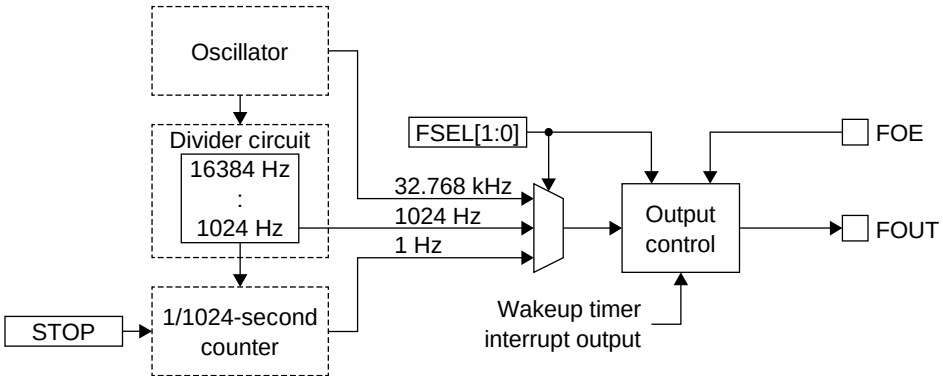


Figure 3.28 Configuration of FOUT Output Circuit

Note: The FOUT function is available only in the model with the FOUT pin. Also the FOUT control function using an external signal can be used only in the model with the FOE pin.

3.8.2 Operations

Initial Settings

Depending on the model option, the FOUT and FOE pins are shared with other functions. In this case, it may be necessary to switch the pin function for the FOUT output by setting a register as an initial setting. For more information, refer to "*0x38: WTICFG (Wakeup Timer Interrupt Configuration)*" in Section 4.1.

Controlling FOUT Output (when not using the FOE pin)

The FOUT output is disabled (Hi-Z) at power-on. The TCTL.FSEL[1:0] bits are used to enable or disable (Hi-Z) the FOUT output. Note that the TSTP_INTE.STOP bit setting affects the 1 Hz output setting.

Table 3.15 FOUT Output Selection

TSTP_INTE.STOP	TCTL.FSEL[1:0]	Output
0	0b00	32.768 kHz
	0b01	1024 Hz
	0b10	1 Hz
	0b11	Off (Hi-Z)
1	0b00	32.768 kHz
	0b01	1024 Hz
	0b10	Fixed at H or L
	0b11	Off (Hi-Z)

Controlling FOUT Output (when using the FOE pin)

In the model with the FOE pin, the FOUT output can be controlled using the FOE input signal. The output clock frequency should be selected using the TCTL.FSEL[1:0] bits (see Table 3.15).

While the FOE input signal is a high level, the FOUT signal with the frequency selected by setting the TCTL.FSEL[1:0] bits is output from the FOUT pin. While the FOE input signal is a low level, the FOUT pin goes into a Hi-Z state.

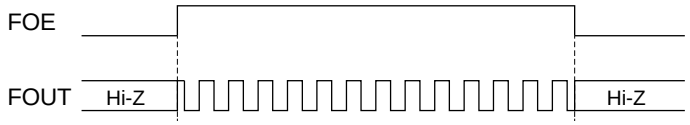


Figure 3.29 FOUT Output by FOE Control

Wakeup Timer Interrupt Signal Output from FOUT pin

If the clock output is not necessary, the FOUT pin can be used as the wakeup timer interrupt request signal output pin by setting the WTICFG.WTIOUT bit to 1. The selected clock and the wakeup timer interrupt request signal are NORed to output together from the FOUT pin if the TCTL.FSEL[1:0] bits are set to other than 0b11.

3.9 Reset Output Function

3.9.1 Overview

The RA4000CE/RA8000CE has a reset output function to prevent a system malfunction due to a power supply voltage drop. The reset output function detects a drop of the power supply voltage V_{DD} and outputs a reset signal (/RST) to external devices until the voltage is restored.

Note: The reset output function is available only in the model with the /RST pin.

3.9.2 Operations

V_{DD} Voltage Detection Operation for Reset Output

The reset output is controlled according to the V_{DD} voltage detection results.

In Normal mode (when the V_{DD} voltage is normal), the V_{DD} voltage drop detection function operates continuously. When a V_{DD} voltage drop below the V_{DD} drop detection voltage $-V_{DET1n}$ is detected, a reset signal (active low) is output from the /RST pin and the RA4000CE/ RA8000CE enters Safe mode.

In Safe mode, the V_{DD} voltage drop detection operation is switched into intermittent operation to suppress power consumption. When a restoring of the V_{DD} voltage to the V_{DD} rise detection voltage $+V_{DET1n}$ or more is detected, the reset output is cancelled (/RST pin = L to Hi-Z) after 60 ms , and the RA4000CE/RA8000CE returns to Normal mode.

For the V_{DD} drop/rise detection voltages ($-V_{DET1n}$, $+V_{DET1n}$) and the intermittent operation intervals in Safe mode, refer to "*5.7 Reset Output Characteristics*" and Figure 5.2, respectively.

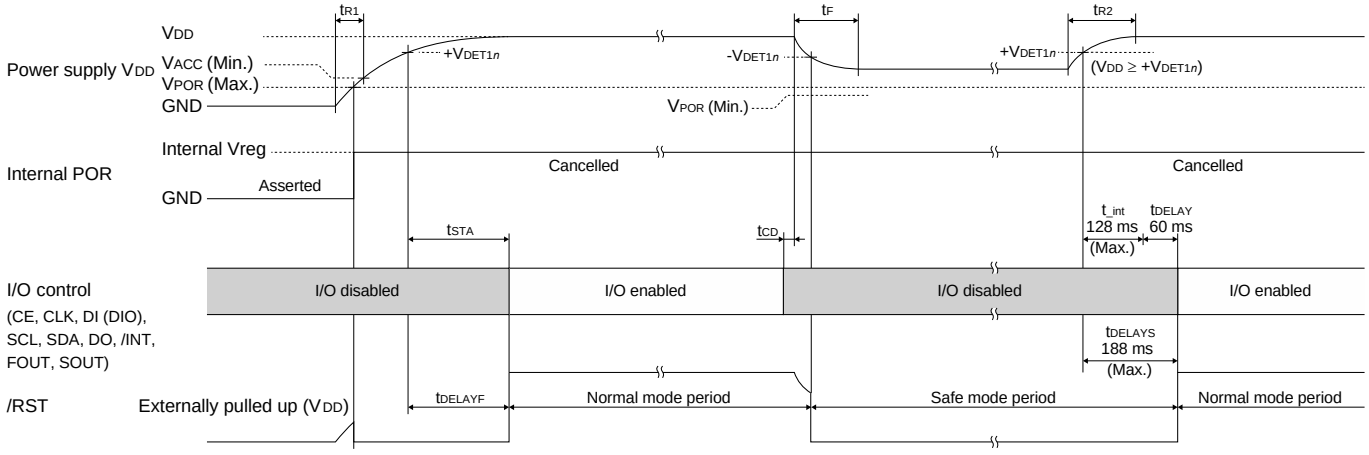


Figure 3.30 Reset Output Timing

Reset Output Flag

When a reset output starts, the reset output flag (BUF_INTF.RSTOF bit) is set to 1. This flag is an internal event trigger factor to capture a time stamp and to generate an interrupt.
This flag must be cleared by writing 0 after the operating mode has been switched from Safe mode to Normal mode and the reset output has been cancelled due to restoring the V_{DD} voltage to $+V_{DET1n}$ or more. During Safe mode, the reset output flag is always set to 1, therefore, it cannot be cleared even if 0 is written.

I/O Control During Reset Output

The /INT, FOUT, and SOUT outputs and the host interface inputs/outputs during Safe mode can be individually enabled or disabled.

The /INT, FOUT, and SOUT outputs are enabled/disabled using the WTICFG.RSTOPT0 bit. When this bit is set to 0 (disabled), the /INT, FOUT, and SOUT output pins are all placed into a Hi-Z state during Safe mode.

The host interface is enabled/disabled using the WTICFG.RSTOPT1 bit. When this bit is set to 0 (disabled), the host interface input/output signals, FOE, CE, CLK, DI, DIO, SDA, and SCL are disabled (can be placed into a Hi-Z state), and DO output pin is placed into a Hi-Z state during Safe mode.

The EVIN*n* pin inputs are always enabled even in Safe mode.

3.10 Self-Monitoring Function

3.10.1 Overview

The RA4000CE/RA8000CE includes a function to monitor the power supply voltage and oscillation statuses, and provides the status flags for software to read the monitoring results. These flags can also be used as a time stamp trigger and recording data, and an event detection interrupt source. The following lists the monitoring items:

- Power-on reset execution (PORF flag, VLF flag)
- Oscillation stoppage (OSCSTPF flag, VLF flag)
- Drop of power supply voltage (V_{DD}) below temperature compensation update stop voltage (VTMPLF flag)

The models with the /INT and SOUT pins can output the status of these status flags to an external device except for the PORF and VLF flags.

3.10.2 Self-Monitoring Flags

Power-On Reset Detection: PORF flag

The PORF flag (INTF.PORF bit) is set to 1 when a power-on reset execution is detected after power is turned on. This flag does not automatically revert to 0 even if the power-on reset is cancelled after that. When the INTF.PORF bit = 1, perform necessary initial settings and clear the flag by writing 0.

Crystal Oscillation Stop Detection: OSCSTPF flag

The OSCSTPF flag (INTF.OSCSTPF bit) is set to 1 when the built-in crystal oscillator stops oscillating for 10 ms or more. This flag does not automatically revert to 0 after being set to 1 even if the oscillation is restored. When the INTF.OSCSTPF bit = 1, perform necessary initial settings and clear the flag by writing 0.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.11.5 Time Stamp (Event Detection) Interrupts*."

Invalid Date and Time Data Warning: VLF Flag

The VLF flag (INTF.VLF bit) is set to 1 when the above PORF flag or OSCSTPF flag is set. If the INTF.VLF bit, this flag, is 1 after turning the V_{DD} power on or restoring from Safe mode, initial settings are required. For an initial setting procedure including INTF.VLF bit manipulations, refer to "*2.2.3 Initial Settings*."

Temperature Compensation Update Stop Detection: VTMPLF flag

The VTMPLF flag (INTF.VTMPLF bit) is set to 1 when the V_{DD} voltage drops to the temperature compensation update stop voltage (V_{DET2}) or less. In this case, the temperature compensation circuit stops and the oscillation continues under the last frequency correction condition before being stopped. The INTF.VTMPLF bit is cleared by writing 0 after V_{DD} has risen above V_{TMP}.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.11.5 Time Stamp (Event Detection) Interrupts*."

3.10.3 Self-Monitoring Flag Output Function

The /INT pin can output the flag setting statuses as event detection interrupts. This function is included in the event detection interrupt, a part of the time stamp interrupts, so refer to "*3.11.5 Time Stamp (Event Detection) Interrupts*," for details.

The SOUT pin can also output flag setting statuses. For more information on the SOUT output function, refer to "*3.12 SOUT Output Function*."

3.11 Time Stamp Function

3.11.1 Overview

The RA4000CE/RA8000CE has a time stamp function that records the information such as the date/time and event factor when an external event, which is generated due to a change of a EVIN*n* pin input signal, or an internal event, such as a voltage drop or oscillation stop status detected by the self-monitoring function, has occurred. The main features of the time stamp function are outlined below.

- Time stamp trigger sources
  External event inputs: - Max. 2 channels (EVIN1, EVIN2)
  - Internal pull-up/pull-down resistors are configurable.
  - Trigger edge is selectable: Rising edge, falling edge, or both edges.
  - Noise filters are included (selectable filtering time: 0 to 5000 ms, 125 ms steps).
  - Event counters are included (6 bits each, available only for counting external events).
  - Input-pin status can be monitored.

  Internal events: - Reset output (-V_{DET1n} voltage drop detection)
  - V_{DET2} voltage drop detection
  - Oscillation stop detection

  Command trigger: - Writing to the specific address can issue a trigger.
- Time stamp buffer - A 32-byte SRAMs is included.
  - Two buffer operating modes are supported: Direct mode that records two stamp data of the selected events, and SRAM mode that uses the whole area as an SRAM allowing reading and writing data freely.
  - Two write modes are supported in Direct mode: Overwrite mode that enables overwriting to the 2nd buffer when the buffers are in full status, and Overwrite Inhibit mode that does not overwrite the buffer.
- Record data - 1/1024 seconds to 1 second, clock/calendar data in BCD format (second, minute, hour, day (day-of-week is not recorded), month, and year), or binary counter data, EVIN*n* pin status, voltage drop and oscillation statuses, and time stamp trigger factor
- Time stamp data can be captured even in Safe mode.
- Can generate an interrupt when an external or internal event occurs.

Figure 3.31 shows the configuration of the time stamp circuit.

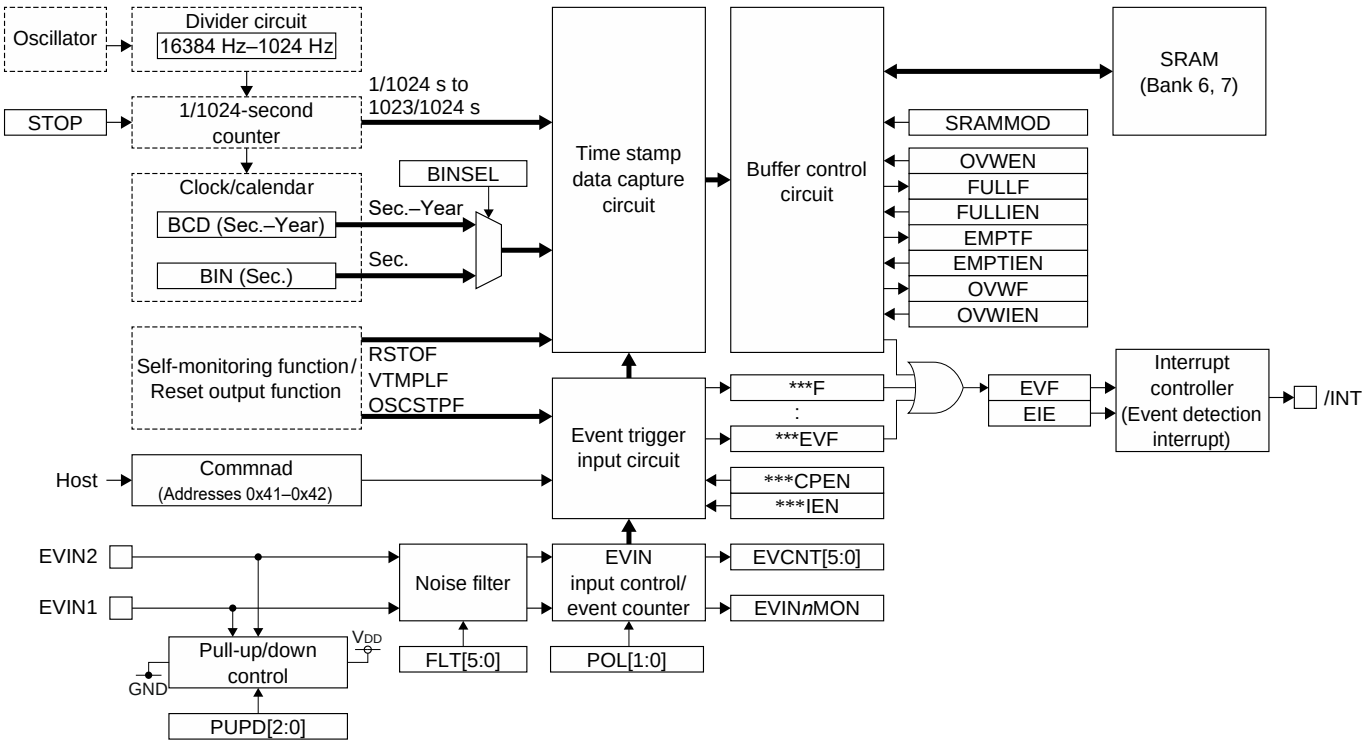


Figure 3.31 Configuration of Time Stamp Circuit

3.11.2 Time Stamp Triggers

When a trigger is generated by an external event, internal event, or writing to the specific address, the RA4000CE/ RA8000CE captures time stamp data at that point and writes it to the buffer. These time stamp triggers are referred to EVIN*n* event input trigger, internal event trigger, and command trigger.

External Event Inputs (EVIN*n* pin) Trigger

External event input trigger signals are input from the EVIN1 and EVIN2 pins. The following shows the functions, or conditions that should be set, related to the external event trigger input.

Pull-up/pull-down resistors

The EVIN*n* pins have software configurable pull-up and pull-down resistors.

Table 3.16 EVIN*n* Pin Pull-Up/Pull-Down Resistor Selections

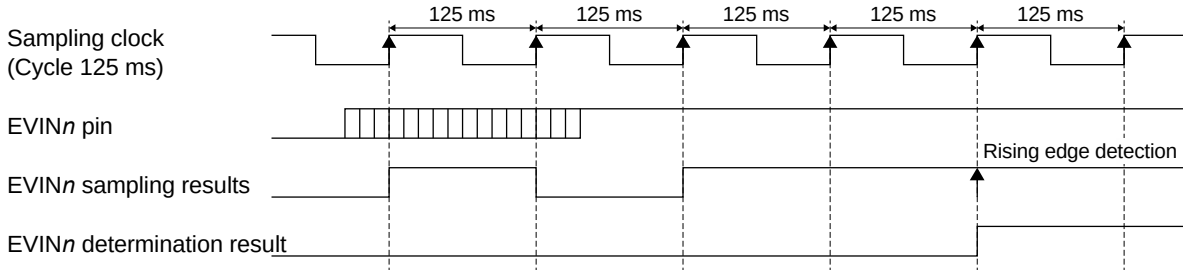
EVIN1_CFG.PUPD[2:0] EVIN2_CFG.PUPD[2:0]	Pull-up/pull-down resistor
0b000	No pull-up/pull-down resistor
0b001	Pull-up resistor 500 kΩ
0b010	Pull-up resistor 1 MΩ (default)
0b011	Pull-up resistor 10 MΩ
0b100	Pull-down resistor 500 kΩ
Other	No pull-up/pull-down resistor

Noise filter

The EVIN*n* pin has a noise filter circuit that eliminates noise on the input signal. The EVIN*n* pin input signal is sampled in 125 ms cycles and when the sampling results are continuously matched the number of times set in the EVIN*n*_FLT.FLT[5:0] bits, it is determined that the sampled logical value has been input.

EVIN1 noise filter: EVIN1_FLT.FLT[5:0] bits
EVIN2 noise filter: EVIN2_FLT.FLT[5:0] bits (Filtering time [ms] = FLT[5:0] × 125)

The figure below is an example when the EVIN*n*_FLT.FLT[5:0] bit = 0x03.



(When rising edge is detected, EVIN*n*_FLT.FLT[5:0] bit = 0x03)

Figure 3.32 EVIN*n* Noise Filter Function

Notes:
- To determine that the EVIN*n* pin input signal is valid, it must have a 1 ms or more pulse width even if the EVIN*n*_FLT.FLT[5:0] bits are set to 0x00.
- The input signal is fetched after 5 ms from the input detection, therefore, a 5 ms delay occurs until the time stamp data is captured.

Table 3.17 Valid EVIN*n* Input Pulse Width

EVIN*n*_FLT. FLT[5:0]	Uncertain EVIN*n* pulse width (Whether the edge input is detected or not depends on the relationship between the edge input timing and the sampling timing in 125 ms cycles.)	Valid EVIN*n* pulse width (The edge input is always detected.)
0x00	–	1 ms or more
0x01 (Setting prohibited)	–	–
0x02	125 ms or more and less than 250 ms	250 ms or more
0x03	250 ms or more and less than 375 ms	375 ms or more
:	:	:
0x27	4750 ms or more and less than 4875 ms	4875 ms or more
0x28	4875 ms or more and less than 5000 ms	5000 ms or more
0x29 or more (Setting prohibited)	–	–

Input detection

The EVIN*n* pin input signal edge to be detected is configurable.

Table 3.18 EVIN*n* Pin Input Detection Edge

EVIN1_CFG.POL[1:0] EVIN2_CFG.POL[1:0]	Detection edge
0b00	Falling edge (default)
0b01	Rising edge
0b10	Falling and rising edges
0b11	

Event counter

Each EVIN*n* input has a 6-bit counter to count the number of event trigger inputs within the range from 0 to 63. The counter value can be read from the bits shown below.

EVIN1 event counter: EVIN1_EVCNT.EVCNT[5:0] bits
EVIN2 event counter: EVIN2_EVCNT.EVCNT[5:0] bits

Monitor

The RA4000CE/RA8000CE provides the bits for monitoring the current EVIN*n* pin status (input logic level).

EVIN1 monitor: EVINMON.EVIN1MON bit
EVIN2 monitor: EVINMON.EVIN2MON bit (1: High level input, 0: Low level input)

Internal Event Trigger

When a power supply voltage drop status or an oscillation stop status is detected, the detector circuit can issue an internal event trigger.

Reset output (Time stamp data is captured when $V_{DD} < -V_{DET1n}$ is detected.)
V_{DET2} voltage drop detection (Time stamp data is captured when $V_{DD} \leq V_{DET2}$ is detected.)
Oscillation stop detection (Time stamp data capturing starts when the oscillator resumes oscillation.)

Command trigger

A command trigger can be issued by writing an arbitrary value to Register WRCMD_TRG after setting the WRCMD_CFG.CMDTRGEN bit to 1.

3.11.3 Time Stamp Buffer

The RA4000CE/RA8000CE includes a 32-byte SRAM (register RAM) that are used as a time stamp buffer for storing captured time stamp data.

Time Stamp Data

The time stamp buffer can record two time-stamp data that consists of the date and time, internal statuses, and trigger factor when an event has occurred. The date and time to be recorded is selected from BCD counter data and BIN counter data using the BUF1_CFG1.BINSEL bit.
Figure 3.33 shows the data layout in the time stamp buffer. The first captured data after the buffer has been cleared can be read from Bank 6 (Addresses 0x60 to 0x69); the second or latest data can be read from Bank 7 (Addresses 0x70 to 0x79). The buffer data can be read by accessing continuously from Addresses 0x60 to 0x69 or Addresses 0x70 to 0x79.

When BCD counter data is captured (BUF1_CFG1.BINSEL bit = 0)

Address	Captured data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	1/1024-second divider counter data	SUBSEC1	SUBSEC0	–	–	–	–	–	–
0x70		2	1						
0x61		SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2
0x71		512	256	128	64	32	16	8	4
0x62	Second BCD data (0–59)	–	SEC_H[2:0]			SEC_L[3:0]			
0x72			10-second digit (BCD)			1-second digit (BCD)			
0x63	Minute BCD data (0–59)	–	MIN_H[2:0]			MIN_L[3:0]			
0x73			10-minute digit (BCD)			1-minute digit (BCD)			
0x64	Hour BCD data (0–23)	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
0x74				10-hour digit (BCD)		1-hour digit (BCD)			
0x65	Day BCD data (1–31)	–	–	DAY_H[1:0]		DAY_L[3:0]			
0x75				10-day digit (BCD)		1-day digit (BCD)			
0x66	Month BCD data (1–12)	–	–	–	MONTH_H	MONTH1[3:0]			
0x76					10-Month digit (BCD)	1-Month digit (BCD)			
0x67	Year BCD data (0–99)	YEAR_H[3:0]				YEAR_L[3:0]			
0x77		10-year digit (BCD)				1-year digit (BCD)			
0x68	Internal status	–	EVIN2POL	EVIN1POL	–	RSTOSTAT	VTMPLSTAT	–	OSCSTP STAT
0x78			EVIN2 input status	EVIN1 input status		Reset output status	V_{DET2} drop detection status		Oscillation stop detection status
0x69	Data capturing trigger factor	OVWFSTAT*	EVIN2TRG	EVIN1TRG	WRCMDTRG	RSTOTRG	VTMPLTRG	–	OSCSTPTRG
0x79		Overwrite status	EVIN2 input trigger	EVIN1 input trigger	Command trigger	Reset output trigger	V_{DET2} drop detection trigger		Oscillation stop detection trigger

* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

When BIN counter data is captured (BUF1_CFG1.BINSEL bit = 1)

Address	Captured data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	1/1024-second divider counter data	SUBSEC1	SUBSEC0	–	–	–	–	–	–
0x70		2	1						
0x61		SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2
0x71		512	256	128	64	32	16	8	4
0x62	Second binary data 0	SEC_BIN7	SEC_BIN6	SEC_BIN5	SEC_BIN4	SEC_BIN3	SEC_BIN2	SEC_BIN1	SEC_BIN0
0x72		128 s	64 s	32 s	16 s	8 s	4 s	2 s	1 s
0x63	Second binary data 1	SEC_BIN15	SEC_BIN14	SEC_BIN13	SEC_BIN12	SEC_BIN11	SEC_BIN10	SEC_BIN9	SEC_BIN8
0x73		32768 s	16384 s	8192 s	4096 s	2048 s	1024 s	512 s	256 s
0x64	Second binary data 2	SEC_BIN23	SEC_BIN22	SEC_BIN21	SEC_BIN20	SEC_BIN19	SEC_BIN18	SEC_BIN17	SEC_BIN16
0x74		8388608 s	4194304 s	2097152 s	1048576 s	524288 s	262144 s	131072 s	65536 s
0x65	Second binary data 3	SEC_BIN31	SEC_BIN30	SEC_BIN29	SEC_BIN28	SEC_BIN27	SEC_BIN26	SEC_BIN25	SEC_BIN24
0x75		2147483648 s	1073741824 s	536870912 s	268435456 s	134217728 s	67108864 s	33554432 s	16777216 s
0x66	Second binary data 4	–	–	–	–	–	–	–	SEC_BIN32
0x76									4294967296 s
0x67	–	–							
0x77									
0x68	Internal status	–	EVIN2POL	EVIN1POL	–	RSTOSTAT	VTMPLSTAT	–	OSCSTP STAT
0x78			EVIN2 input status	EVIN1 input status		Reset output status	V_{DET2} drop detection status		Oscillation stop detection status
0x69	Data capturing trigger factor	OVWFSTAT*	EVIN2TRG	EVIN1TRG	WRCMDTRG	RSTOTRG	VTMPLTRG	–	OSCSTPTRG
0x79		Overwrite status	EVIN2 input trigger	EVIN1 input trigger	Command trigger	Reset output trigger	V_{DET2} drop detection trigger		Oscillation stop detection trigger

* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

Figure 3.33 Time Stamp Data and Read Addresses

Time Stamp Buffer Operating Mode

The time stamp buffer has two operating modes that can be selected with the BUF1_CFG2.SRAMMOD bit, Direct mode and SRAM mode.

Direct Mode (BUF1_CFG2.SRAMMOD bit = 0)

This mode is used only for reading time stamp data and does not allow the host to write data to the buffer. As shown in Figure 3.33, time stamp data can be read from Bank 6 (Addresses 0x60 to 0x69) and Bank 7 (Address 0x70 to 0x79).

SRAM mode (BUF1_CFG2.SRAMMOD bit = 1)

In this mode, the buffer can be read/written as an SRAM through Bank 6 (Addresses 0x60 to 0x69) and Bank 7 (Address 0x70 to 0x79) The figure below shows the relationship between the physical address of the SRAM and the read/write address in Bank 6 and Bank 7.

SRAM address	**SRAM data R/W address**
0x00	Address 0x60
0x01	Address 0x61
0x02	Address 0x62
0x03	Address 0x63
:	:
0x0D	Address 0x6D
0x0E	Address 0x6E
0x0F	Address 0x6F
0x10	Address 0x70
0x11	Address 0x71
0x12	Address 0x72
0x13	Address 0x73
:	:
0x1D	Address 0x7D
0x1E	Address 0x7E
0x1F	Address 0x7F

Figure 3.34 Memory Access in SRAM Mode

Time Stamp Buffer Write Mode

When two time-stamp data are recorded to the time stamp buffer that has been cleared, the buffer enters full state. The RA4000CE/RA8000CE provides two write modes that have a different behavior after the buffer becomes full.

Overwrite mode

The time stamp buffer enters Overwrite mode by setting the BUF1_CFG1.OVWF bit to 1. When a time stamp trigger is generated while the time stamp buffer is in full state, the new captured time stamp is overwritten to Bank 7. The time stamp recorded in Bank 6 is retained without being overwritten.
When an overwrite occurs, the BUF1_STAT.OVWF bit is set to 1.

Overwrite Inhibit mode

The time stamp buffer enters Overwrite Inhibit mode by setting the BUF1_CFG1.OVWEN bit to 0. When a time stamp trigger is issued while the buffer is in full state, although the overwrite flag, BUF1_STAT.OVWF bit, is set, the captured data is discarded. The time stamps recorded in Bank 6 and Bank 7 are retained without being overwritten.

3.11.4 Operations

Initial Settings

1. Disabling event detection interrupt outputs from the /INT pin
   Disable interrupts so that unnecessary event detection interrupts will not occur during initial setting.

   1-1. Set the TSTP_INTE.EIE bit to 0. (Disable time stamp event detection interrupt)

2. Setting EVIN*n* input conditions
   Perform the following settings according to the EVIN*n* input to be used:

   2-1. When using the EVIN1 input, configure the following bits in Registers EVIN1_CFG and EVIN1_FLT:
   - EVIN1_CFG.PUPD[2:0] bits (Select pull-up/pull-down resistor)
   - EVIN1_CFG.POL[1:0] bits (Select detection edge)
   - EVIN1_FLT.FLT[5:0] bits (Set input filtering time)

   2-2. When using the EVIN2 input, configure the following bits in Registers EVIN2_CFG and EVIN2_FLT:
   - EVIN2_CFG.PUPD[2:0] bits (Select pull-up/pull-down resistor)
   - EVIN2_CFG.POL[1:0] bits (Select detection edge)
   - EVIN2_FLT.FLT[5:0] bits (Set input filtering time)

3. Setting interrupts

   3-1. When enabling external event input interrupts, set the following bits in Register EVNT_INTE to 1 (or set to 0 to disable):
   - EVNT_INTE.EVIN1IEN bit *1 (Enable/disable EVIN1 event input interrupt)
   - EVNT_INTE.EVIN2IEN bit *1 (Enable/disable EVIN2 event input interrupt)

   3-2. When enabling internal event interrupts, set the following bits in Register EVNT_INTE to 1 (or set to 0 to disable):
   - EVNT_INTE.RSTOIEN bit *1 (Enable/disable reset output event interrupt)
   - EVNT_INTE.VTMPLIEN bit *1 (Enable/disable V_{DET2} voltage drop detection event interrupt)
   - EVNT_INTE.OSCSTPIEN bit *1 (Enable/disable oscillation stop detection event interrupt)

   *1 These bits enable/disable interrupts by occurrence of the events regardless of whether time stamp data is captured or not.

   3-3. When enabling time stamp trigger input interrupts, set the following bits in Register BUF1_CFG1 to 1 (or set to 0 to disable):
   - BUF1_CFG1.FULLIEN bit (Enable/disable buffer full (2nd capture) interrupt)
   - BUF1_CFG1.EMPTIEN bit (Enable/disable buffer not empty (1st capture) interrupt)
   - BUF1_CFG1.OVWIEN bit (Enable/disable buffer overwrite (3rd or following capture) interrupt)

4. Setting buffer

   4-1. Configure the following bits in Register BUF1_CFG1:
   - BUF1_CFG1.BINSEL bit (Select date and time data type (BCD/BIN))
   - BUF1_CFG1.OVWEN bit (Select Overwrite/Overwrite Inhibit mode)

5. Clearing event counters and buffer flags by issuing a command trigger

   5-1. Switch to SRAM mode and clear the buffer data to all 1 or 0 as necessary.

   For more information on SRAM mode, refer to "*3.11.6 Reading/Writing in SRAM mode*."

   5-2. Write 0x90 to Register WRCMD_CFG. (Clear command)

   5-3. Write any value to Register WRCMD_TRG. (Issue command trigger)

6. Enabling event detection interrupt outputs from the /INT pin

   6-1. Set the TSTP_INTE.EIE bit to 1. (Enable time stamp event detection interrupt)

7. Setting external events to capture time stamps

   7-1. When capturing time stamps using the EVIN*n* inputs, set the following bits in Register EVIN_EN to 1 (or set to 0 to disable):
   - EVIN_EN.EVIN1CPEN bit (Enable/disable time stamp capture by EVIN1 input)
   - EVIN_EN.EVIN2CPEN bit (Enable/disable time stamp capture by EVIN2 input)

8. Setting internal events to capture time stamps

   8-1. When capturing time stamps when an internal event occurs, set the following bits in Register CAP_EN to 1 (or set to 0 to disable):
   - CAP_EN.RSTOCPEN bit (Enable/disable time stamp capture by reset output event trigger)
   - CAP_EN.VTMPLCPEN bit (Enable/disable time stamp capture by V_{DET2} voltage drop detection event trigger)
   - CAP_EN.OSCSTPCPEN bit (Enable/disable time stamp capture by oscillation stop detection event trigger)

9. Enabling external event inputs

   9-1. When enabling external event inputs from the EVIN*n* pin, set the following bits in Register EVIN_EN to 1 (or set to 0 to disable):
   - EVIN_EN.EVIN1EN bit *2 (Enable/disable external event input from EVIN1)
   - EVIN_EN.EVIN2EN bit *2 (Enable/disable external event input from EVIN2)

   *2 When setting the EVIN_EN.EVIN*n*EN bit to 0 (EVIN*n* input disabled), the EVIN_EN.EVIN*n*CPEN bit should also be set to 0.

Time Stamp Capturing Operation

When a trigger is generated by an event that is enabled to capture time stamp data or a command trigger, the RA4000CE/RA8000CE captures time stamp data from the counters and flags, and writes it to the buffer.
The first captured time stamp data after the buffer is cleared is written to the Bank 6 buffer and the second captured data is written to the Bank 7 buffer. After that, subsequently captured data are overwritten to the Bank 7 buffer in overwrite mode or destroyed in Overwrite Inhibit mode until the buffer is cleared by executing a buffer flag reset command.
Figure 3.35 and Figure 3.36 show the statuses of the buffer and buffer status bits according to data capturing.

Time stamp capture	Initial	1st time	2nd time	CLR *1	3rd time	4th time	CLR *1	5th time	6th time	CLR *1	7th time	8th time
Buffer												
Bank 6	Undefined	1st data	1st data	1st data	3rd data	3rd data	3rd data	5th data	5th data	5th data	7th data	7th data
Bank 7	Undefined	Undefined	2nd data	2nd data	2nd data	4th data	4th data	4th data	6th data	6th data	6th data	8th data
Bank 6 read		↑			↑			↑			↑	
Bank 7 read			↑			↑			↑			↑
Flag/interrupt												
BUF1_STAT.EMPTF	1	0	0	1	0	0	1	0	0	1	0	0
Buffer not empty interrupt		↑			↑			↑			↑	
BUF1_STAT.FULLF	0	0	1	0	0	1	0	0	1	0	0	1
Buffer full interrupt			↑			↑			↑			↑
BUF1_STAT.OVWF	0	0	0	0	0	0	0	0	0	0	0	0
Buffer overwrite interrupt												
Event counter *2												
EVIN*n*_EVCNT.ECNT[5:0]	0x00	0x01	0x02	0x00	0x01	0x02	0x00	0x01	0x02	0x00	0x01	0x02

Time stamp capture	9th time	10th time	11th time	…	69th time	70th time	71st time	CLR *1	72nd time	73rd time	74th time	75th time
Buffer												
Bank 6	7th data	7th data	7th data	7th data	7th data	7th data	7th data	7th data	72nd data	72nd data	72nd data	72nd data
Bank 7	8th data	8th data	8th data	8th data	8th data	8th data	8th data	8th data	8th data	73rd data	73rd data	73rd data
Bank 6 read												
Bank 7 read												
Flag/interrupt												
BUF1_STAT.EMPTF	0	0	0	0	0	0	0	1	0	0	0	0
Buffer not empty interrupt									↑			
BUF1_STAT.FULLF	1	1	1	1	1	1	1	0	0	1	1	1
Buffer full interrupt										↑		
BUF1_STAT.OVWF	1	1	1	1	1	1	1	0	0	0	1	1
Buffer overwrite interrupt	↑	↑	↑	↑	↑	↑	↑				↑	↑
Event counter *2												
EVIN*n*_EVCNT.ECNT[5:0]	0x03	0x04	0x05	…	0x3F	0x00	0x01	0x00	0x01	0x02	0x03	0x04

■ Writing a new data to Bank 6 ■ Writing a new data to Bank 7
*1: CLR means that a command trigger with Register WRCMD_CFG set to 0x90 is executed.
*2: The event counter contents are the values when no event triggers other than EVIN*n* inputs have been issued.

Figure 3.35 Time Stamp Capture Operations (Overwrite Inhibit mode)

Time stamp capture	Initial	1st time	2nd time	CLR *1	3rd time	4th time	CLR *1	5th time	6th time	CLR *1	7th time	8th time
Buffer												
Bank 6	Undefined	1st data	1st data	1st data	3rd data	3rd data	3rd data	5th data	5th data	5th data	7th data	7th data
Bank 7	Undefined	Undefined	2nd data	2nd data	2nd data	4th data	4th data	4th data	6th data	6th data	6th data	8th data
Bank 6 read		↑			↑			↑			↑	
Bank 7 read			↑			↑			↑			↑
Flag/interrupt												
BUF1_STAT.EMPTF	1	0	0	1	0	0	1	0	0	1	0	0
Buffer not empty interrupt		↑			↑			↑			↑	
BUF1_STAT.FULLF	0	0	1	0	0	1	0	0	1	0	0	1
Buffer full interrupt			↑			↑			↑			↑
BUF1_STAT.OVWF	0	0	0	0	0	0	0	0	0	0	0	0
Buffer overwrite interrupt												
Event counter *2												
EVIN*n*_EVCNT.ECNT[5:0]	0x00	0x01	0x02	0x00	0x01	0x02	0x00	0x01	0x02	0x00	0x01	0x02

Time stamp capture	9th time	10th time	11th time	…	63rd time	64th time	65th time	CLR *1	6th time	67th time	68th time	69th time
Buffer												
Bank 6	7th data	7th data	7th data	7th data	7th data	7th data	7th data	7th data	66th data	66th data	66th data	66th data
Bank 7	9th data	10th data	11th data	…	63rd data	64th data	65th data	65th data	65th data	67th data	68th data	69th data
Bank 6 read												
Bank 7 read												
Flag/interrupt												
BUF1_STAT.EMPTF	0	0	0	0	0	0	0	1	0	0	0	0
Buffer not empty interrupt									↑			
BUF1_STAT.FULLF	1	1	1	1	1	1	1	0	0	1	1	1
Buffer full interrupt										↑		
BUF1_STAT.OVWF	1	1	1	1	1	1	1	0	0	0	1	1
Buffer overwrite interrupt	↑	↑	↑	↑	↑	↑	↑				↑	↑
Event counter *2												
EVIN*n*_EVCNT.ECNT[5:0]	0x03	0x04	0x05	…	0x3F	0x00	0x01	0x00	0x01	0x02	0x03	0x04

■ Writing a new data to Bank 6 ■ Writing a new data to Bank 7

*1: CLR means that a command trigger with Register WRCMD_CFG set to 0x90 is executed.

*2: The event counter contents are the values when no event triggers other than EVIN*n* inputs have been issued.

Figure 3.36 Time Stamp Capture Operations (Overwrite mode)

Buffer status

The buffer provides the flags listed below to indicate its status.

- Buffer empty flag (BUF1_STAT.EMPTF bit)
- Buffer full flag (BUF1_STAT.FULLF bit)
- Buffer overwrite flag (BUF1_STAT.OVWF bit)

The buffer is set to empty status (buffer data is undefined) in initial state and the buffer status flags are set as follows:

BUF1_STAT.EMPTF bit = 1 (Buffer empty)
BUF1_STAT.FULLF bit = 0 (Buffer not full)
BUF1_STAT.OVWF bit = 0 (Not overwritten)

Buffer is also placed into empty status and the buffer status flags are reset as above by issuing a command trigger (writing any value to Register WRCMD_TRG) with the WRCMD_CFG.BUF1FCLREN bit set to 1 (buffer status flag reset). However, the buffer contents are retained without being cleared. When clearing the buffer data, rewrite the contents by setting the time stamp buffer into SRAM mode. For more information on SRAM mode, refer to "*3.11.6 Reading/Writing in SRAM mode*."

1. When the 1st time stamp data is captured

   When the 1st time stamp data is captured while the buffer is in empty status, the data is written to the Bank 6 buffer and the buffer status flags are set as follows:

   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 0 (Buffer not full)
   BUF1_STAT.OVWF bit = 0 (Not overwritten)

   A buffer not empty interrupt can be generated when the BUF1_STAT.EMPTF bit is cleared to 0. Read the time stamp data from Bank 6 using this interrupt. Note that the BUF1_STAT.EMPTF bit is not reset to 1 by this reading.

2. When the 2nd time stamp data is captured

   When the 2nd time stamp data is captured after Step 1 above, the data is written to the Bank 7 buffer regardless of whether Bank 6 is read or not. The buffer status flags are set as follows:

   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 1 (Buffer full)
   BUF1_STAT.OVWF bit = 0 (Not overwritten)

   A buffer full interrupt can be generated when the BUF1_STAT.FULLF is set to 1. Read the time stamp data from Bank 7 using this interrupt. Note that the BUF1_STAT.FULLF bit is not cleared to 0 by this reading.

3. When the 3rd (or later) time stamp data is captured

   In Overwrite mode

   When a new time stamp data is captured while the buffer is in full status, the data is overwritten to the Bank 7 buffer regardless of whether Banks 6 and 7 are read or not. The buffer status flags are set as follows:

   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 1 (Buffer full)
   BUF1_STAT.OVWF bit = 1 (Overwritten)

   A buffer overwrite interrupt can be generated when the BUF1_STAT.OVWF is set to 1. If the buffer status flags have been set as above, the data in Bank 7 before being read has been overwritten. To avoid this, issue a command trigger (buffer status flag reset) to place the buffer into empty status after reading Banks 6 and 7.

   In Overwrite Inhibit mode

   Time stamp data captured in buffer full status are not written to the buffer and discarded. The buffer status flags are set as follows:

   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 1 (Buffer full)
   BUF1_STAT.OVWF bit = 1 (Overwritten)

   The BUF1_STAT.OVWF bit is set to 1 when the 3rd or a later time stamp data is captured even in Overwrite Inhibit mode, thus an overwrite interrupt can be generated. However, Banks 6 and 7 retain the 1st and 2nd time stamp data captured after the initial status or the buffer status flags have been reset.

Issuing Command Trigger

The RA4000CE/RA8000CE allows the host to issue a time stamp trigger by writing data to specific registers. The following shows its procedure:

1. Set the WRCMD_CFG.CMDTRGEN bit to 1. (Specify command trigger)
2. Write any data to the WRCMD_TRG.WRTRG[7:0] bits. (Issue command trigger)
3. Confirm if the BUF_INTF.BUF1F bit has been set to 1.
   Or confirm if the BUF1_CFG2.RDPAGE[3:0] bits have been incremented.
4. Confirm if the WRCMD_TRG.WRTRG[7:0] bits revert to 0x00.

Step 3 is a method to confirm that the time stamp trigger is accepted normally.
Step 4 is necessary when reading time stamp data or issuing the next command trigger immediately after a command trigger has been issued.

Note: When issuing time stamp triggers in succession, a 5 ms interval is required between the triggers.

Figure 3.37 shows the time stamp trigger timing when a command trigger is issued.
In both RA4000CE and RA8000CE, a command trigger is issued at the rising edge of the clock for the LSB of the Register WRCMD_TRG data.

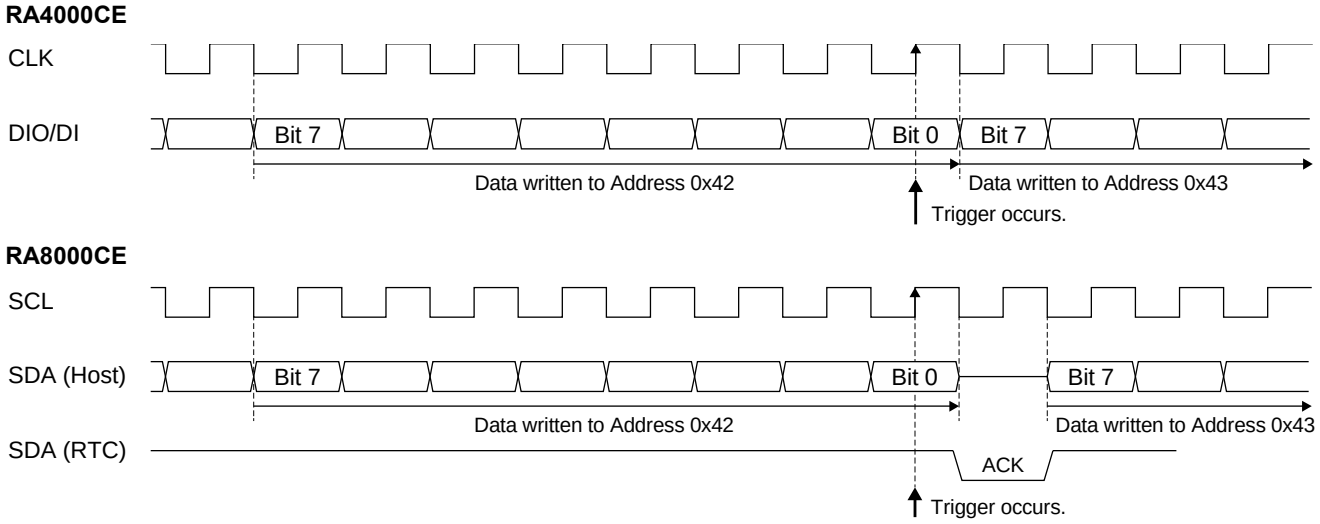


Figure 3.37 Command Trigger Timing

The command trigger has the following functions in addition to the time stamp trigger:

WRCMD_CFG.EVCNTCLREN bit: Issuing a command trigger with this bit set to 1 clears the event counters (Registers EVIN*n*_EVCNT).

WRCMD_CFG.BUF1FCLREN bit: Issuing a command trigger with this bit set to 1 clears the following bits.
BUF1_STAT.FULLF bit (Buffer full flag)
BUF1_STAT.EMPTF bit (Buffer empty flag)
BUF1_STAT.OVWF bit (Buffer overwrite flag)

Reading Time Stamp Data

The following shows an example of time stamp data read procedure:

1. After an interrupt has occurred (/INT = L), read Register INTF (or Register INTF_MIR).
   When the INTF.EVF bit = 1, a time stamp event detection interrupt has occurred. In this case, perform the procedure from Step 2.

   If another interrupt has occurred, execute the corresponding interrupt handler.

2. Read Registers EVNT_INTF and BUF_INTF to determine the interrupt factor that has occurred.

   <When a flag in Register EVNT_INTF has been set>
   It indicates that an EVIN*n* or internal event has occurred. Table 3.19 shows the set condition of each flag. Execute an interrupt handler according to the event that has occurred. The flag that has been set to 1 should be cleared by writing 0 in the interrupt handler.

Note: When the EVNT_INTF.RSTOEVF bit = 1, the BUF_INTF.RSTOF bit has been set as well. To subsequently capture time stamp data by a reset output event, these two flags must be cleared. The EVNT_INTF.RSTOEVF bit is cleared immediately by writing 0, but the BUF_INTF.RSTOF bit cannot be cleared until the V_{DD} voltage is restored to $+V_{DET1n}$ or higher. Therefore, capturing the next time stamp data by a reset output event can be performed after the V_{DD} voltage is restored. For more information of the BUF_INTF.RSTOF bit, refer to "*3.9 Reset Output Function*."

   <When BUF_INTF.BUF1F bit = 1>
   This interrupt occurs when a time stamp data is written to the buffer by occurrence of an event that has been enabled to capture time stamp data.
   Read the captured time stamp data by the following operations.

3. To temporarily disable interrupts, set the TSTP_INTE.EIE bit to 0. (Disable time stamp event detection interrupt))

4. Read Register BUF1_STAT to check the buffer status.

   <Status 1>
   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 0 (Buffer not full)
   BUF1_STAT.OVWF bit = 0 (Not overwritten)

   The first captured time stamp data has been written to Bank 6.

   <Status 2>
   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 1 (Buffer full)
   BUF1_STAT.OVWF bit = 0 (Not overwritten)

   The 1st captured time stamp data has been written to Bank 6 and the 2nd data has been written to Bank 7.

   <Status 3>
   BUF1_STAT.EMPTF bit = 0 (Buffer not empty)
   BUF1_STAT.FULLF bit = 1 (Buffer full)
   BUF1_STAT.OVWF bit = 1 (Overwritten)

   In Overwrite Inhibit mode, Banks 6 and 7 retain the same data as in <Status 2>. The subsequent captured data have been destroyed.
   In Overwrite mode, Bank 6 retains the 1st time stamp data. The data in buffer 7 before being read have been overwritten with the latest data captured in the 3rd or later.

5. Read time stamp data according to the buffer status.
   The data in Bank 6 or Bank 7 should be continuously read for 10 bytes from Addresses 0x60 to 0x69 or Addresses 0x70 to 0x79, respectively. See Figure 3.33 for the contents of these addresses.

   In the following cases, read the time stamp data twice and determine as correct when they match, as data may be updated during reading.
   • When reading Bank 6 when the BUF1_STAT.EMPTF bit = 1 (Buffer empty).
   • When reading Bank 7 when the BUF1_STAT.FULLF bit = 0 (Buffer not full).
   • When reading Bank 7 in <Status 2> or <Status 3> during Overwrite mode.

   In <Status 3>, execute necessary processing, as the newly captured data was destroyed (in Overwrite Inhibit mode) or Bank 7 was overwritten (in Overwrite mode).

6. Issue a command trigger to clear all EVIN*n* event counters and buffer flags.
   - Write 0x90 to Register WRCMD_CFG. (Clear command)
   - Write any value to Register WRCMD_TRG. (Issue command trigger)
7. Confirm if Register WRCMD_TRG.WRTRG reverts to 0x00. (Command execution completed)
   Although the SRAM contents are not cleared, Steps 6 and 7 put the buffer into empty status.

   When clearing the buffer data, rewrite the contents by setting the time stamp buffer into SRAM mode. For more information on SRAM mode, refer to "*3.11.6 Reading/Writing in SRAM mode*."
8. Set the TSTP_INTE.EIE bit to 1 (if it was set to 0 in Step 3). (Enable time stamp event detection interrupt)

3.11.5 Time Stamp (Event Detection) Interrupts

Figure 3.38 shows the configuration of the time stamp interrupt circuit.

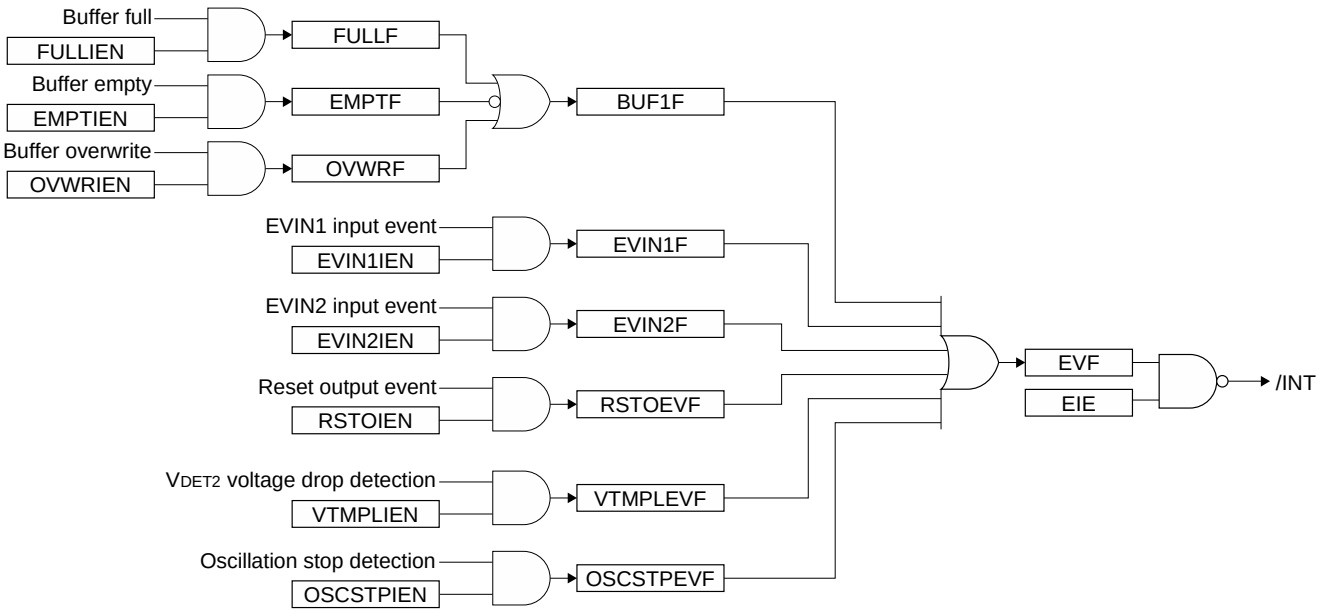


Figure 3.38 Configuration of Time Stamp Interrupt Circuit

The time stamp function has the event detection interrupt factors shown below.

Table 3.19 Event Detection Interrupt Factors and Control Bits

Interrupt factor flag	Interrupt enable bit	Interrupt flag set condition	Clear condition
BUF1_STAT.FULLF	BUF1_CFG1.FULLIEN	Set when the 2nd captured time stamp data is written to the Bank 7 buffer (buffer full status). Not set if the FULLIEN bit = 0.	Cleared by executing a command trigger (buffer status flag reset). * The BUF1_STAT. EMPTF bit is reset to 1.
BUF1_STAT.EMPTF	BUF1_CFG1.EMPTIEN	Set in the initial status or when a command trigger (buffer status flag reset) is executed (buffer empty status). However, an interrupt will occur when this flag is cleared by writing the 1st captured time stamp data to the Bank 6 buffer (buffer not empty status). Not cleared if the EMPTIEN bit = 0.	
BUF1_STAT.OVWF	BUF1_CFG1.OVWIEN	Set when the 3rd or later time stamp data is captured. Not set if the OVWIEN bit = 0.	
BUF_INTF.BUF1F	↑	Set when the FULLF bit = 1, EMPTF bit = 0, or OVWF bit = 1. Not set if the FULLIEN bit, EMPTIEN bit, and OVWIEN bit are all set to 0.	
EVNT_INTF.EVIN1F	EVNT_INTE.EVIN1IEN	Set when an event trigger is input from the EVIN*n* pin regardless of whether a data is written to the buffer or not. Not set if the EVIN*n*IEN bit = 0.	Cleared by writing 0.
EVNT_INTF.EVIN2F	EVNT_INTE.EVIN2IEN		
EVNT_INTF.RSTOEVF	EVNT_INTE.RSTOIEN	Set when the /RST pin starts a reset output. Not set if the RSTOIEN bit = 0.	
EVNT_INTF.VTMPLEVF	EVNT_INTE.VTMPLIEN	Set when a V_{DET2} voltage drop is detected. Not set if the VTMPLIEN bit = 0.	
EVNT_INTF.OSCSTPEVF	EVNT_INTE.OSCSTPIEN	Set when an oscillation stoppage is detected. Not set if the OSCSTPIEN bit = 0.	

These factors can be individually enabled/disabled to generate an interrupt. When a factor occurs, the interrupt factor flag is set and INTF.EVF bit is also set. If the TSTP_INTE.EIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. The INTF.EVF bit that has been set to 1 is not cleared by writing 0. To clear the INTF.EVF bit, the flags in Registers BUF_INTF and EVNT_INTF must be all cleared. When the INTF.EVF bit is cleared, the /INT pin goes into a Hi-Z state.

3.11.6 Reading/Writing in SRAM Mode

Banks 6 and 7 enter SRAM mode by setting the BUF1_CFG2.SRAMMOD bit to 1 allowing reading/writing all the bits as normal registers. This makes it possible to clear the buffered old data before capturing time stamp data.

Furthermore, Banks 6 and 7 can be used as a general-purpose RAM when time stamp data is not recorded.

Before setting Banks 6 and 7 into SRAM mode, disable all events to capture time stamp data.

3.12 SOUT Output Function

The SOUT pin has a function to output either a status flag or a logical value specified by the SOUTCTL.DC bit. This function is selected using the SOUTCTL.DCE bit.

Status Output

When the SOUTCTL.DCE bit = 0, the SOUT pin outputs the setting value of an internal status flag (interrupt flag) selected with the SOUTCTL.SOUT[2:0] bits. Table 3.20 lists the flags selected with the SOUTCTL.SOUT[2:0] bits.

Table 3.20 Internal Status Flags Output from SOUT Pin

SOUTCTL.SOUT[2:0]	Status flag
0b000	INTF.TF bit (Wakeup timer interrupt flag)
0b001	INTF.AF bit (Alarm interrupt flag)
0b010	INFF.UF bit (Time update interrupt flag)
0b011	INTF.EF bit (Event detection interrupt flag)
0b100	INTF.VTMPLF bit (Temperature compensation update stop detection flag)
0b101	INTF.VLF bit (Invalid date and time data warning flag)
0b110–0b111	Reserved

The SOUT signal polarity is specified using the SOUTCTL.SIGINV bit.

DC Output

When the SOUTCTL.DCE bit = 1, the SOUT pin outputs the logical value set in the SOUTCTL.DC bit.
An L level is output when the SOUTCTL.DC bit = 0; an H level is output when the SOUTCTL.DC bit = 1.

4 Registers

4.1 List of Registers

Symbol meanings

Bit name = –: This bit is not writable, and the read value is always 0.
Bit name = ×: This bit is not writable, and the read value is undefined.
Bit name = (GP): This is a general-purpose bit that allows writing 0 and 1 as well as reading the contents.

Notes:
- The address values indicate {bank number, address in bank}. (Example: 0x0F = Bank 0, Address 0xF)
- The registers must be accessed in eight-bit units.
- Be sure to avoid writing/reading data to/from an address not listed in the register tables.
- After power is turned on or if the INTF.VLF bit = 1 after the RA4000CE/RA8000CE returns from Safe mode, be sure to initialize all the registers.

Bank 0

Address	Register name (function)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	SEC (Second Data)	BCD mode	–	SEC_H[2:0]			SEC_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x01	MIN (Minute Data)	BCD mode	–	MIN_H[2:0]			MIN_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x02	HOUR (Hour Data)	BCD mode	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x03	WEEKDAY (Day-of-Week Data)	BCD mode	–	WEEK[6:0]						
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x04	DAY (Day Data)	BCD mode	–	–	DAY_H[1:0]		DAY_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x05	MONTH (Month Data)	BCD mode	–	–	–	MONTH_H	MONTH_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x06	YEAR (Year Data)	BCD mode	YEAR_H[3:0]				YEAR_L[3:0]			
	Not used	BIN mode	–	–	–	–	–	–	–	–
0x07	ALM_MIN (Minute Alarm)		XMAE	MALM_H[2:0]			MALM_L[3:0]			
	Not used	BIN mode	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)
0x08	ALM_HOUR (Hour Alarm)		XHAE	(GP)	HALM_H[1:0]		HALM_L[3:0]			
	Not used	BIN mode	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)
0x09	ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm)		XWAE	WKALM[6:0]						
				(GP)	DALM_H[1:0]		DALM_L[3:0]			
	Not used	BIN mode	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)	(GP)
0x0A	WTCNT_L (Wakeup Timer Counter Low)		WTCNT[7:0]							
0x0B	WTCNT_M (Wakeup Timer Counter Middle)		WTCNT[15:8]							
0x0C	WTCNT_H (Wakeup Timer Counter High)		WTCNT[23:16]							
0x0D	TCTL (Timer Control)		FSEL[1:0]		USEL0	TE	WADA	–	TSEL[1:0]	
0x0E	INTF (Status Flag)		PORF	OSCSTPF	UF	TF	AF	EVF	VLF	VTMPLF
0x0F	TSTP_INTE (Timer Stop and Interrupt Enable)		CSEL[1:0]		UIE	TIE	AIE	EIE	–	STOP

Bank 1

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	SUBSEC_L (Sub-Second Data Low)	SUBSEC[1:0]		–	–	–	–	–	–
0x11	SUBSEC_H (Sub-Second Data High)	SUBSEC[9:2]							
0x12	SEC_MIR BCD mode (Mirrored Second Data, = 0x00)	–	SEC_H[2:0]			SEC_L[3:0]			
	SEC_BIN0 BIN mode (Second Binary Data 0,)	SEC_BIN[7:0]							
0x13	MIN_MIR BCD mode (Mirrored Minute Data, = 0x01)	–	MIN_H[2:0]			MIN_L[3:0]			
	SEC_BIN1 BIN mode (Second Binary Data 1,)	SEC_BIN[15:8]							
0x14	HOUR_MIR BCD mode (Mirrored Hour Data, = 0x02)	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
	SEC_BIN2 BIN mode (Second Binary Data 2,)	SEC_BIN[23:16]							
0x15	WEEKDAY_MIR BCD mode (Mirrored Day-of-Week Data, = 0x03)	–	WEEK[6:0]						
	SEC_BIN3 BIN mode (Second Binary Data 3,)	SEC_BIN[31:24]							
0x16	DAY_MIR BCD mode (Mirrored Day Data, = 0x04)	–	–	DAY_H[1:0]		DAY_L[3:0]			
	SEC_BIN4 BIN mode (Second Binary Data 4,)	–	–	–	–	–	–	–	SEC_BIN[32]
0x17	MONTH_MIR BCD mode (Mirrored Mont Data, = 0x05)	–	–	–	MONTH_H	MONTH_L[3:0]			
0x18	YEAR_MIR BCD mode (Mirrored Year Data, = 0x06)	YEAR_H[3:0]				YEAR_L[3:0]			
0x19	OFS_SUBSEC_H (Offset Sub-Second Data High)	OFS_ SUBSEC[0]	(GP)	(GP)	OFS_SUBSEC[9:5]				
0x1A	OFS_SUBSEC_L (Offset Sub-Second Data Low)	OFS_SUBSEC[4:0]					–	OFSFIN	OFSEN
0x1B	DIG_TRIM_H (Digital Trimming Data High)	DTRIM[8:1]							
0x1C	DIG_TRIM_L (Digital Trimming Data Low)	DTRIM[0]	–	–	–	–	–	–	DTRIMEN
0x1D	TCTL_MIR (Mirrored Timer Control, = 0x0D)	FSEL[1:0]		USEL0	TE	WADA	–	TSEL[1:0]	
0x1E	INTF_MIR (Mirrored Status Flag, = 0x0E)	PORF	OSCSTPF	UF	TF	AF	EVF	VLF	VTMPLF
0x1F	CNTSEL (Counter Select)	–	–	–	–	–	ACCBCD	BINCNTEN	BCDCNTEN

Bank 2

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	EVIN_EN (Event Input Enable)	–	–	–	EVIN2CPEN	EVIN1CPEN	–	EVIN2EN	EVIN1EN
0x21	EVIN1_CFG (EVIN1 Configuration)	–	–	–	PUPD[2:0]			POL[1:0]	
0x22	EVIN1_FLT (EVIN1 Noise Filter)	–	–	FLT[5:0]					
0x23	EVIN2_CFG (EVIN2 Configuration)	–	–	–	PUPD[2:0]			POL[1:0]	
0x24	EVIN2_FLT (EVIN2 Noise Filter)	–	–	FLT[5:0]					
0x27	BUF1_CFG1 (BUF1 Configuration 1)	BINSEL	OVWEN	–	–	–	FULLIEN	EMPTIEN	OVWIEN
0x28	BUF1_STAT (BUF1 Status)	FULLF	EMPTF	–	–	–	–	–	OVWF
0x29	BUF1_CFG2 (BUF1 Configuration 2)	–	SRAMMOD	–	–	–	–	–	–

Bank 3

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	ALM_SEC (Second Alarm)	XSAE	SALM_H[2:0]			SALM_L[3:0]			
0x31	ALM_MIN_MIR (Mirrored Minute Alarm, = 0x07)	XMAE	MALM_H[2:0]			MALM_L[3:0]			
0x32	ALM_HOUR_MIR (Mirrored our Alarm, = 0x08)	XHAE	(GP)	HALM_H[1:0]		HALM_L[3:0]			
0x33	ALM_WEEKDAY_MIR (Mirrored Day-of-Week Alarm / Day Alarm, = 0x09)	XWAE	WKALM[6:0]						
			(GP)	DALM_H[1:0]		DALM_L[3:0]			
0x34	UPDISEL (Time Update Interrupt Select)	–	–	–	–	–	–	USEL1	–
0x38	WTICFG (Wakeup Timer Interrupt Configuration)	PINMUX[1:0]		RSTOPT[1:0]		WTONETIM	TSEL2	WTIOUT	UPDOWN MOD
0x39	WTCTL (Wakeup Timer Control)	WTRST	EXWTRSTEN	WTRSTWIN[1:0]		WTMODSEL	WTSTOPCTL	–	WTSTOP
0x3A	WTCNT_L_MIR (Mirrored Wakeup Timer Counter Low, = 0x0A)	WTCNT[7:0]							
0x3B	WTCNT_M_MIR (Mirrored Wakeup Timer Counter Middle, = 0x0B)	WTCNT[15:8]							
0x3C	WTCNT_H_MIR (Mirrored Wakeup Timer Counter High, = 0x0C)	WTCNT[23:16]							
0x3D	TCTL_MIR (Mirrored Timer Control, = 0x0D)	FSEL[1:0]		USEL0	TE	WADA	–	TSEL[1:0]	
0x3E	INTF_MIR (Mirrored Status Flag, = 0x0E)	PORF	OSCSTPF	UF	TF	AF	EVF	VLF	VTMPLF
0x3F	TSTP_INTE_MIR (Mirrored Timer Stop and Interrupt Enable, = 0x0F)	CSEL[1:0]		UIE	TIE	AIE	EIE	–	STOP

Bank 4

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	WRCMD_CFG (Write Command Configuration)	EVCNT CLREN	–	–	BUF1F CLREN	–	–	–	CMDTRGEN
0x42	WRCMD_TRG (Write Command Trigger)	WRTRG[7:0]							
0x43	EVNT_INTE (Event Interrupt Enable)	–	EVIN2IEN	EVIN1IEN	RSTOIEN	–	VTMPLIEN	–	OSCSTPIEN
0x44	CAP_EN (Capture Enable)	–	–	–	RSTOCPEN	–	VTMPLCPEN	–	OSCSTP CPEN
0x45	INTF_MIR (Mirrored Status Flag, = 0x0E)	PORF	OSCSTPF	UF	TF	AF	EVF	VLF	VTMPLF
0x46	BUF_INTF (Buffer Interrupt Factor)	–	–	BUF1F	RSTOF	–	–	–	–
0x47	EVNT_INTF (Event Interrupt Factor)	–	EVIN2F	EVIN1F	RSTOEVF	–	VTMPLEVF	–	OSCSTPEVF

Bank 5

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x51	EVIN1_EVCNT (EVIN1 Event Counter)	–	–	EVCNT[5:0]					
0x52	EVIN2_EVCNT (EVIN2 Event Counter)	–	–	EVCNT[5:0]					
0x54	EVINMON (EVIN Monitor)	–	EVIN2MON	EVIN1MON	–	–	–	–	–
0x55	SOUTCTL (SOUT Control)	DCE	DC	–	–	SIGINV	SOUT[2:0]		

Bank 6/7 (when reading time stamp (BCD) data in Direct mode)

Settings when time stamp data is captured: BUF1_CFG1.BINSEL bit = 0, CNTSEL.BCDCNTEN bit = 1

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60 0x70	TIMESTAMP_SUBSEC_L (SUBSEC Time Stamp Data Low)	SUBSEC[1:0]		×	×	×	×	×	×
0x61 0x71	TIMESTAMP_SUBSEC_H (SUBSEC Time Stamp Data High)	SUBSEC[9:2]							
0x62 0x72	TIMESTAMP_SEC (SEC Time Stamp Data)	×	SEC_H[2:0]			SEC_L[3:0]			
0x63 0x73	TIMESTAMP_MIN (MIN Time Stamp Data)	×	MIN_H[2:0]			MIN_L[3:0]			
0x64 0x74	TIMESTAMP_HOUR (HOUR Time Stamp Data)	×	×	HOUR_H[1:0]		HOUR_L[3:0]			
0x65 0x75	TIMESTAMP_DAY (DAY Time Stamp Data)	×	×	DAY_H[1:0]		DAY_L[3:0]			
0x66 0x76	TIMESTAMP_MONTH (MONTH Time Stamp Data)	×	×	×	MONTH_H	MONTH_L[3:0]			
0x67 0x77	TIMESTAMP_YEAR (YEAR Time Stamp Data)	YEAR_H[3:0]				YEAR_L[3:0]			
0x68 0x78	TIMESTAMP_EVSTAT (Event Status Time Stamp Data)	×	EVIN2POL	EVIN1POL	×	RSTOSTAT	VTMPLSTAT	×	OSCSTP STAT
0x69 0x79	TIMESTAMP_TRG (Time Stamp Trigger Factor)	OVWFSTAT*	EVIN2TRG	EVIN1TRG	WRCMDTRG	RSTOTRG	VTMPLTRG	×	OSCSTPTRG

* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

Bank 6/7 (when reading time stamp data (BIN) in Direct mode)

Settings when time stamp data is captured: BUF1_CFG1.BINSEL bit = 1, CNTSEL.BINCNTEN bit = 1

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60 0x70	TIMESTAMP_SUBSEC_L (SUBSEC Time Stamp Data Low)	SUBSEC[1:0]		×	×	×	×	×	×
0x61 0x71	TIMESTAMP_SUBSEC_H (SUBSEC Time Stamp Data High)	SUBSEC[9:2]							
0x62 0x72	TIMESTAMP_SEC (SEC Time Stamp Data)	SEC_BIN[7:0]							
0x63 0x73	TIMESTAMP_MIN (MIN Time Stamp Data)	SEC_BIN[15:8]							
0x64 0x74	TIMESTAMP_HOUR (HOUR Time Stamp Data)	SEC_BIN[23:16]							
0x65 0x75	TIMESTAMP_DAY (DAY Time Stamp Data)	SEC_BIN[31:24]							
0x66 0x76	TIMESTAMP_MONTH (MONTH Time Stamp Data)	×	×	×	×	×	×	×	SEC_BIN32
0x67 0x77	TIMESTAMP_YEAR (YEAR Time Stamp Data)	×	×	×	×	×	×	×	×
0x68 0x78	TIMESTAMP_EVSTAT (Event Status Time Stamp Data)	×	EVIN2POL	EVIN1POL	×	RSTOSTAT	VTMPLSTAT	×	OSCSTP STAT
0x69 0x79	TIMESTAMP_TRG (Time Stamp Trigger Factor)	OVWFSTAT*	EVIN2TRG	EVIN1TRG	WRCMDTRG	RSTOTRG	VTMPLTRG	×	OSCSTPTRG

* OVWFSTAT exists only in Address 0x79 (not exist in Address 0x69).

Bank 6 (SRAM mode)

Setting when accessing to the SRAM: BUF1_CFG2.SRAMMOD bit = 1

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	SRAM Address 0x00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x61	SRAM Address 0x01								
0x62	SRAM Address 0x02								
0x63	SRAM Address 0x03								
0x64	SRAM Address 0x04								
0x65	SRAM Address 0x05								
0x66	SRAM Address 0x06								
0x67	SRAM Address 0x07								
0x68	SRAM Address 0x08								
0x69	SRAM Address 0x09								
0x6A	SRAM Address 0x0A								
0x6B	SRAM Address 0x0B								
0x6C	SRAM Address 0x0C								
0x6D	SRAM Address 0x0D								
0x6E	SRAM Address 0x0E								
0x6F	SRAM Address 0x0F								
0x70	SRAM Address 0x10	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x71	SRAM Address 0x11								
0x72	SRAM Address 0x12								
0x73	SRAM Address 0x13								
0x74	SRAM Address 0x14								
0x75	SRAM Address 0x15								
0x76	SRAM Address 0x16								
0x77	SRAM Address 0x17								
0x78	SRAM Address 0x18								
0x79	SRAM Address 0x19								
0x7A	SRAM Address 0x1A								
0x7B	SRAM Address 0x1B								
0x7C	SRAM Address 0x1C								
0x7D	SRAM Address 0x1D								
0x7E	SRAM Address 0x1E								
0x7F	SRAM Address 0x1F								

4.2 Description of Registers

*1 "x" in the initial value row indicates that the initial value is undefined.

*2 [BCD mode] indicates that the register can only be used in BCD mode (CNTSEL.ACCBCD bit = 1, CNTSEL. BCDCNTEN bit = 1).
[BIN mode] indicates that the register can only be used in BIN mode (NTSEL.ACCBCD bit = 0, CNTSEL.BINCNTEN bit = 0).

0x00: SEC (Second Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	SEC_H[2:0]			SEC_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

Bits 6–4: SEC_H[2:0]
Bits 3–0: SEC_L[3:0]

The second counter value can be set or read through these bits.
The SEC_H[2:0] bits are the BCD code (0–5) of the 10-second digit and the SEC_L[3:0] bits are the BCD code (0–9) of the 1-second digit. Writing second data to this address resets the 1/1024-second counter and clears Registers SUBSEC_L and SUBSEC_H to 0.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x01: MIN (Minute Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	MIN_H[2:0]			MIN_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

Bits 6–4: MIN_H[2:0]
Bits 3–0: MIN_L[3:0]

The minute counter value can be set or read through these bits.
The MIN_H[2:0] bits are the BCD code (0–5) of the 10-minute digit and the MIN_L[3:0] bits are the BCD code (0–9) of the 1-minute digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x02: HOUR (Hour Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

Bits 5–4: HOUR_H[1:0]
Bits 3–0: HOUR_L[3:0]

The hour counter value can be set or read through these bits.
The HOUR_H[1:0] bits are the BCD code (0–2) of the 10-hour digit and the HOUR_L[3:0] bits are the BCD code (0–9) of the 1-hour digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x03: WEEKDAY (Day-of-Week Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	WEEK[6:0]						
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W						

Bits 6–0: WEEK[6:0]

The day-of-week counter value can be set or read through these bits.
Each WEEK[6:0] bit one-to-one corresponds to a day of the week as the setting example shown below. Therefore, only one bit corresponding to today must be set. The WEEK[6:0] bits are shifted one bit to the left at the same time the day counter is updated (bit 6 is shifted to bit 0).

Example of day of week setting

WEEK6	WEEK5	WEEK4	WEEK3	WEEK2	WEEK1	WEEK0
Saturday (0x40)	Friday (0x20)	Thursday (0x10)	Wednesday (0x08)	Tuesday (0x04)	Monday (0x02)	Sunday (0x01)

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x04: DAY (Day Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	DAY_H[1:0]		DAY_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

Bits 5–4: DAY_H[1:0]
Bits 3–0: DAY_L[3:0]

The day counter value can be set or read through these bits.
The DAY_H[1:0] bits are the BCD code (0–3) of the 10-day digit and the DAY_L[3:0] bits are the BCD code (0–9) of the 1-day digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

*2 For the behavior of the register at leap years, refer to "*Leap Year Determination*" in Section 3.3.

0x05: MONTH (Month Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	MONTH_H	MONTH_L[3:0]			
Initial value	0	0	0	x	x	x	x	x
R/W	R	R	R	R/W	R/W			

Bit 4: MONTH_H
Bits 3–0: MONTH_L[3:0]

The month counter value can be set or read through these bits.
The MONTH_H bits are the BCD code (0–1) of the 10-month digit and the MONTH_L[3:0] bits are the BCD code (0–9) of the 1-month digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x06: YEAR (Year Data) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	YEAR_H[3:0]				YEAR_L[3:0]			
Initial value	x	x	x	x	x	x	x	x
R/W	R/W				R/W			

Bits 7–4: YEAR_H[3:0]
Bits 3–0: YEAR_L[3:0]

The year counter value can be set or read through these bits.
The YEAR_H[3:0] bits are the BCD code (0–9) of the 10-year digit and the YEAR_L[3:0] bits are the BCD code (0–9) of the 1-year digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x07: ALM_MIN (Minute Alarm) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XMAE**	**MALM_H[2:0]**			**MALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W			R/W			

Bit 7: XMAE

This bit enables/disables the minute alarm setting.

1 (R/W): Minute alarm is disabled.
0 (R/W): Minute alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the minute counter value and the setting value of the MALM_H[2:0] and MALM_L[3:0] bits is included in the alarm generation condition.

Bits 6–4: MALM_H[2:0]
Bits 3–0: MALM_L[3:0]

These bits set the minute alarm condition in a BCD code.
The MALM_H[2:0] bits specify the 10-minute digit (0–5) and the MALM_L[3:0] bits specify 1-minute digit (0–9).

*1 For more information on the alarm function, refer to "*3.6 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from occurring.

0x08: ALM_HOUR (Hour Alarm) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XHAE**	**(GP)**	**HALM_H[1:0]**		**HALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

Bit 7: XHAE

This bit enables/disables the hour alarm setting.

1 (R/W): Hour alarm is disabled.
0 (R/W): Hour alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the hour counter value and the setting value of the HALM_H[1:0] and HALM_L[3:0] bits is included in the alarm generation condition.

Bits 5–4: HALM_H[1:0]
Bits 3–0: HALM_L[3:0]

These bits set the hour alarm condition in a BCD code.
The HALM_H[1:0] bits specify the 10-hour digit (0–2) and the HALM_L[3:0] bits specify 1-hour digit (0–9).

*1 For more information on the alarm function, refer to "*3.6 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x09: ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm) [BCD mode]

Day-of-Week Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**WKALM[6:0]**						
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W						

Day Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**(GP)**	**DALM_H[1:0]**		**DALM_L[3:0]**			

Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

Note: This register switches its function according to the TCTL.WADA bit setting.
TCTL.WADA bit = 0: Day-of-Week Alarm
TCTL.WADA bit = 1: Day Alarm

Bit 7: XWAE

This bit enables/disables the day-of-week or day alarm setting.

1 (R/W): Day-of-week/day alarm is disabled.
0 (R/W): Day-of-week/day alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and an alarm will be generated if the following condition is met.

TCTL.WADA bit = 0: The same bit in the day-of-week counter as one that has been set within WKALM[6:0] is set.

TCTL.WADA bit = 1: The day counter value matches with the DALM_H[1:0]/DALM_L[3:0] bit setting value.

Bits 6–0: WKALM[6:0] (Day-of-Week Alarm)

These bits set the day-of-week alarm condition.
More than one bit can be set to specify two or more days of the week.

Bits 5–4: DALM_H[1:0] (Day Alarm)
Bits 3–0: DALM_L[3:0] (Day Alarm)

These bits set the day alarm condition in a BCD code.
The DALM_H[1:0] bits specify the 10-day digit (0–3) and the DALM_L[3:0] bits specify 1-day digit (0–9).

*1 For more information on the alarm function, refer to "*3.6 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x0A: WTCNT_L (Wakeup Timer Counter Low)
0x0B: WTCNT_M (Wakeup Timer Counter Middle)
0x0C: WTCNT_H (Wakeup Timer Counter High)

Wakeup Timer Counter Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[7:0]**							
Initial value	0	0	0	0	0	0	0	1
R/W	R/W							

Wakeup Timer Counter Middle

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[15:8]**							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Wakeup Timer Counter High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[23:16]**							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Bits 7–0: WTCNT[7:0] (Wakeup Timer Counter Low)
WTCNT[15:8] (Wakeup Timer Counter Middle)
WTCNT[23:16] (Wakeup Timer Counter High)

When writing
These registers set the preset value for the wakeup timer counter. The wakeup timer allows setting of a preset value within the range from 1 to 16777215 and uses it as the count period.
When the counter exceeds the preset value by counting up in Count-up mode, the initial value (1) is loaded to the counter and the counting up continues.

When the counter reaches 0 by counting down in Count-down mode, the preset value is loaded to the counter and the counting down continues.

Notes: • Make sure the TCTL.TE bit = 0 (wakeup timer disabled) before setting a preset value.

• The preset data cannot be set to 0x000000. If 0x000000 is written to Registers WTCNT_L, WTCNT_M, and WTCNT_H, the wakeup timer cannot perform counting up/down and an interrupt does not occur. The counter value is read as 0x000001 regardless of how the TCTL.TE bit is set (0 or 1).

When reading

When the TCTL.TE bit = 1 (wakeup timer enabled), the current counter value is read out from these registers. This counter has a read buffer function, so the correct value can be obtained in any time by reading these three registers successively even if the wakeup timer is operating.
When the TCTL.TE bit = 0 (wakeup timer disabled), the currently set preset value is read out.

*1 For more information on the wakeup timer function, refer to "*3.7 Wakeup Timer Function*."

*2 When the wakeup timer is not used (both the TCTL.TE and TSTP_INTE.TIE bits are set to 0), these registers can be used as readable/writable general-purpose registers.

0x0D: TCTL (Timer Control)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	FSEL[1:0]		USEL0	TE	WADA	–	TSEL[1:0]	
Initial value	0	0	0	0	0	0	1	0
R/W	R/W		R/W	R/W	R/W	R	R/W	

Bits 7–6: FSEL[1:0]

These bits select an FOUT frequency.

Table 4.1 FOUT Output Clock Selections

TCTL.FSEL[1:0]	Output clock
0b00	32.768 kHz (default)
0b01	1024 Hz
0b10	1 Hz
0b11	Off

Bit 5: USEL0

This bit selects a time update interrupt event by using in conjunction with the UPDISEL.USEL1 bit.

Table 4.2 Time Update Interrupt Event Selections

UPDISEL.USEL1	TCTL.USEL0	Interrupt event
0	0	Second counter update (default)
0	1	Minute counter update
1	0	Hour counter update
1	1	No interrupt event

Bit 4: TE

This bit enables/disables wakeup timer interrupts.

1 (R/W): Wakeup timer interrupts are enabled.
0 (R/W): Wakeup timer interrupts are disabled.

Bit 3: WADA

This bit selects either day-of-week alarm or day alarm to be used as an alarm generation condition.

1 (R/W): Day alarm
0 (R/W): Day-of-week alarm

Bits 1–0: TSEL[1:0]

These bits select an internal clock used as the source clock of the wakeup timer.

Table 4.3 Wakeup Timer Source Clock Selections

TCTL.TSEL[1:0]	Source clock
0b00	1024 Hz
0b01	64 Hz
0b10	1 Hz (default)
0b11	1/60 Hz

This setting is effective when the WTICFG.TSEL2 bit = 0. When the WTICFG.TSEL2 bit = 1, the external clock input to the EVIN2 pin is used as the source clock.

*1 For more information on the FOUT function, refer to "*3.8 FOUT Output Function*."

*2 For more information on the time update interrupt, refer to "*3.5 Time Update Interrupt Function*."

*3 For more information on the wakeup timer function, refer to "*3.7 Wakeup Timer Function*."

*4 For more information on the alarm function, refer to "*3.6 Alarm Function*."

0x0E: INTF (Status Flag)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PORF**	**OSCSTPF**	**UF**	**TF**	**AF**	**EVF**	**VLF**	**VTMPLF**
Initial value	1	1	x	x	x	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: PORF

This is a self-monitoring flag that indicates whether a power-on-reset is executed after power is turned on or not.

1 (R): Power-on-reset has been detected.
0 (R): No power-on-reset has been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when power-on reset has been cancelled)

Bit 6: OSCSTPF

This is a self-monitoring flag that indicates whether the oscillation of the crystal oscillator has stopped or not.

1 (R): Oscillation stop state has been detected. (Set to 1 by detecting an oscillation stop for 10 ms or more.)
0 (R): Oscillator stop state has not been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when an oscillation stop state has not been detected)

Bit 5: UF
Bit 4: TF
Bit 3: AF
Bit 2: EVF

They are interrupt flags that indicate occurrence of an RTC interrupt event.

1 (R): Interrupt event has occurred.
0 (R): No interrupt event has occurred.
1 (W): Ineffective
0 (W): Flag clear (except for EVF)

The following shows the correspondence between the bit and interrupt:

UF: Time update interrupt
TF: Wakeup timer interrupt
AF: Alarm interrupt
EVF: Time stamp event detection interrupt

In the wakeup timer (TF), time update (UF), and alarm (AF) interrupts, clearing the flag by writing 0 negates the /INT signal (low to Hi-Z).
The low output from /INT by a wakeup timer or time update interrupt event is automatically cancelled after a prescribed time has elapsed from occurrence of an interrupt event. However, the interrupt flag (TF or UF) is not automatically cleared.

Various events that generate an interrupt exist in the event detection and time stamp functions, and the interrupt flags that are set when the corresponding event occurs are assigned in Registers BUF_INTF and EVNT_INTF. The EVF bit is set to 1 at the same time one or more interrupt flags are set and it is cleared to 0 when all the flags in Registers BUF_INTF and EVNT_INTF are cleared (it is not cleared by writing 0). This clear operation also negates the /INT signal.

Bit 1: VLF

This is a self-monitoring flag that indicates an abnormality of the RA4000CE/RA8000CE .

1 (R): There is an abnormality. (PORF bit = 1 or OSCSTPF bit = 1)
0 (R): No abnormality
1 (W): Ineffective
0 (W): Flag clear (effective only when power-on reset has been cancelled and an oscillation stop state has not been detected)

Bit 0: VTMPLF

This is a self-monitoring flag that indicates the history of a V_{DD} voltage drop to the temperature compensation update stop voltage or less ($V_{DD} \leq V_{DET2}$).

1 (R): Voltage drop has been detected. ($V_{DD} \leq V_{DET2}$, temperature compensation update stopped)
0 (R): Voltage drop has not been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when the V_{DD} voltage is normal)

*1 For more information on the self-monitoring function, refer to "*3.10 Self-Monitoring Function*."

*2 For more information on the interrupts, refer to "*3.5 Time Update Interrupt Function*," "*3.7 Wakeup Timer Function*," "*3.6 Alarm Function*," or "*3.11 Time Stamp Function*."

0x0F: TSTP_INTE (Timer Stop and Interrupt Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**CSEL[1:0]**		**UIE**	**TIE**	**AIE**	**EIE**	**–**	**STOP**
Initial value	0	1	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R	R/W

Bits 7–6: CSEL[1:0]

These bits set the execution interval of the temperature sensor measurement operation.

Table 4.4 Execution Interval of Temperature Sensor Measurement Operation

TSTP_INTE.CSEL[1:0]	Execution interval
0b00	0.5 seconds
0b01	2.0 seconds (default)
0b10	10.0 seconds
0b11	30.0 seconds

Bit 5: UIE
Bit 4: TIE
Bit 3: AIE
Bit 2: EIE

These bits enable the RA4000CE/RA8000CE interrupts.

1 (R/W): Interrupts are enabled.
0 (R/W): Interrupts are disabled. (The interrupt signal is cleared. Note)

Each bit corresponds to an interrupt as shown below.

UIE: Time update interrupt
TIE: Wakeup timer interrupt
AIE: Alarm interrupt
EIE: Time stamp event detection interrupt

Bit 0: STOP

This bit controls the counter operations.

1 (W): Stops operating of the counters.
0 (W): Starts operating of the counters.
1 (R): The timer is idle.
0 (R): The timer is operating.

The STOP bit stops the following operations:

1) 1/1024-second , second, minute, day, day of week, month, and year counters, and binary second counter update operations
Consequently, a time update interrupt and an alarm interrupt do not occur.
The time stamp function uses the time at the point the counters stop as the clock data.

2) Wakeup timer interrupt
The wakeup timer stops and does not generate an interrupt.

3) FOUT output
The FOUT output fixed at H or L when 1 Hz output is selected.
When 32.768 kHz or 1024 Hz is selected, the output continues even if the STOP bit = 1.

Note: If the timer is stopped by the STOP bit when reading clock/calendar data, time error is increased. Therefore, do not stop the counter using the STOP bit when reading the clock/calendar registers.

*1 For more information on the temperature compensation operation, refer to "*3.3 Temperature Compensation Function*."

*2 For more information on the interrupts, refer to "*3.5 Time Update Interrupt Function*," "*3.7 Wakeup Timer Function*," "*3.6 Alarm Function*," or "*3.11 Time Stamp Function*."

0x10: SUBSEC_L (Sub-Second Data Low)
0x11: SUBSEC_H (Sub-Second Data High)

Sub-Second Data Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**SUBSEC[1:0]**		–	–	–	–	–	–
Initial value	x	x	0	0	0	0	0	0
R/W	R/W		R	R	R	R	R	R

Sub-Second Data High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**SUBSEC[9:2]**							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Bits 7–6: SUBSEC[1:0] (Sub-Second Data Low)
Bits 7–0: SUBSEC[9:2] (Sub-Second Data High)

These bits are used to set and read the 1/1024-second counter, which is a 10-bit binary counter.
The SUBSEC_L.SUBSEC[1:0] bits are the low-order 2 bits of the 1/1024-second counter and the SUBSEC_H. SUBSEC[9:2] bits are the high-order 8 bits.

Table 4.5 SUBSEC[9:0] bits

Bit	SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2	SUBSEC1	SUBSEC0
Count value (1024 Hz cycle)	512	256	128	64	32	16	8	4	2	1

To obtain or change the 1/1024-second counter value, read or write these two addresses successively. By accessing Addresses 0x12 to 0x18 following it, the clock/calendar data can be read/written continuously.
Writing data to Register SEC (Address 0x00, BCD mode) resets the 1/1024-second counter, as a result, Registers SUBSEC_L and SUBSEC_H are cleared to 0. On the other hand, writing data to Register SEC_MIR (Address 0x12), which is the mirror address of Register SEC, does not reset the 1/1024-second counter.

*1 For more information on the sub-second counter, refer to "*3.2 Clock and Calendar Function*."

0x12: SEC_MIR (Mirrored Second Data, = 0x00) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	SEC_H[2:0]			SEC_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

This is a mirror register of Register SEC. For more information, refer to "*0x00: SEC (Second Data)*." However, writing to this address does not reset the 1/1024-second counter.

0x13: MIN_MIR (Mirrored Minute Data, = 0x0h) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	MIN_H[2:0]			MIN_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

This is a mirror register of Register MIN. For more information, refer to "*0x01: MIN (Minute Data)*."

0x14: HOUR_MIR (Mirrored Hour Data, = 0x02) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

This is a mirror register of Register HOUR. For more information, refer to "*0x02: HOUR (Hour Data)*."

0x15: WEEKDAY_MIR (Mirrored Day-of-Week Data, = 0x03) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	WEEK[6:0]						
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W						

This is a mirror register of Register WEEKDAY. For more information, refer to "*0x03: WEEKDAY (Day-of-Week Data)*."

0x16: DAY_MIR (Mirrored Day Data, = 0x04) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	DAY_H[1:0]		DAY_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

This is a mirror register of Register DAY. For more information, refer to "*0x04: DAY (Day Data)*."

0x17: MONTH_MIR (Mirrored Month Data, = 0x05) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	MONTH_H	MONTH_L[3:0]			
Initial value	0	0	0	x	x	x	x	x
R/W	R	R	R	R/W	R/W			

This is a mirror register of Register MONTH. For more information, refer to "*0x05: MONTH (Month Data)*."

0x18: YEAR_MIR (Mirrored Year Data, = 0x06) [BCD mode]

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	YEAR_H[3:0]				YEAR_L[3:0]			
Initial value	x	x	x	x	x	x	x	x
R/W	R/W				R/W			

This is a mirror register of Register YEAR. For more information, refer to "*0x06: YEAR (Year Data)*."

0x12: SEC_BIN0 (Second Binary Data 0) [BIN mode]
0x13: SEC_BIN1 (Second Binary Data 1) [BIN mode]
0x14: SEC_BIN2 (Second Binary Data 2) [BIN mode]
0x15: SEC_BIN3 (Second Binary Data 3) [BIN mode]
0x16: SEC_BIN4 (Second Binary Data 4) [BIN mode]

Second Binary Data 0

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	SEC_BIN[7:0]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Second Binary Data 1

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	SEC_BIN[15:8]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Second Binary Data 2

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	SEC_BIN[23:16]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Second Binary Data 3

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	SEC_BIN[31:24]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Second Binary Data 4

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	–	–	–	–	SEC_BIN[32]
Initial value	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R/W

Bits 7–0: SEC_BIN[7:0] (Second Binary Data 0)
SEC_BIN[15:8] (Second Binary Data 1)
SEC_BIN[23:16] (Second Binary Data 2)
SEC_BIN[31:24] (Second Binary Data 3)
Bit 0: SEC_BIN[32] (Second Binary Data 4)

The BIN counter value can be set or read through these bits.
Writing second data to these registers does not clear Registers SUBSEC_L and SUBSEC_H to 0.
These registers can be accessed when Register CNTSEL = 0x3 or 0x2.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x19: OFS_SUBSEC_H (Offset Sub-Second Data High)
0x1A: OFS_SUBSEC_L (Offset Sub-Second Data Low)

Offset Sub-Second Data High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	OFS_SUBSEC[10]	(GP)	(GP)	OFS_SUBSEC[9:5]				
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W				

Offset Sub-Second Data Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	OFS_SUBSEC[4:0]					–	OFSFIN	OFSEN
Initial value	0	0	0	0	0	0	1	0
R/W	R/W					R	R	W

Bit 7: OFS_SUBSEC[10] (Offset Sub-Second Data High)
Bits 4–0: OFS_SUBSEC[9:5] (Offset Sub-Second Data High)
Bits 7–3: OFS_SUBSEC[4:0] (Offset Sub-Second Data Low)

These bits are used to set the offset value for adjusting 1/1024-second time. To directly add the offset value to the 1/1024-second counter, it must be calculated as a 2's complement value with 11-bit data length and set the Bit 10 to the OFS_SUBSEC [10] bit and Bits 9 to 0 to the OFS_SUBSEC[9:0] bits.

Bit 1 OFSFIN (Offset Sub-Second Data Low)

This bit indicates the operation status of the 1/1024-second offset correction.

1 (R): Offset correction has completed. / Ready for offset correction.
0 (R): Offset correction is in progress.

Bit 0 OFSEN (Offset Sub-Second Data Low)

This bit starts a 1/1024-second offset correction.

1 (W): Start offset correction
0 (W): Ineffective

The offset value will be reflected to the 1/1024-second counter when the second counter is updated immediately after this writing. This processing is performed only once and will not be performed at the subsequent updates of the second counter.

*1 For the 1/1024-second offset correction procedure, refer to "*1/1024-Second Offset Time Adjustment*" in Section 3.2.

0x1B: DIG_TRIM_H (Digital Trimming Data High)
0x1C: DIG_TRIM_L (Digital Trimming Data Low)

Digital Trimming Data High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	DTRIM[8:1]							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Digital Trimming Data Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**DTRIM[0]**	**–**	**–**	**–**	**–**	**–**	–	**DTRIMEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R/W

Bits 7–0: DTRIM[8:1] (Digital Trimming Data High)
Bit 7: DTRIM[0] (Digital Trimming Data Low)

These bits are used to set the correction value in 2's complement when performing a theoretical regulation.

Bit 0 DTRIMEN (Digital Trimming Data Low)

This bit enables/disables the theoretical regulation function.

1 (R/W): Theoretical regulation function is enabled.
0 (R/W): Theoretical regulation function is disabled.

*1 For more information on the theoretical regulation function, refer to "*3.4 Theoretical Regulation Function*."

0x1D: TCTL_MIR (Mirrored Timer Control, = 0x0D)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FSEL[1:0]**		**USEL0**	**TE**	**WADA**	**–**	**TSEL[1:0]**	
Initial value	0	0	0	0	0	0	1	0
R/W	R/W		R/W	R/W	R/W	R	R/W	

This is a mirror register of Register TCTL. For more information, refer to "*0x0D: TCTL (Timer Control)*."

0x1E: INTF_MIR (Mirrored Status Flag, = 0x0E)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PORF**	**OSCSTPF**	**UF**	**TF**	**AF**	**EVF**	**VLF**	**VTMPLF**
Initial value	1	1	x	x	x	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a mirror register of Register INTF. For more information, refer to "*0x0E: INTF (Status Flag)*."

0x1F: CNTSEL (Counter Select)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**–**	**–**	**–**	**–**	**–**	**ACCBCD**	**BINCNTEN**	**BCDCNTEN**
Initial value	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R/W	R/W	R/W

Bit 2: ACCBCD

This bit selects a clock/calendar counter access mode (selects whether to access the BCD counters [Registers SEC to YEAR] or BIN counter [Registers SEC_BIN*n*]).

1 (R/W): BCD mode (to read/write the BCD counters)
0 (R/W): BIN mode (to read/write the BIN counter)

Bit 1: BINCNTEN

This bit enables/disables the BIN counter to operate.

1 (R/W): BIN counter is enabled.
0 (R/W): BIN counter is disabled.

Bit 0: BCDCNTEN

This bit enables/disables the BCD counters to operate.

1 (R/W): BCD counters are enabled.
0 (R/W): BCD counters are disabled.

*1 For more information on the counter access mode, refer to "*3.2 Clock and Calendar Function*."

0x20: EVIN_EN (Event Input Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	**EVIN2CPEN**	**EVIN1CPEN**	–	**EVIN2EN**	**EVIN1EN**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R	R/W	R/W

Bit 4 EVIN2CPEN
Bit 3 EVIN1CPEN

These bits enable/disable external event trigger inputs from the EVIN*n* pin to capture time stamp data to the buffer.

1 (R/W): EVIN*n* is enabled to capture time stamp data.
0 (R/W): EVIN*n* is disabled to capture time stamp data.

The EVIN*n*CPEN bit setting is effective when the EVIN*n*EN bit (described below) = 1.

Bit 1 EVIN2EN
Bit 0 EVIN1EN

These bits enable/disable the EVIN*n* pin to input external event triggers.

1 (R/W): EVIN*n* is enabled to input event triggers.
0 (R/W): EVIN*n* is disabled to input event triggers.

*1 For more information on the time stamp function, refer to "*3.11 Time Stamp Function*."

0x21: EVIN1_CFG (EVIN1 Configuration)
0x23: EVIN2_CFG (EVIN2 Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	**PUPD[2:0]**			**POL[1:0]**	
Initial value	0	0	0	0	1	0	0	0
R/W	R	R	R	R/W			R/W	

Bits 4–2: PUPD[2:0]

These bits select an internal pull-up or pull-down resistor to be connected to the EVIN*n* pin.

Table 4.6 EVIN*n* Pin Pull-Up/Pull-Down Resistor Selections

EVIN*n*_CFG.PUPD[2:0]	Pull-up/down resistor
0b000	No pull-up/pull-down resistor
0b001	Pull-up resistor 500 kΩ
0b010	Pull-up resistor 1 MΩ (default)
0b011	Pull-up resistor 10 MΩ
0b100	Pull-down resistor 500 kΩ
Other	No pull-up/pull-down resistor

Bits 1–0: POL[1:0]

These bits select the EVIN*n* input signal detection edge polarity that captures time stamp data.

Table 4.7 Selecting EVIN*n* Input Signal Detection Edge Polarity

EVIN*n*_CFG.POL[1:0]	Detection clock polarity
0b00	Falling edge (default)
0b01	Rising edge
0b10	Rising and falling edges
0b11	

*1 For more information on the time stamp function, refer to "*3.11 Time Stamp Function*."

0x22: EVIN1_FLT (EVIN1 Noise Filter)
0x24: EVIN2_FLT (EVIN2 Noise Filter)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	FLT[5:0]					
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R/W					

Bits 5–0: FLT[5:0]

These bits set the noise filtering time for the EVIN*n* input signals.

Table 4.8 Noise Filtering Time for EVIN*n* Input

EVIN*n*_FLT. FLT[5:0]	Uncertain EVIN*n* pulse width (Whether the edge input is detected or not depends on the relationship between the edge input timing and the sampling timing in 125 ms cycles.)	Valid EVIN*n* pulse width (The edge input is always detected.)
0x00	–	1 ms or more
0x01 (Setting prohibited)	–	–
0x02	125 ms or more and less than 250 ms	250 ms or more
0x03	250 ms or more and less than 375 ms	375 ms or more
:	:	:
0x27	4750 ms or more and less than 4875 ms	4875 ms or more
0x28	4875 ms or more and less than 5000 ms	5000 ms or more
0x29 or more (Setting prohibited)	–	–

*1 For more information on the time stamp function, refer to "*3.11 Time Stamp Function*."

0x27: BUF1_CFG1 (BUF1 Configuration 1)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	BINSEL	OVWEN	–	–	–	FULLIEN	EMPTIEN	OVWIEN
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit 7: BINSEL

This bit selects either the BCD counter or the BIN counter to capture date and time data to be recorded to the buffer when an event occurs.

1 (R/W): BIN counter data is captured.
0 (R/W): BCD counter data is captured.

Bit 6: OVWEN

This bit sets the write mode after the buffer becomes full (after captured data is written to Bank 7).

1 (R/W): Overwrite mode (Bank 7 is overwritten.)
0 (R/W): Overwrite Inhibit mode (recording stops in buffer full state, captured data are discarded.)

Bit 2: FULLIEN

This bit enables/disables buffer full interrupts.

1 (R/W): Buffer full interrupts are enabled.
0 (R/W): Buffer full interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1_STAT.FULLF bit) will be set to 1 if a buffer full status occurs.

Bit 1: EMPTIEN

This bit enables/disables buffer not empty interrupts.

1 (R/W): Buffer not empty interrupts are enabled.
0 (R/W): Buffer not empty interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1_STAT.EMPTF bit) will be set to 1 if time stamp data is written to the buffer in empty status.

Bit 0: OVWIEN

This bit enables/disables buffer overwrite interrupts.

1 (R/W): Buffer overwrite interrupts are enabled.
0 (R/W): Buffer overwrite interrupts are disabled.

When this bit is set to 1, the interrupt flag (BUF1_STAT.OVWF bit) will be set to 1 if a time stamp is captured while the buffer is in full status.

*1 For more information on the time stamp function, refer to "*3.11 Time Stamp Function*."

0x28: BUF1_STAT (BUF1 Status)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FULLF**	**EMPTF**	**–**	**–**	**–**	**–**	**–**	**OVWF**
Initial value	0	1	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit 7: FULLF

This flag indicates whether the buffer is in full status or not.

1 (R): Buffer full status
0 (R): Free space available in the buffer

This flag is set to 1 if a newly captured time stamp data is written to the Bank 7 buffer when data has been written to the Bank 6 buffer only.

Bit 6: EMPTF

This flag indicates whether the buffer is in empty status or not.

1 (R): Buffer empty status
0 (R): Buffer data available

This flag is initially set to 1 and cleared to 0 when the 1st captured time stamp data is written to the Bank 6 buffer.

Bit 0: OVWF

This flag indicates whether a new time stamp data is captured or not while the buffer is in full status.

Overwrite Inhibit mode
1 (R): Data has been captured while the buffer is in full status (the latest data was destroyed).
0 (R): Data has not been captured after the buffer becomes full.

Overwrite mode
1 (R): Overwriting has occurred (Bank 7 was overwritten with the latest data).
0 (R): Overwriting has not occurred.

This flag is set to 1 when a new time stamp data is captured while the buffer is in full status.

Note: The flags in this register cannot be reset by reading the buffer. To reset the flags, it is necessary to issue a command trigger (writing to Register WRCMD_TRG) with the WRCMD_CFG. BUF1FCLREN bit set to 1.

*1 For more information on the time stamp function, refer to "*3.11 Time Stamp Function*."

0x29: BUF1_CFG2 (BUF1 Configuration 2)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	SRAMMOD	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R	R	R	R	R	R

Bit 6: SRAMMOD

This bit enables/disables SRAM mode for reading/writing from/to the buffer.

1 (R/W): SRAM mode is enabled.
0 (R/W): SRAM mode is disabled.

*1 For more information on the time stamp function and how to read/write the SRAM/buffer, refer to "*3.11 Time Stamp Function*."

0x30: ALM_SEC (Second Alarm)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	XSAE	SALM_H[2:0]			SALM_L[3:0]			
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W			R/W			

Bit 7: XSAE

This bit enables/disables the second alarm setting.

1 (R/W): Second alarm is disabled.
0 (R/W): Second alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the second counter value and the setting value of the SALM_H[2:0] and SALM_L[3:0] bits is included in the alarm generation condition.

Bits 6–4: SALM_H[2:0]
Bits 3–0: SALM_L[3:0]

These bits set the second alarm condition in a BCD code.
The SALM_H[2:0] bits specify the 10-second digit (0–5) and the SALM_L[3:0] bits specify 1-second digit (0–9).

*1 For controlling the alarm function, refer to "*3.6 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x31: ALM_MIN_MIR (Mirrored Minute Alarm, = 0x07)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	XMAE	MALM_H[2:0]			MALM_L[3:0]			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W			R/W			

This is a mirror register of Register ALM_MIN. For more information, refer to "*0x07: ALM_MIN (Minute Alarm)*."

0x32: ALM_HOUR_MIR (Mirrored Hour Alarm, = 0x08)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	XHAE	(GP)	HALM_H[1:0]		HALM_L[3:0]			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

This is a mirror register of Register ALM_HOUR. For more information, refer to "*0x08: ALM_HOUR (Hour Alarm)*."

0x33: ALM_WEEKDAY_MIR (Mirrored Day-of-Week Alarm / Day Alarm, = 0x09)

Mirrored Day-of-Week Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**WKALM[6:0]**						
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W						

Mirrored Day Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**(GP)**	**DALM_H[1:0]**		**DALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

This is a mirror register of Register ALM_WEEKDAY. For more information, refer to "*0x09: ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm)*."

0x34: UPDISEL (Time Update Interrupt Select)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**–**	**–**	**–**	**–**	**–**	**–**	**USEL1**	**–**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R

Bit 1: USEL1

This bit selects a time update interrupt event by using it together with the TCTL.USEL0 bit (see Table 4.2.).

0x38: WTICFG (Wakeup Timer Interrupt Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PINMUX[1:0]**		**RSTOPT[1:0]**		**WTONETIM**	**TSEL2**	**WTIOUT**	**UPDOWNMOD**
Initial value	0/1	0/1	0	0	0	0	0	0
R/W	R/W		R/W		R/W	R/W	R/W	R/W

Bits 7–6: PINMUX[1:0]

Be sure to avoid changing these bits from the initial value, otherwise, unexpected pin functions may be assigned.

Table 4.9 lists the initial values different by each model and option.

Table 4.9 WTICFG.PINMUX[1:0] Bit Initial Value of Each Product

Product name	Interface	WTICFG.PINMUX[1:0] initial value
RA4000CE Option A YB	3-wire SPI	0b01
RA4000CE Option B YB		0b01
RA4000CE Option C YB		0b00
RA4000CE Option D YB	4-wire SPI	0b00
RA4000CE Option E YB		0b00
RA8000CE Option A YB	I^2C-Bus	0b01
RA8000CE Option B YB		0b01
RA8000CE Option C YB		0b00
RA8000CE Option D YB		0b10

Bits 5–4: RSTOPT[1:0]

These bits select whether to disable the inputs/outputs or not while the reset signal (/RST) is being output.

When the input pins are disabled, they can be placed into a Hi-Z state.
When the output pins are disabled, they go into a Hi-Z state.

Disable: Inputs/outputs are disabled while /RST = L (power supply voltage drop is detected).
Enable: Inputs/outputs are not disabled while /RST = L (power supply voltage drop is detected).

This function is effective only in the models with the /RST pin function.

Table 4.10 Selecting Reset Output Option

WTICFG. RSTOPT[1:0]	FOE, CE, CLK, DI (DIO), SCL, SDA pin inputs DO pin output	FOUT, /INT, SOUT pin outputs
0b00	Disabled (default)	Disabled (default)
0b01	Disabled	Enabled
0b10	Enabled	Disabled
0b11	Enabled	Enabled

Bit 3: WTONETIM

This bit selects whether to automatically negate the /INT output or not after a wakeup timer interrupt occurs.

1 (R/W): Not negated automatically (low output)
0 (R/W): Negated automatically (7.812 ms width low pulse output)

Bit 2: TSEL2

This bit selects an external clock as the wakeup timer source clock.

1 (R/W): External clock input to the EVIN2 pin
0 (R/W): Internal clock selected with the TCTL.TSEL[1:0] bits

Bit 1: WTIOUT

This bit selects the wakeup timer interrupt signal output pin.

1 (R/W): Output from the FOUT pin (CMOS buffer output)
0 (R/W): Output from the /INT pin (N-ch. open drain output)

Note: When the FOUT pin is selected as the wakeup timer interrupt output pin, the wakeup timer interrupt signal is NORed with the FOUT signal before being output from the FOUT pin. Therefore, when using the FOUT pin only for the wakeup timer interrupt signal output, set the TCTL.FSEL[1:0] bits to 0b11 to disable the FOUT output.

Bit 0: UPDOWNMOD

This bit sets the wakeup timer count mode.

1 (R/W): Count-up mode
0 (R/W): Count-down mode

*1 For more information on the wakeup timer function, refer to "*3.7 Wakeup Timer Function*."

0x39: WTCTL (Wakeup Timer Control)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTRST**	**EXWTRSTEN**	**WTRSTWIN[1:0]**		**WTMODSEL**	**WTSTOPCTL**	**–**	**WTSTOP**
Initial value	0	0	0	0	0	0	0	0
R/W	W	R/W	R/W		R/W	R/W	R	R/W

Bit 7: WTRST

This bit reloads the preset value to the wakeup timer.

1 (W): Timer is preset.
0 (W): Ineffective

Writing 1 to this bit reloads the preset value to the wakeup timer counter in Count-down mode or reloads 1 in Count-up mode, and then restarts the count operation. This makes it possible to use the wakeup timer as a watchdog timer.
This bit is always read as 0 even after writing 1.

Bit 6: EXWTRSTEN

This bit enables/disables resetting the wakeup timer by an external input signal.

1 (W): External input reset is enabled.
0 (W): External input reset is disabled.

When the EXWTRSTEN bit is set to 1, the wakeup timer is reset by inputting a high pulse having a 977 µs or more width to the EVIN2 pin. This external input reset can be used in combination with the WTRST bit reset.

Bits 5–4: WTRSTWIN[1:0]

These bits specify the reset acceptance period (reset window) for the wakeup timer set into Count-down mode. This limitation of reset acceptance period is applied to both resets by the WTRST bit and external signal input.

Table 4.11 Reset Window Settings

WTCTL.WTRSTWIN[1:0]	Reset acceptance period (Count-down mode)
0b00	Whole period (default)
0b01	Counter value = 2 to 1
0b10	Counter value = 16 to 1
0b11	Counter value = 64 to 1

The wakeup timer preset value must be larger than the reset acceptance period.

Bit 3: WTMODSEL

This bit restricts the wakeup timer to operate either in Normal mode (reset output is cancelled) or Safe mode (during reset output).

1 (R/W): The counter stops in Normal mode.
0 (R/W): The counter stops in Safe mode.

Bit 2: WTSTOPCTL

This bit enables/disables the WTMODSEL and WTSTOP bit functions.

1 (R/W): WTMODSEL is enabled and WTSTOP is disabled.
0 (R/W): WTMODSEL is disabled and WTSTOP is enabled.

Bit 0: WTSTOP

This bit temporarily stops the wakeup timer.

1 (R/W): The wakeup timer is temporarily stopped.
0 (R/W): The wakeup timer temporary stop state is cancelled (the wakeup timer is operating normally).

*1 For more information on the wakeup timer function, refer to "*3.7 Wakeup Timer Function*."

0x3A: WTCNT_L_MIR (Mirrored Wakeup Timer Counter Low, = 0x0A)
0x3B: WTCNT_M_MIR (Mirrored Wakeup Timer Counter Middle, = 0x0B)
0x3C: WTCNT_H_MIR (Mirrored Wakeup Timer Counter High, = 0x0C)

Mirrored Wakeup Timer Counter Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[7:0]							
Initial value	0	0	0	0	0	0	0	1
R/W	R/W							

Mirrored Wakeup Timer Counter Middle

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[15:8]							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Mirrored Wakeup Timer Counter High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[23:16]							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

These are mirror registers of Registers WTCNT_L, WTCNT_M, and WTCNT_H. For more information, refer to "*0x0A–0x0C: WTCNT_L/WTCNT_M/WTCNT_H (Wakeup Timer Counter Low/Middle/High)*."

0x3D: TCTL_MIR (Mirrored Timer Control, = 0x0D)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FSEL[1:0]**		**USEL0**	**TE**	**WADA**	**–**	**TSEL[1:0]**	
Initial value	0	0	0	0	0	0	1	0
R/W	R/W		R/W	R/W	R/W	R	R/W	

This is a mirror register of Register TCTL. For more information, refer to "*0x0D: TCTL (Timer Control)*."

0x3E: INTF_MIR (Mirrored Status Flag, = 0x0E)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PORF**	**OSCSTPF**	**UF**	**TF**	**AF**	**EVF**	**VLF**	**VTMPLF**
Initial value	1	1	x	x	x	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a mirror register of Register INTF. For more information, refer to "*0x0E: INTF (Status Flag)*."

0x3F: TSTP_INTE_MIR (Mirrored Timer Stop and Interrupt Enable, = 0x0F)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**CSEL[1:0]**		**UIE**	**TIE**	**AIE**	**EIE**	**–**	**STOP**
Initial value	0	1	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R	R/W

This is a mirror register of Register TSTP_INTE. For more information, refer to "*0x0F: TSTP_INTE (Timer Stop and Interrupt Enable)*."

0x41: WRCMD_CFG (Write Command Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**EVCNTCLREN**	–	–	**BUF1FCLREN**	**–**	**–**	**–**	**CMDTRGEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R/W	R	R	R	R/W

Note: This register specifies the functions that will be executed when any data is written to Register WRCMD_TRG (Address 0x42).

Bit 7: EVCNTCLREN

This bit specifies whether to initialize the event counters or not when a command trigger is executed by writing to Register WRCMD_TRG.

1 (R/W): Event counter is initialized.
0 (R/W): Event counter is not initialized.

Executing a command trigger with this bit set to 1 initializes the EVIN1 and 2 event input counters shown below to clear to 0.

EVIN1_EVCNT.EVCNT[5:0] bits (EVIN1 event counter)
EVIN2_EVCNT.EVCNT[5:0] bits (EVIN2 event counter)

Bit 4: BUF1FCLREN

This bit specifies whether to initialize the buffer status flags when a command trigger is executed.

1 (R/W): Buffer status flag is initialized.
0 (R/W): Buffer status flag is not initialized.

Executing a command trigger with this bit set to 1 initializes the buffer status flags shown below to set the buffer into empty status.

BUF1_STAT.FULLF bit (Buffer full flag)
BUF1_STAT.EMPTF bit (Buffer empty flag)
BUF1_STAT.OVWF bit (Buffer overwrite flag)

Bit 0: CMDTRGEN

This bit specifies whether to issue a time stamp trigger when a command trigger is executed.

1 (R/W): Time stamp trigger is issued.
0 (R/W): Time stamp trigger is not issued.

Executing a command trigger with this bit set to 1 issues a time stamp trigger. To issue this time stamp trigger successively, a 5 ms or more interval must be inserted between the triggers. Check if the BUF_INTF.BUF1F bit is set to 1 to confirm that the time stamp trigger is accepted.

0x42: WRCMD_TRG (Write Command Trigger)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WRTRG[7:0]**							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Bits 7–0: WRTRG[7:0]

By writing any value to this address, a command trigger is issued to execute the command configured in Register WRCMD_CFG (Address 0x41) (the command is issued at the register write timing. For more information on the timing, refer to "*Issuing Command Trigger*" in Section 3.11).

After a command trigger has been issued, this register retains a value other than 0x00 until the subsequent command trigger can be issued or the captured time stamp data can be read. Make sure this register has reverted to 0x00 by reading if the time stamp data is read or a subsequent command trigger is issued immediately after a time stamp trigger is issued.

0x43: EVNT_INTE (Event Interrupt Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**–**	**EVIN2IEN**	**EVIN1IEN**	**RSTOIEN**	–	**VTMPLIEN**	–	**OSCSTPIEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R/W	R	R/W

Bit 6: EVIN2IEN
Bit 5: EVIN1IEN

These bits enable/disable the EVIN*n* event input to generate interrupts.

1 (R/W): EVIN*n* event input interrupts are enabled.
0 (R/W): EVIN*n* event input interrupts are disabled.

Bit 4: RSTOIEN

This bit enables/disables the reset output function (to detect if the V_{DD} voltage drops below the V_{DD} drop detection voltage) to issue event triggers. This bit is effective only in the models with the /RST pin.

1 (R/W): Reset output event trigger is enabled.
0 (R/W): Reset output event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.RSTOEVF bit) is set to 1 when a reset output is started (V_{DD} voltage drop below the V_{DD} drop detection voltage ($-V_{DET1n}$) is detected).

Bit 2: VTMPLIEN

This bit enables/disables the V_{DET2} voltage drop detection function (to detect if the V_{DD} voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) to issue event triggers.

1 (R/W): V_{DET2} voltage drop detection event trigger is enabled
0 (R/W): V_{DET2} voltage drop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.VTMPLEVF bit) is set to 1 when a V_{DET2} voltage drop is detected.

Bit 0: OSCSTPIEN

This bit enables/disables the oscillation stop detection function to issue event triggers.

1 (R/W): Oscillation stop detection event trigger is enabled.
0 (R/W): Oscillation stop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.OSCSTPEVF bit) is set to 1 when an oscillation stoppage is detected.

0x44: CAP_EN (Capture Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	**RSTOCPEN**	–	**VTMPLCPEN**	–	**OSCSTPCPEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R/W	R	R/W

Bit 4: RSTOCPEN

This bit enables/disables the reset output (to detect if the V_{DD} voltage drops below the V_{DD} drop detection voltage) event trigger to capture time stamp data.

1 (R/W): Reset output time stamp capturing is enabled.
0 (R/W): Reset output time stamp capturing is disabled.

Bit 2: VTMPLCPEN

This bit enables/disables the V_{DET2} voltage drop detection (to detect if the V_{DD} voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) event trigger to capture time stamp data.

1 (R/W): V_{DET2} voltage drop detection time stamp capturing is enabled.
0 (R/W): V_{DET2} voltage drop detection time stamp capturing is disabled.

Bit 0: OSCSTPCPEN

This bit enables/disables the oscillation stop detection event trigger to capture time stamp data.

1 (R/W): Oscillation stop detection time stamp capturing is enabled.
0 (R/W): Oscillation stop detection time stamp capturing is disabled.

Note: To actually execute time stamp capturing by each event trigger, it is necessary to set the ***IEN bit in Register EVNT_INTE corresponding to the event enabling the event flag (***EVF bit) in Register EVNT_INTF to be set.

0x45: INTF_MIR (Mirrored Status Flag, = 0x0E)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PORF**	**OSCSTPF**	**UF**	**TF**	**AF**	**EVF**	**VLF**	**VTMPLF**
Initial value	1	1	x	x	x	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

This is a mirror register of Register INTF. For more information, refer to "*0x0E: INTF (Status Flag)*."

0x46: BUF_INTF (Buffer Interrupt Factor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	**BUF1F**	**RSTOF**	–	–	–	–
Initial value	0	0	0	1	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R

Bit 5: BUF1F

These flags indicate that a time stamp buffer event trigger input interrupt factor has occurred.

1 (R): An event trigger input has occurred.
0 (R): No event trigger input has occurred.

This flag is set to 1 when a buffer full (BUF1_STAT.FULLF bit = 1), buffer not empty (BUF1_STAT.EMPTF bit = 0), or buffer overwrite (BUF1_STAT.OVWF bit = 1) has occurred.

The BUF1F bit is cleared to 0 when a command trigger for resetting these flags (BUF1_STAT.FULLF bit = 0, BUF1_STAT.EMPTF bit = 1, BUF1_STAT.OVWF bit = 0) is issued.
This flag must be cleared to accept the subsequent event and to output an interrupt.

Bit 4: RSTOF

This flag is set when a reset output has started (V_{DD} voltage drop below the V_{DD} drop detection voltage is detected).

1 (R): Reset output has started. (V_{DD} voltage drop below -V_{DET1n} has been detected.)
0 (R): Reset output has not started. (No V_{DD} voltage drop has been detected.)
1 (W): Ineffective
0 (W): Flag clear (Takes effect after the V_{DD} voltage is restored.)

If a V_{DD} voltage drop status is being continued, this flag cannot be cleared by writing 0.
This flag must be cleared to accept the subsequent event and to output an interrupt.

0x47: EVNT_INTF (Event Interrupt Factor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	**EVIN2F**	**EVIN1F**	**RSTOEVF**	**–**	**VTMPLEVF**	**–**	**OSCSTPEVF**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R/W	R	R/W

Bit 6: EVIN2F
Bit 5: EVIN1F

These flags indicate that an event input has occurred to EVIN*n*.

1 (R): An EVIN*n* event input has occurred.
0 (R): No EVIN*n* event input has occurred.
1 (W): Ineffective
0 (W): Flag clear

Bit 4: RSTOEVF

This flag indicates that a reset output event (the V_{DD} voltage drops below the V_{DD} drop detection voltage) has occurred.

1 (R): Reset output event has occurred.
0 (R): No reset output event has occurred.
1 (W): Ineffective
0 (W): Flag clear

Bit 2: VTMPLEVF

This flag indicates that a V_{DET2} voltage drop detection event (the V_{DD} voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) has occurred.

1 (R): A V_{DET2} voltage drop detection event has occurred.
0 (R): No V_{DET2} voltage drop detection event has occurred.
1 (W): Ineffective
0 (W): Flag clear

Bit 0: OSCSTPEVF

This flag indicates that an oscillation stop detection event has occurred.

1 (R): An oscillation stop detection event has occurred.
0 (R): No oscillation stop detection event has occurred.
1 (W): Ineffective
0 (W): Flag clear

When an oscillation stop detection event has occurred, time stamp data will be captured after the oscillation restarts.

Note: The flags in this register are not set even if an event has occurred when the corresponding ****IEN bit in Register EVNT_INTE has been set to 0.

0x51: EVIN1_EVCNT (EVIN1 Event Counter)
0x52: EVIN2_EVCNT (EVIN2 Event Counter)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	EVCNT[5:0]					
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R					

Bits 5–0: EVCNT[5:0]

These bits indicate the event count (0 to 63 times) input to the EVIN*n* pin.

If the input count exceeds 63 times, the counter reverts to 0 and continues counting. The EVIN*n* event counter does not operate when the EVIN_EN.EVIN*n*EN bit = 0.

0x54: EVINMON (EVIN Monitor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	EVIN2MON	EVIN1MON	–	–	–	–	–
Initial value	0	x	x	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit 6: EVIN2MON
Bit 5: EVIN1MON

These bits indicate the current input level on the EVIN*n* pin.

1 (R): High level
0 (R): Low level

0x55: SOUTCTL (SOUT Control)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	DCE	DC	–	–	SIGINV	SOUT[2:0]		
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R/W	R/W		

Bit 7: DCE

This bit enables/disables DC output from the SOUT pin.

1 (R/W): DC output is enabled.
0 (R/W): DC output is disabled (status flag output or Hi-Z state)

Bit 6: DC

This bit sets the DC level output from the SOUT pin when the DCE bit = 1.

1 (R/W): High level
0 (R/W): Low level

The two-bit combination of DCE and DC allows selection of an SOUT output status as shown in the table below.

Table 4.12 SOUT Output Selections

SOUTCTL.DCE	SOUTCTL.DC	SOUT pin output status
0b0	0b0	Hi-Z
0b0	0b1	According to SIGINV and SOUT[2:0] bit settings
0b1	0b0	Low output
0b1	0b1	High output

Bit 3: SIGINV

This bit selects whether the output level is inverted or not when a status flag is output from the SOUT pin.

1 (R/W): Inverted output (When the flag = 1: Low level output; when the flag = 0: High level output)
0 (R/W): Non-inverted output (When the flag = 1: High level output; when the flag = 0: Low level output)

The invert setting with this bit is ineffective when the DCE bit = 1.

Bits 2–0: SOUT[2:0]

These bits select the status flag to be output from the SOUT pin. This selection is effective only when the DCE bit = 0.

Table 4.13 SOUT Outputtable Internal Status Flags

SOUTCTL.SOUT[2:0]	Status flag
0b000	INTF.TF bit (Wakeup timer interrupt flag)
0b001	INTF.AF bit (Alarm interrupt flag)
0b010	INFF.UF bit (Time update interrupt flag)
0b011	INTF.EF bit (Event detection interrupt flag)
0b100	INTF.VTMPLF bit (Temperature compensation operation stop detection flag)
0b101	INTF.VLF bit (Invalid date and time data warning flag)
0b110–0b111	Reserved

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}	–	-0.3 to +6.5	V
Input voltage	V_{IN}	FOE, CE, SCL, CLK, SDA, DIO, DI, EVIN1, EVIN2	-0.3 to +6.5	V
Output voltage	V_{OUT}	/INT, /RST, SDA, FOUT, SOUT, DIO, DO	-0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	-55 to +125	°C

(Notes) • All the voltages are based on GND = 0 V.
- Operating or placing the device under the condition exceeding the above absolute maximum ratings may cause permanent damage to the device. In normal operation, the device is desired to be used within the recommended operating condition ranges, otherwise, it may cause a malfunction or may adversely affect reliability.
- Voltages must always satisfy the condition of $V_{DD} \geq V_{SS}$.
- Device operations are guaranteed within the ranges of the electrical characteristics.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage *1	V_{DD}	Main power supply V_{DD} pin	1.6	3.0	5.5	V
Interface power voltage	V_{ACC}	V_{DD} pin voltage (I^2C-Bus IF, SPI IF 3-wire/4-wire)	1.6	3.0	5.5	V
Temperature compensation voltage	V_{TMP}	V_{DD} power voltage that can keep temperature compensation operation	1.6 *2	3.0	5.5	V
Time keeping voltage	V_{CLK}	V_{DD} power voltage that can keep clocking operation	V_{VLF} *3	3.0	5.5	V
Operating temperature	Ta	No condensation	-40	+25	+125	°C

*1 A bypass capacitor for noise suppression must be connected as close to the power supply pin as possible.

*2 When the V_{DD} power supply voltage is less than the Min. value of the temperature compensation voltage, the temperature-dependent frequency correction value update function is stopped.

*3 V_{VLF} is the minimum time keeping voltage value after a power-on-reset in $V_{DD} \geq V_{ACC}$ (Min.).

5.3 Frequency Characteristics

Table 5.3 Frequency Characteristics

Unless otherwise specified: GND = 0 V, V_{DD} = 3.0 V, Ta = -40 °C to +125 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output frequency	fo	Ta = +25 °C			32.768		kHz
Frequency tolerance	Δf/f	YB	Ta = 0 °C to +50 °C	–	–	±3.8 *1	×10^{-6}
			Ta = -40 °C to +85 °C	–	–	±5.0 *2	
			Ta = +85 °C to +105 °C	–	–	±8.0 *3	
			Ta = +105 °C to +125 °C	–	–	±50.0 *4	
Frequency-voltage characteristics	f/V	Ta = +25 °C, V_{DD} = 1.6 V to 5.5 V		–	–	±1	×10^{-6}/V
FOUT duty	Duty	Vth = 50% V_{DD}, Ta = -40 °C to +125 °C, V_{DD} = 1.6 V to 5.5 V		40	–	60	%
Crystal oscillation start-up time	t_{STA}	Ta = +25 °C, V_{DD} = 1.6 V to 5.5 V		–	0.5	1.0	s
		Ta = -40 °C to +125 °C, V_{DD} = 1.6 V to 5.5 V		–	–	3.0	
Aging	fa	Ta = +25 °C, power supply voltage = 3.0 V, first year		–	–	±3	×10^{-6}/year
Reflow	Δfref	Reflow process: 260°C Max., twice		–		±3 *5	10^{-6}

∗1 Monthly rate: ±10 seconds ∗2 Monthly rate: ±13.2 seconds ∗3 Monthly rate: ±21 seconds ∗ 4 Monthly rate: ±132 seconds

∗5 Frequency change rate before and after being mounted by reflow soldering that was measured under a room temperature environment after being left for 24 hours

5.4 DC Characteristics

DC Characteristics

Table 5.4 DC Characteristics

Unless otherwise specified: GND = 0 V, V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +125 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
V_{POR} voltage	V_{POR}	POR assert voltage		1.00	1.20	1.30	V
Temperature compensation update stop detection voltage	V_{DET2}	Detection power system = V_{DD}		1.51	1.55	1.59	V
VLF detection voltage	V_{VLF}	V_{DD} power supply drop detection voltage		1.00	1.20	1.30	V
Current consumption 1	I_{DD1}	/INT = Hi-Z, FOUT: Output OFF (Hi-Z)	V_{DD} = 5 V	–	0.35	1.8	µA
Current consumption 2	I_{DD2}	Temperature compensation interval: 2.0 s No /RST pin, SCL, SDA = H, CE = L	V_{DD} = 3 V	–	0.30	1.7	
Current consumption 3	I_{DD3}	/INT = Hi-Z FOUT: 32 kHz output, C_L = 0 pF	V_{DD} = 5 V	–	1.20	3.1	µA
Current consumption 4	I_{DD4}	Temperature compensation interval: 2.0 s No /RST pin, SCL, SDA = H, CE = L	V_{DD} = 3 V	–	0.80	3.0	
Current consumption 5	I_{DD5}	/INT= Hi-Z FOUT: 32 kHz output, C_L= 30 pF	V_{DD} = 5 V	–	6.10	8.1	µA
Current consumption 6	I_{DD6}	Temperature compensation interval: 2.0 s No /RST pin, SCL, SDA = H, CE = L	V_{DD} = 3 V	–	4.00	6.0	
Current consumption 7	I_{DD7}	/INT = Hi-Z FOUT: Output OFF (Hi-Z)	V_{DD} = 5 V	–	0.33	1.75	µA
Current consumption 8	I_{DD8}	Temperature compensation circuit: OFF No /RST pin, SCL, SDA = H, CE = L	V_{DD} = 3 V	–	0.28	1.65	
Current consumption 9	I_{DD9}	/INT = Hi-Z FOUT: Output OFF (Hi-Z)	V_{DD} = 5 V	–	60	100	µA
Current consumption 10	I_{DD10}	The temperature compensation operation: peak performance No /RST pin, SCL, SDA = H, CE = L	V_{DD} = 3 V	–	55	95	
Current consumption 11	I_{DD11}	/INT = Hi-Z, FOUT: Output OFF (Hi-Z) Temperature compensation interval: 2.0 s With /RST pin, during output cancelled (Hi-Z) SCL, SDA = H, CE = L	V_{DD} = 5 V	–	1.50	3.7	µA
Current consumption 12	I_{DD12}	/INT = Hi-Z, FOUT: Output OFF (Hi-Z) Temperature compensation interval: 2.0 s With /RST pin, during output (Low) SCL, SDA = H, CE = L	V_{DD} = 2 V	–	0.60	2.25	
Current consumption 13	I_{DD13}	/INT = Hi-Z, FOUT: Output OFF (Hi-Z) Temperature compensation interval: 2.0 s	V_{DD} = 5 V	–	12	20	µA
Current consumption 14	I_{DD14}	With /RST pin, V_{DD} voltage detection operation: peak performance SCL, SDA = H, CE = L	V_{DD} = 3 V	–	11	19	
"H" input voltage	V_{IH}	SCL, SDA, CE, CLK, DIO, DI, EVIN*n*, FOE		0.8 x V_{DD}	–	5.5	V
"L" input voltage	V_{IL}	SCL, SDA, CE, CLK, DIO, DI, EVIN*n*, FOE		GND - 0.3	–	0.2 x V_{DD}	V
"H" output voltage	V_{OH1}	DIO, DO, FOUT, SOUT	V_{DD} = 5.0 V, I_{OH} = -1 mA	4.5	–	5.0	V
	V_{OH2}		V_{DD} = 3.0 V, I_{OH} = -1 mA	2.2	–	3.0	
	V_{OH3}		V_{DD} = 3.0 V, I_{OH} = -100 µA	2.9	–	3.0	
"L" output voltage	V_{OL1}	FOUT, SOUT	V_{DD} = 5.0 V, I_{OL} = 1 mA	GND	–	GND + 0.5	V
	V_{OL2}		V_{DD} = 3.0 V, I_{OL} = 1 mA	GND	–	GND + 0.8	
	V_{OL3}		V_{DD} = 3.0 V, I_{OL} = 100 µA	GND	–	GND + 0.1	
	V_{OL4}	DIO, DO, /INT, /RST	V_{DD} = 5.0 V, I_{OL} = 1 mA	GND	–	GND + 0.25	V
	V_{OL5}		V_{DD} = 3.0 V, I_{OL} = 1 mA	GND	–	GND + 0.4	
	V_{OL6}	SDA	$V_{DD} \geq$ 2.0 V, I_{OL} = 3 mA	GND	–	GND + 0.4	V
Input leakage current	I_{LK}	Input pin, input voltage = V_{DD} or GND		-0.5	–	0.5	µA
Output leakage current	I_{OZ}	Output pin, output voltage = V_{DD} or GND		-0.5	–	0.5	µA
Open drain output pin pull-up voltage	V_{PUP1}	/INT		–	–	5.5	V
	V_{PUP2}	/RST, SDA		V_{DD}	–	5.5	V
EVIN*n* input pull-up resistance	R_{UP1}	EVIN1/EVIN2 pin, V_{DD} = 3 V, 500 kΩ setting		100	500	2000	kΩ
	R_{UP2}	EVIN1/EVIN2 pin, V_{DD} = 3 V, 1 MΩ setting		0.20	1.00	4.00	MΩ
	R_{UP3}	EVIN1/EVIN2 pin, V_{DD} = 3 V, 10 MΩ setting		2.00	10.00	40.00	MΩ
EVIN*n* input pull-down resistance	R_{DWN3}	EVIN1/EVIN2 pin, V_{DD} = 3 V, 500 kΩ setting		100	500	2000	kΩ
Pull-down resistance of CE input and Option C N.C. pins (Pin 1, 5, 6)	R_{DWN1}	CE pin, N.C. pins (Option C), V_{DD} = 5 V		75	150	300	kΩ
	R_{DWN2}	CE pin, N.C. pins (Option C), V_{DD} = 3 V		150	300	600	kΩ

Temperature Compensation Operation and Current Consumption

This model updates the temperature compensation value by measuring the temperature sensor in temperature compensation intervals, therefore, current consumption increases during this operation period. I_{DD1} or I_{DD2} is the average current consumption when the temperature sensor measurement interval is set to 2.0 seconds.

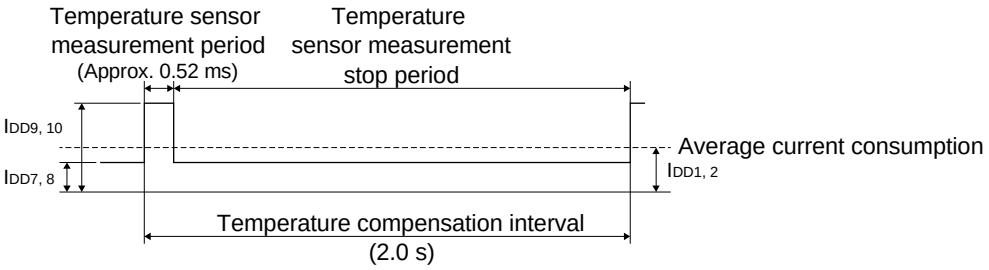


Figure 5.1 Temperature Compensation Operation and Current Consumption

Current Consumption of Model with /RST Output Pin

In the model with the /RST output pin, current consumption of the V_{DD} voltage detection circuit varies periodically as shown in Figure 5.2. I_{DD11} or I_{DD12} is the average current consumption.

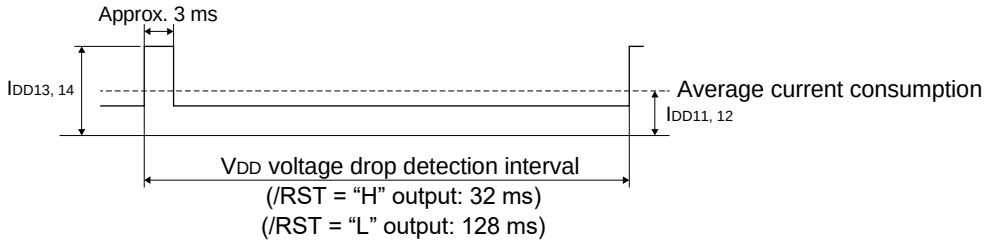


Figure 5.2 Current Consumption of Model with /RST Output Pin

Detection Voltages for State Transition and Self-Monitoring Functions

Figure 5.3 shows the voltages to decide if the RA4000CE/RA8000CE operating state/mode (*Section 2.3*) will transit and if the flags for reset output function (*Section 3.9*) and self-monitoring function (*Section 3.10*) will be set.

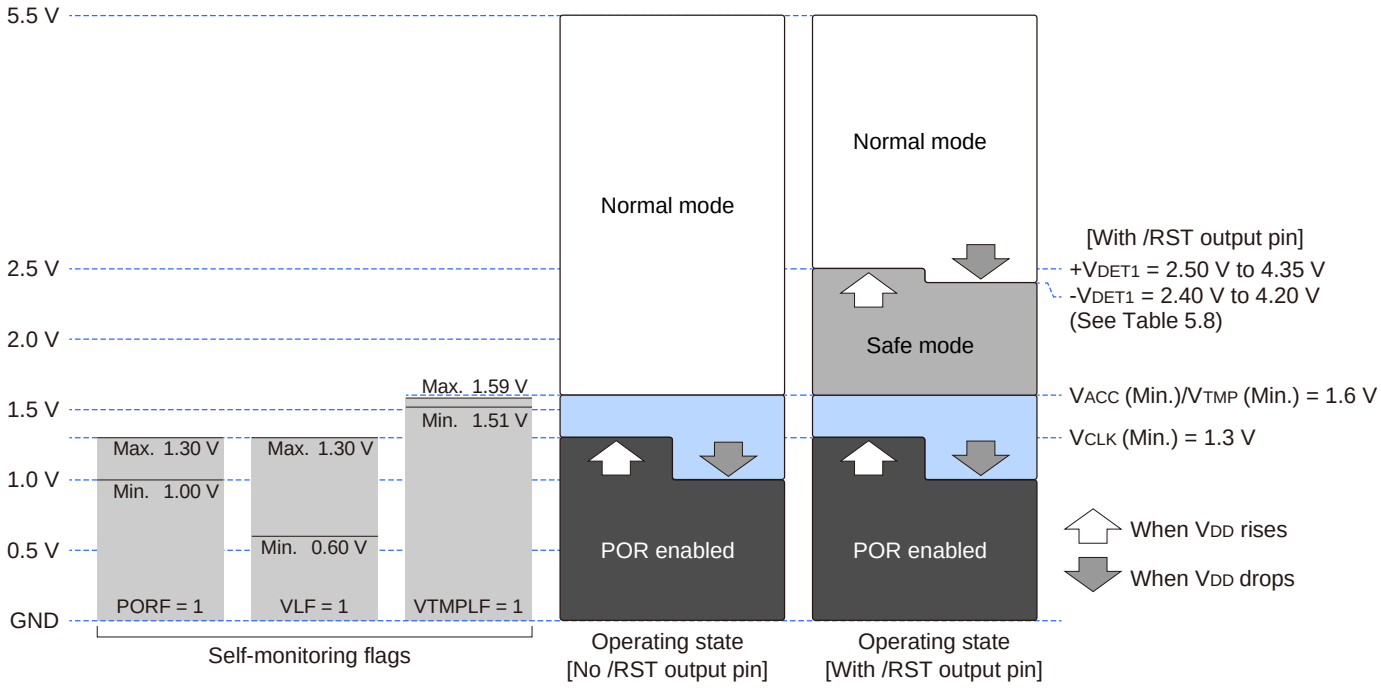


Figure 5.3 Correlation Diagram between Voltages and Operating States/Self-Monitoring Flags

5.5 AC Characteristics

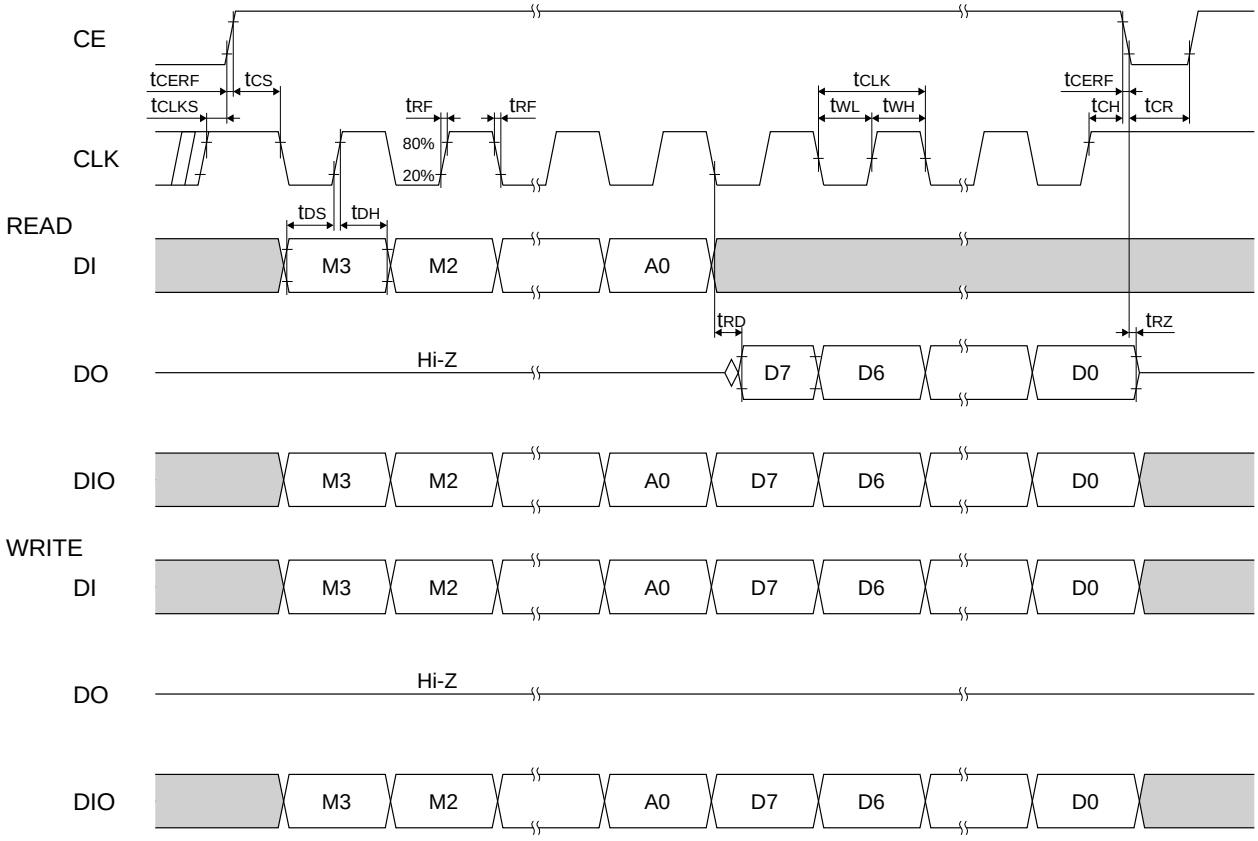
RA4000CE AC Characteristics

Table 5.5 RA4000CE AC Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +125 °C

Item	Symbol	Condition	V_{DD} = 1.8 V ± 0.2 V		V_{DD} = 3.0 V ± 10 %		V_{DD} = 5.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500	–	332	–	250	–	ns
CLK “H” pulse width	t_{WH}		250	–	166	–	125	–	ns
CLK “L” pulse width	t_{WL}		250	–	166	–	125	–	ns
CLK rise/ fall time	t_{RF}		–	100	–	50	–	40	ns
CLK setup time	t_{CLKS}		50	–	30	–	30	–	ns
CE setup time	t_{CS}		200	–	150	–	130	–	ns
CE hold time	t_{CH}		200	–	150	–	130	–	ns
CE recovery time	t_{CR}		300	–	200	–	150	–	ns
CE rise/ fall time	t_{CERF}		–	100	–	50	–	40	ns
Write data setup time	t_{DS}		100	–	50	–	40	–	ns
Write data hold time	t_{DH}		100	–	50	–	40	–	ns
Read data delay time	t_{RD}	C_L = 50 pF	–	200	–	150	–	150	ns
DO (DIO) output disable time	t_{RZ}	C_L = 50 pF, R_L = 10 kΩ	–	200	–	120	–	110	ns

∗1 When V_{DD} = 2.0 V to 2.7 V, the V_{DD} = 1.8 V ± 0.2 V specifications should be applied. When V_{DD} = 3.3 V to 4.5 V, the V_{DD} = 3.0 V ± 10% specifications should be applied.



∗ Do not place the CLK and DI or DIO pins into a floating state during Normal mode.

Figure 5.4 RA4000CE AC Characteristics (SPI Timing Chart)

RA8000CE AC Characteristics

Table 5.6 RA8000CE AC Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +125 °C

Item	Symbol	100 kHz access (Standard mode)		400 kHz access (Fast mode)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	–	100	–	400	kHz
START condition setup time	$t_{SU;STA}$	4.7	–	0.6	–	µs
START condition hold time	$t_{HD;STA}$	4.0	–	0.6	–	µs
Data setup time	$t_{SU;DAT}$	250	–	100	–	ns
Data hold time	$t_{HD;DAT}$	0	–	0	–	ns
STOP condition setup time	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between STOP and START conditions	t_{BUF}	4.7	–	1.3	–	µs
SCL “L” width	t_{LOW}	4.7	–	1.3	–	µs
SCL “H” width	t_{HIGH}	4.0	–	0.6	–	µs
SCL, SDA rise time	tr	–	1.0	–	0.3	µs
SCL, SDA fall time	tf	–	0.3	–	0.3	µs
Allowable spike time on bus	t_{SP}	–	50	–	50	ns

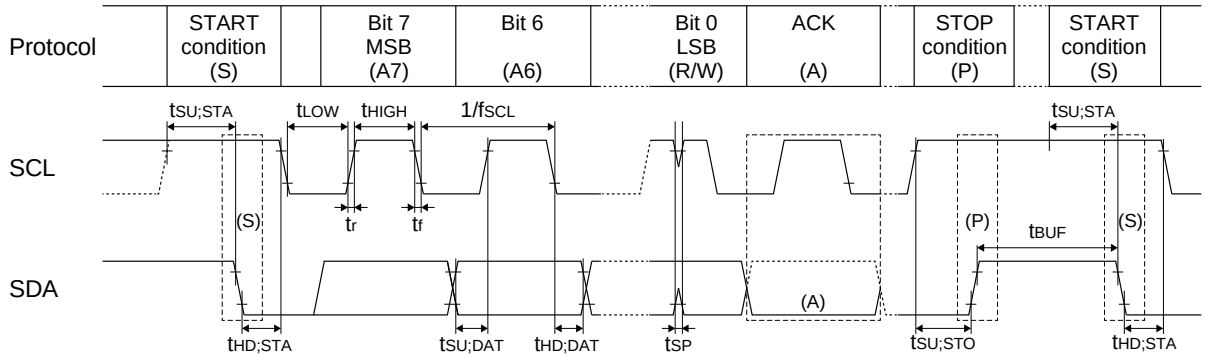


Figure 5.5 RA8000CE AC Characteristics (I^2C-Bus Timing Chart)

∗1 The I^2C-Bus interface of the RA8000CE is reset and SDA is set into Hi-Z in two counts of the internal 1 Hz clock after the slave address is received. Therefore, an I^2C-Bus communication from sending the slave address to generating STOP condition must be completed in one second.

∗2 The RA8000CE loads the 8-bit write data sent from the host at the SCL rising edge while responding with an ACK after all the 8 bits have been received. If the communication is disconnected before loading 8-bit data, the data, which has unreceived bits, is not written to the RA4000CE/RA8000CE register.

5.6 Power-On Characteristics

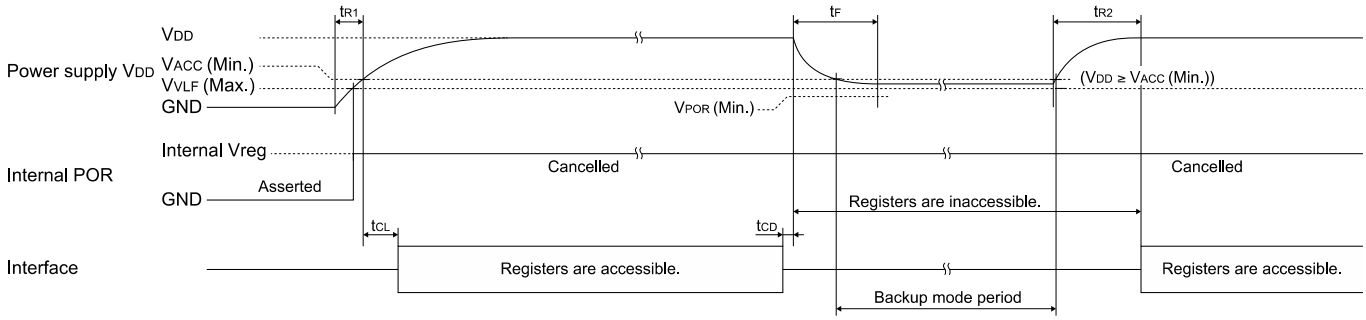
Table 5.7 Power-On Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +125 °C

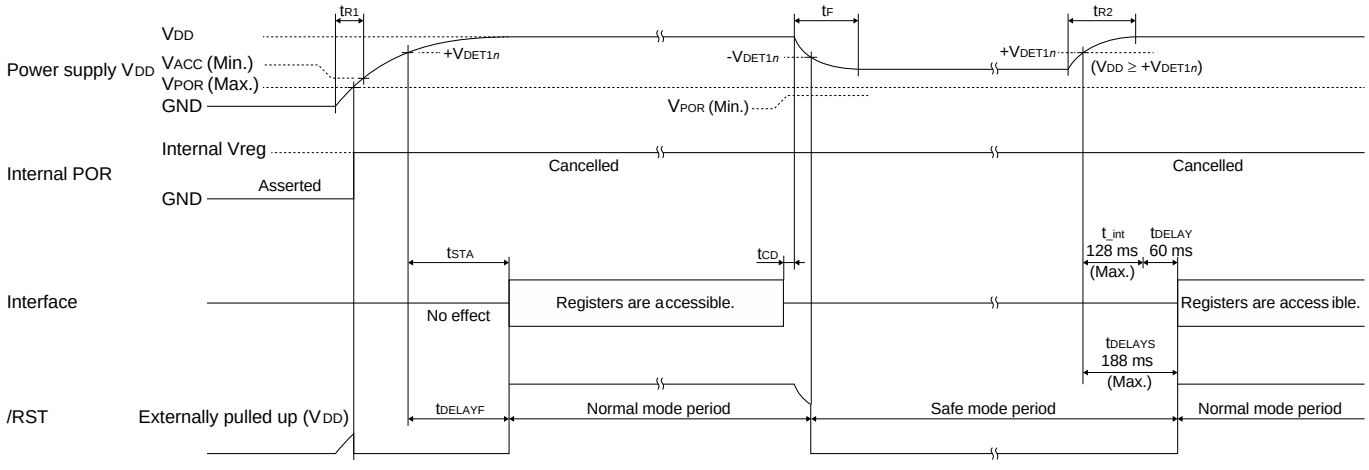
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time 1 *1	t_{R1}	Voltage slope (voltage variation rate) while the V_{DD} voltage is rising from GND after power on (between GND and V_{ACC} (Min.))	1	–	10	ms/V
Access waiting time after power on *2	t_{CL}	Time after V_{DD} reaches V_{ACC} (Min.) until accessing can be started	40	–	–	ms
Access end hold time before power off	t_{CD}	The waiting time until the V_{DD} voltage starts dropping in the t_F voltage slope after the end of access	0	–	–	µs
Power supply fall time	t_F	Voltage slope (voltage variation rate) while the V_{DD} voltage is dropping	1	–	–	ms/V
Power supply rise time 2	t_{R2}	Voltage slope (voltage variation rate) while the power supply voltage is rerising	1	–	–	ms/V

∗1 To execute power-on reset with certainly at the initial power on, the power supply rise time condition must be satisfied and the power voltage must be supplied from the GND level. To ensure that power-on reset takes effect, maintain the V_{DD} is GND level condition for at least 100ms after power-off.

∗2 This characteristic is applied to the models without the /RST output function. Before all the registers can be accessed, it is necessary that the crystal oscillation has started and the internal clock has been supplied. After t_{CL} has elapsed, the VLF bit becomes accessible. The registers are enabled to be configured when the VLF flag is cleared after writing 0 to the VLF bit. In the models with the /RST output function, the registers become accessible after t_{STA} has elapsed and the /RST pin has output an H level.



(1) In the case of a model without the /RST output function



(2) In the case of a model with the /RST output function

Figure 5.6 Power-On Sequence

5.7 Reset Output Characteristics

Table 5.8 Reset Output Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +125 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{DD} rise detection voltage 1 *1	$+V_{DET11}$		4.25	4.35	4.45	V
V_{DD} drop detection voltage 1 *2	$-V_{DET11}$		4.12	4.20	4.28	V
V_{DD} rise detection voltage 2 *1	$+V_{DET12}$		4.15	4.25	4.35	V
V_{DD} drop detection voltage 2 *2	$-V_{DET12}$		4.02	4.10	4.18	V
V_{DD} rise detection voltage 3 *1	$+V_{DET13}$		4.05	4.15	4.25	V
V_{DD} drop detection voltage 3 *2	$-V_{DET13}$		3.92	4.00	4.08	V
V_{DD} rise detection voltage 4 *1	$+V_{DET14}$		3.95	4.05	4.15	V
V_{DD} drop detection voltage 4 *2	$-V_{DET14}$		3.82	3.90	3.98	V
V_{DD} rise detection voltage 5 *1	$+V_{DET15}$		2.75	2.85	2.95	V
V_{DD} drop detection voltage 5 *2	$-V_{DET15}$		2.67	2.75	2.83	V
V_{DD} rise detection voltage 6 *1	$+V_{DET16}$		2.70	2.80	2.90	V
V_{DD} drop detection voltage 6 *2	$-V_{DET16}$		2.62	2.70	2.78	V
V_{DD} rise detection voltage 7 *1	$+V_{DET17}$		2.45	2.55	2.65	V
V_{DD} drop detection voltage 7 *2	$-V_{DET17}$		2.37	2.45	2.53	V
V_{DD} rise detection voltage 8 *1	$+V_{DET18}$		2.40	2.50	2.60	V
V_{DD} drop detection voltage 8 *2	$-V_{DET18}$		2.32	2.40	2.48	V
/RST output internal delay time *3	t_{DELAY}		–	60	–	ms
/RST output delay time (at initial power-on) *3	t_{DELAYF}		560	t_{STA}	–	ms
/RST output cancellation voltage detection time (when Safe mode is cancelled) *3	$t_{\_int}$	Depends on the V_{DD} voltage detection intermittent operation (128 ms intervals) timing during Safe mode	0	–	128	ms
/RST output delay time (when Safe mode is cancelled) *3	t_{DELAYS}	Output delay time when restoring from Safe mode after initial power-on to Normal mode	–	188 $t_{\_int}$ + t_{DELAY}	–	ms

*1 Reset output (Safe mode) cancellation voltage

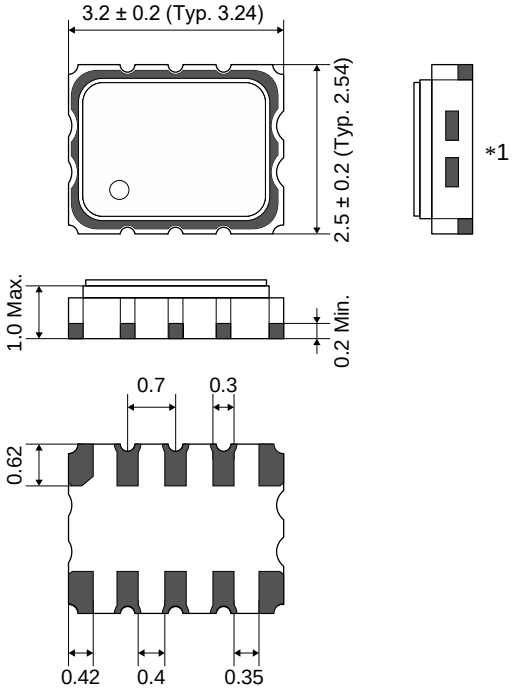
*2 Reset output (Safe mode) start voltage

*3 See (2) in Figure 5.6 for corresponding between the timing parameters and the /RST output signal.

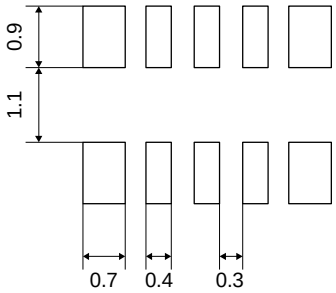
6 Package

6.1 Package Dimensions

• External dimensions



• Recommended soldering pattern

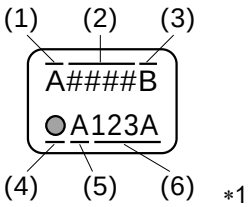


Unit: mm

*1 The metal pads on the short side of the 1st and 10th pins of the package are inspection pads for the crystal unit.
For stable oscillation, make sure that leakage current due to condensation or dust does not occur between these pads.
The metal pads on the short side of the 5-pin and 6-pin sides are not connected inside the RTC.

Figure 6.1 Package Dimensions

6.2 Marking Layout



(1) Logo A → RA
(2) Type 4000 → RA4000CE
8000 → RA8000CE
(3) Frequency tolerance, /RST specification
(4) Pin 1 mark
(5) Product option
(6) Production lot number

*1 Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 6.2 Marking Layout

7 Notes on Mounting

This module includes a crystal oscillator. Do not apply excessive shock and vibration. Further, the module is fabricated with a C-MOS process employed to realize low power consumption. It is necessary to take a measure against static electricity when performing mounting work.

Static Electricity

Although this module includes an electrostatic breakdown protection circuit, the internal circuits may be damaged due to a large discharge of static electricity. Electrically conductive containers should be used for packing and transport. In addition, use a soldering iron and measurement equipment without high voltage leakage, and take a measure against static electricity in mounting and other works.

Noise

If a signal with excessive external noise is applied to the power supply or input pins, the internal circuits may be damaged due to latch up or other malfunctions. In order to ensure stable operation, connect a 0.1 µF or larger ceramic capacitor as close to the power supply pins of this module as possible. Also, avoid placing any device that generates a large noise near this module.

Input Voltage

When a voltage out of the allowable range is constantly applied to an input pin, shoot-through current flows. This causes current consumption to increase or latch up to occur, and the internal circuits may be damaged. Apply a voltage of V_{IL} Max. or lower and V_{IH} Min. or higher to the input pin according to the input voltage specifications.

Handling of Unused Pins

Leaving input pins open causes current consumption to increase and quality deterioration. Fix the input level of unused pins with the internal pull-up and pull-down resistor disabled at either V_{DD} or GND.

Soldering Temperature

If the temperature in the package exceeds +260 °C at soldering, the characteristics of the crystal resonator will be degraded or the internal circuits may be damaged. Check the mounting temperature and time before mounting this device following the solder heat resistance evaluation profile provided by Seiko Epson.

Mounting Equipment

When using general-purpose mounting equipment, check the equipment and its operating conditions, as there is a possibility that the internal crystal resonator will be damaged by a shock at mounting depending on the conditions. If the mounting conditions are later changed, the same check should be performed again. In addition, take a measure against static electricity when performing mounting work.

Ultrasonic Cleaning

Depending on the usage conditions, there is a possibility that the crystal resonator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

Mounting Orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

Leakage between Pins

Current leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Solder Heat Resistance Evaluation Profile (for reference)

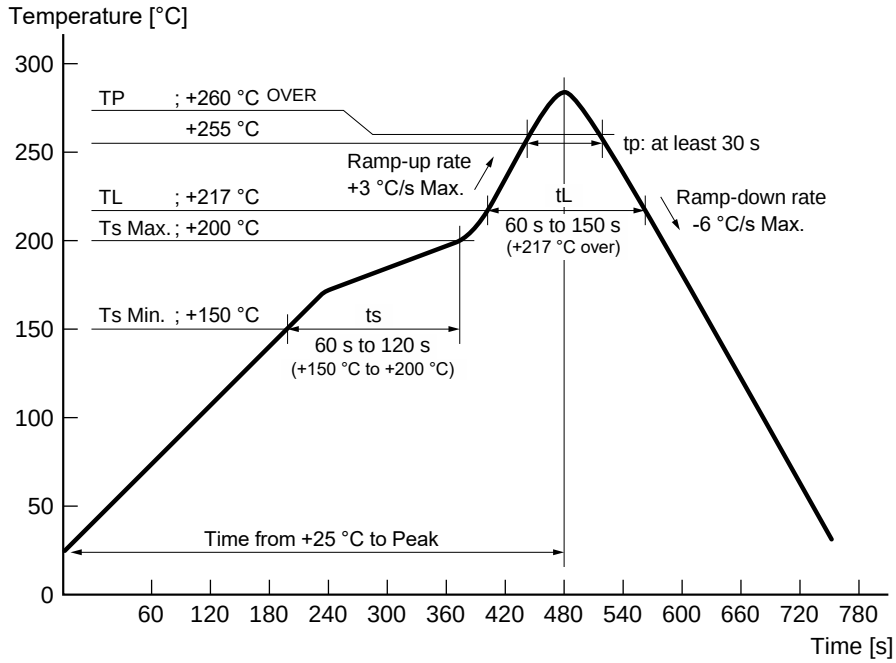


Figure 7.1 Solder Heat Resistance Evaluation Profile (for reference)

8 Moisture Resistance/Electrostatic Breakdown Voltage Characteristics

8.1 Moisture Sensitivity Level (MSL)

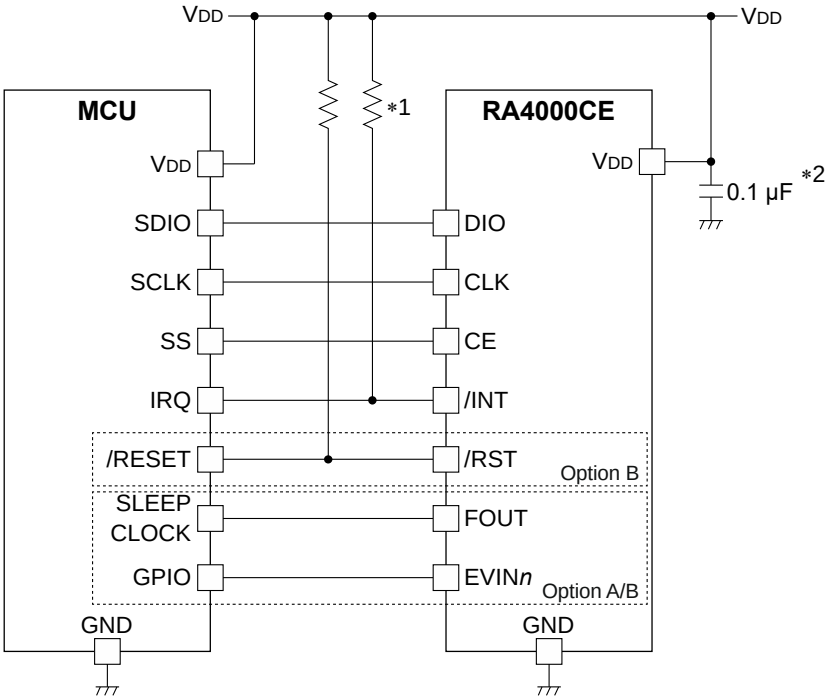
Item	レベル	Condition
MSL	LEVEL1	According to JEDEC J-STD-020D.1

* After unpacking, the products should be stored under an environment with a temperature of +30 °C or lower and humidity of 85 % or less. Also they should be mounted within six months.

8.2 Electrostatic Breakdown Voltage

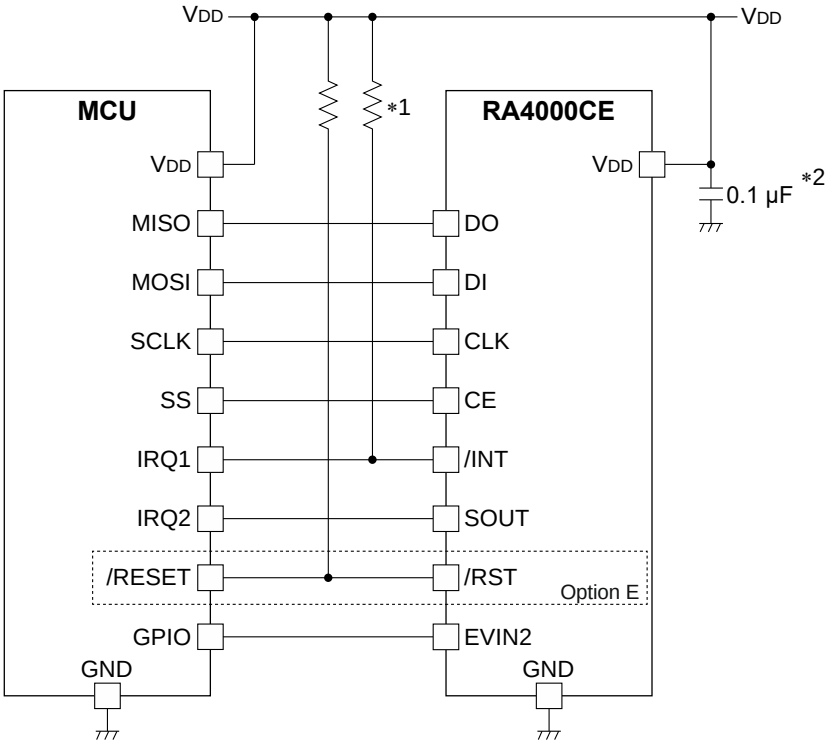
Item	Value	Condition
ESD voltage (HBM)	2000 V (Min.)	According to EIAJ ED-4701-1 C111A
ESD voltage (MM)	2000 V (Min.)	According to EIAJ ED-4701-1 C111

9 Sample Connection Diagram



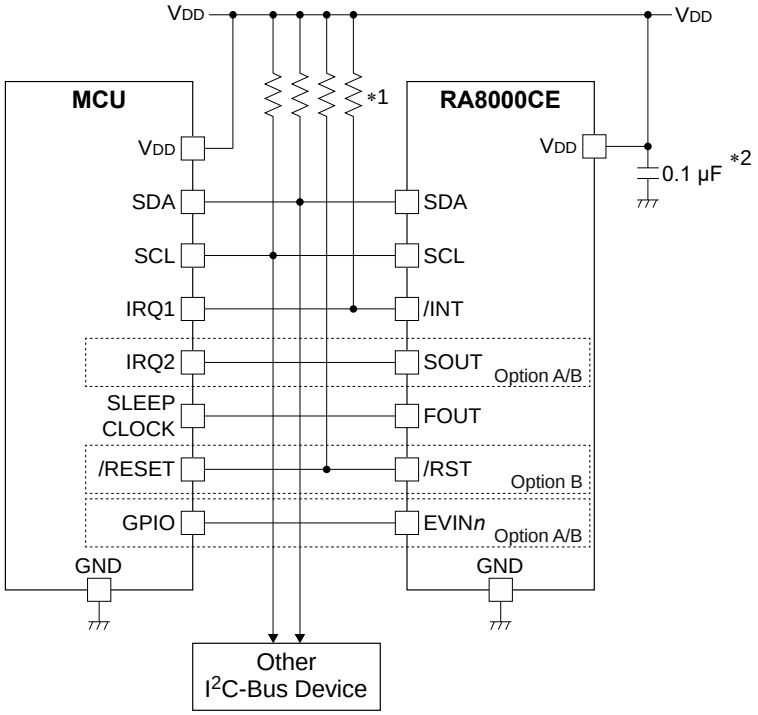
*1 The pull-up resistor value for the /INT pin should be determined considering the output drive capability and output rise time.
*2 The bypass capacitor should be placed as close to the RA4000CE pins as possible.

Figure 9.1 Sample Connection Diagram with a Typical MCU (RA4000CE Option A/B/C)



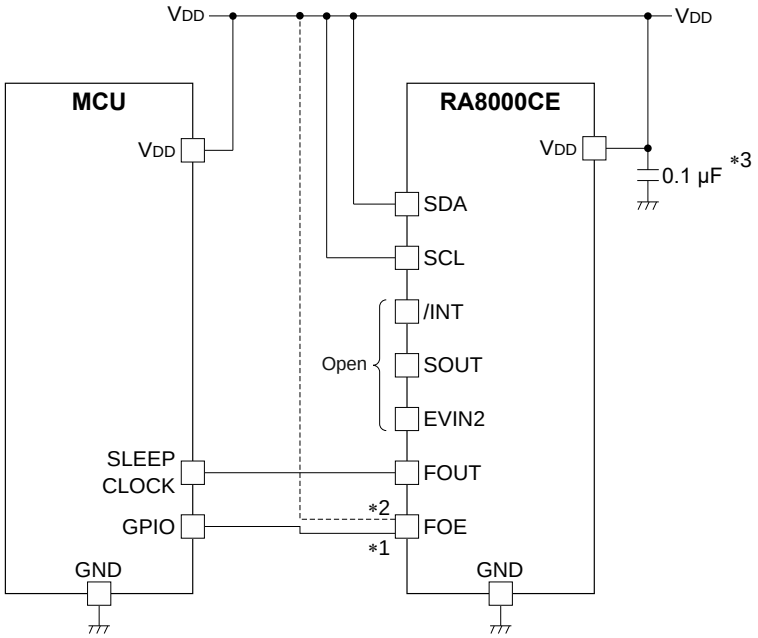
*1 The pull-up resistor value for the /INT pin should be determined considering the output drive capability and output rise time.
*2 The bypass capacitor should be placed as close to the RA4000CE pins as possible.

Figure 9.2 Sample Connection Diagram with a Typical MCU (RA4000CE Option D/E)



*1 The pull-up resistor value for the /INT pin should be determined considering the output drive capability and output rise time.
*2 The bypass capacitor should be placed as close to the RA8000CE pins as possible.

Figure 9.3 Sample Connection Diagram with a Typical MCU (RA8000CE Option A/B/C)



*1 When the FOE pin function is used
*2 When the FOE pin function is not used
*3 The bypass capacitor should be placed as close to the RA8000CE pins as possible.

The RA8000CE Option D can be used as a high-precision temperature compensated crystal oscillator (32.768 kHz DTCXO).

Figure 9.4 Use as Oscillator (32.768 kHz DTCXO) (RA8000CE Option D)

10 Packing Information (reference)

Taping Specification (TE0804L)

Material of the Carrie Tape: PS
Material of the Top Tape: PET + PE

(Unit: mm)

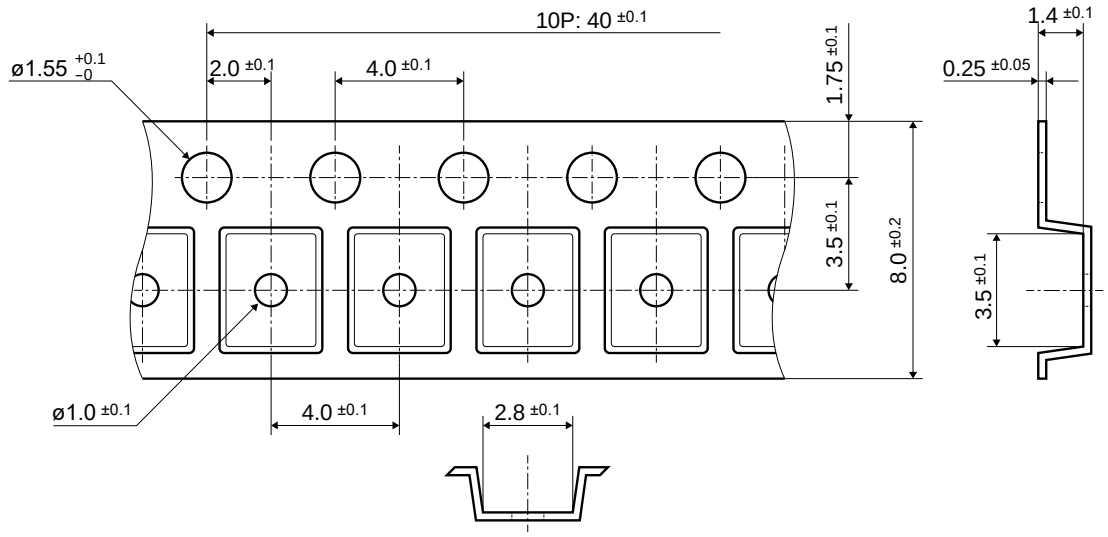
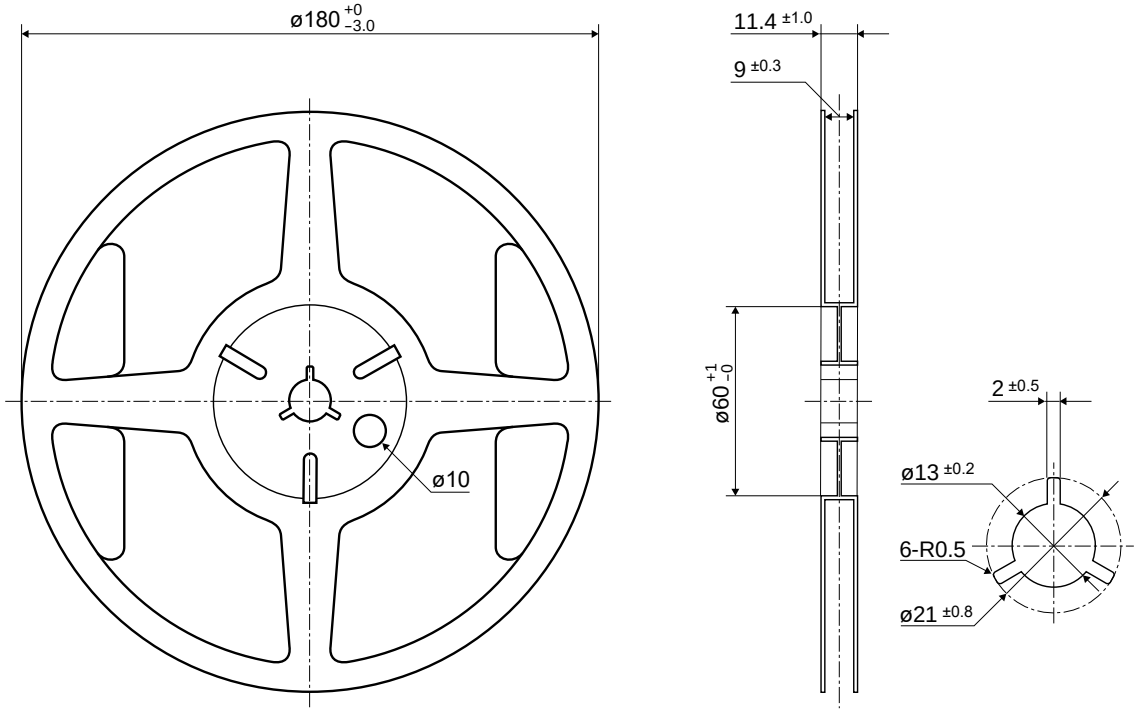


Figure 10.1 Tape Dimensions

Reel Specification

Material of the Reel: PS

(Unit: mm)



The reel window form and size are a typical example.

Figure 10.2 Reel Dimensions

List of Figures/Tables

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Application Manual

Real Time Clock Module

RA4000CE/RA8000CE

America

Epson America, Inc.

Headquarter

3131 Katella Avenue Los Alamitos, CA 90720 USA

www.epson.com/microdevices

San Jose Office

214 Devcon Drive, San Jose, CA 95112 USA

Europe

Epson Europe Electronics GmbH

Riesstrasse 15, 80992 Munich, Germany

www.epson-electronics.de

Asia

Epson (China) Co., Ltd.

Headquarter

4F, Tower 1 of China Central Place, 81 Jianguo Street, Chaoyang District, Beijing, 100025 China

www.epson.com.cn/ed

Shanghai Branch

High-Tech Building C900, Yishan Road, Shanghai 200233, China

Shenzhen Branch

Room 603-604, 6F, Tower 7, One Shenzhen Bay, No.3008 Center Rd, Shenzhen, 518054 China

Epson Hong Kong Ltd.

Unit 715-723 7/F Trade Square, 681 Cheung Sha Wan Road, Kowloon, Hong Kong

www.epson.com.hk

Epson Taiwan Technology & Trading Ltd.

15F., No.100, Songren Rd., Sinyi Dist.,Taipei City, 11073 Taiwan

www.epson.com.tw/ElectronicComponent

Epson Singapore Pte., Ltd.

Electronic Devices Sales Division Alexandra Technopark Block B, #04-01/04 438B Alexandra Rd, Singapore 119968

www.epson.com.sg/electronic-devices

Epson Korea Co.,Ltd

10F Posco Tower Yeoksam, Teheranro 134 Gangnam-gu, Seoul, 06235, Korea

www.epson.co.kr

Electronic devices information on WWW server

www5.epsondevice.com/en/