EPSON TOYOCOM

Application Manual

Real Time Clock Module

RTC-4574SA/JE/NB

EPSON TOYOCOM CORPORATION

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SERIAL-INTERFACE REAL TIME CLOCK MODULE

RTC – 4574 SA / JE / NB

- Built-in 32.768-kHz crystal resonator (with controlled frequency precision).
- Interface type : 3-wire serial interface
- Interface voltage range : 1.6 V to 5.5 V
- Voltage when during hold (timer hold) : 1.6 V to 5.5 V
- Current consumption during backup : 0.5 μA / 3 V (Typ.)
- 32.768-kHz output function with output control : FOUT pin output (C-MOS output)
- Real-time clock function
  Clock/calendar function, auto leap year correction function, alarm interrupt function, etc.

1. Overview

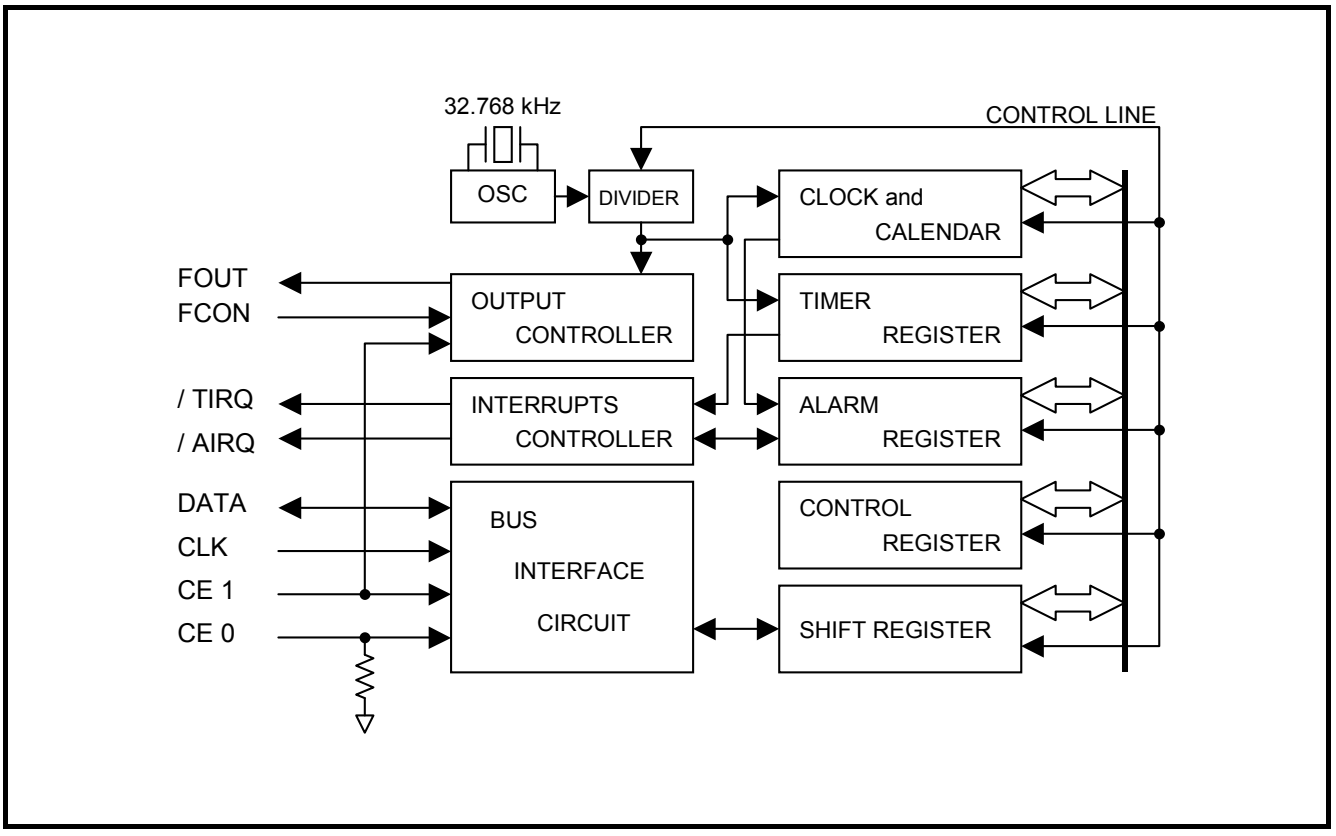
This module is a serial interface real time clock that has a built-in crystal unit.

The module offers many functions such as clock & calendar circuitry with automatic leap year adjustment (from seconds to year), alarm, and Timer interrupt. In addition, it can detect stopping of oscillation and time update.

The serial interface can be controlled by three signal lines, and it enables minimum number of ports required in the system.

Because it is available in two small packages, SOP-14 pin and VSOJ-20 pin and SON-22 pin, in high density mounting, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

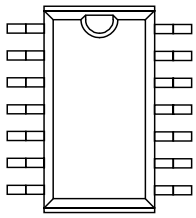
2. Block Diagram



3. Terminal description

3.1. Terminal connections

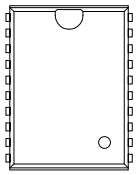
RTC – 4574 SA



1.	GND	14.	FCON
2.	FOUT	13.	CE1
3.	N.C.	12.	DATA
4.	N.C.	11.	CLK
5.	N.C.	10.	/ TIRQ
6.	N.C.	9.	/ AIRQ
7.	VDD	8.	CE0

SOP – 14 pin

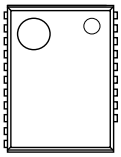
RTC – 4574 JE



1.	VDD	20.	N.C.
2.	FOUT	19.	N.C.
3.	CE0	18.	N.C.
4.	/ AIRQ	17.	N.C.
5.	/ TIRQ	16.	N.C.
6.	CLK	15.	N.C.
7.	DATA	14.	N.C.
8.	CE1	13.	N.C.
9.	FCON	12.	N.C.
10.	GND	11.	N.C.

VSOJ – 20 pin

RTC – 4574 NB



1.	GND	22.	N.C.
2.	FCON	21.	N.C.
3.	N.C.	20.	N.C.
4.	CE1	19.	N.C.
5.	DATA	18.	N.C.
6.	CLK	17.	N.C.
7.	/ TIRQ	16.	N.C.
8.	/ AIRQ	15.	N.C.
9.	CE0	14.	N.C.
10.	FOUT	13.	–
11.	VDD	12.	–

SON – 22 pin

3.2. Pin Functions

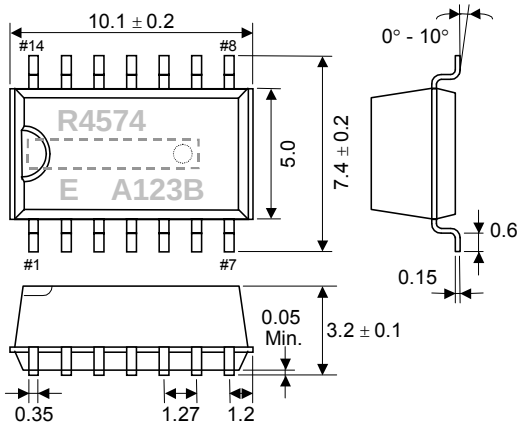
Signal name	I/O	Function
CE0	Input	This is a chip enabled 0 input pin with built-in pull-down resistors. When both CE0 and CE1 pins are at the "H" level, access to this RTC becomes possible.
CE1	Input	This is a chip enabled 1 input pin. When both CE0 and CE1 pins are at the "H" level, access to this RTC becomes possible. When the CE1 pin is at the "H" level, regardless of the state of the CE0 pin, the FOUT pin is in the output state. When the pin is at the "L" level, the FOUT pin is at the high impedance level.
CLK	Input	This is a shift clock input pin for serial data transmission. In the write mode, it takes in data from the DATA pin using the CLK signal rise edge. In the read mode, it outputs data from the DATA pin using the fall edge.
DATA	Bi-directional	This is a data input/output pin for serial data transmission. After the input rise of CE0 or CE1, by using the first 8-bit write data to set the write or read mode, this pin can be set as either input pin or output pin.
FOUT	Output	This pin outputs the clock signal of frequency set up at the frequency setup register and FCON input pin. See the following table for details. (CMOS output)
FCON	Input	This pin controls the FOUT output. When the CE1 pin is at the "H" level, if the FCON pin is set to "L", then regardless of the content of the frequency setup register, the FOUT pin outputs at 32.768 kHz. See the table below for details.
/ AIRQ	Output	This is an open drain output pin dedicated for alarm interrupt.
/ TIRQ	Output	This is an open drain output pin dedicated for Timer interrupt.
VDD	-	This pin connects to the plus side of the power.
GND	-	This pin connects to the minus side (ground) of the power.
N.C.	-	This pin is not connected internally. Be sure to connect using OPEN, or GND or VDD. But , In RTC-4574NB(SON-22pin), all pins from 14 pin to 22 pin are connected with inside frame mutually.

Note : Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

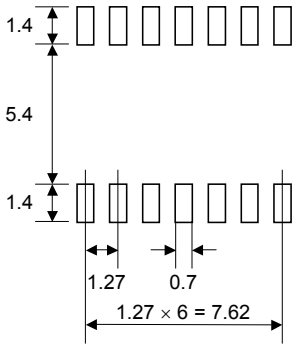
4. External Dimensions / Marking Layout

RTC - 4574 SA (SOP - 14 pin)

• External dimensions



• Recommended soldering pattern

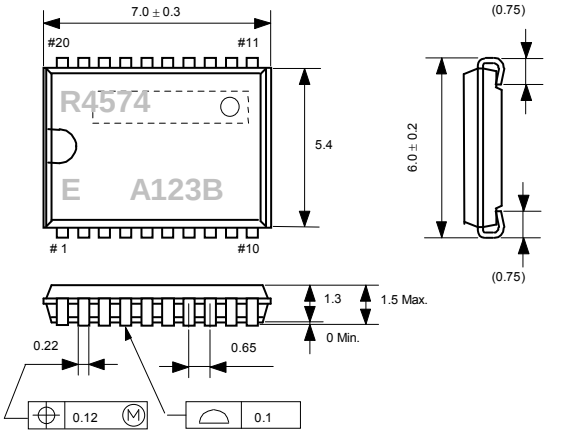


Unit : mm

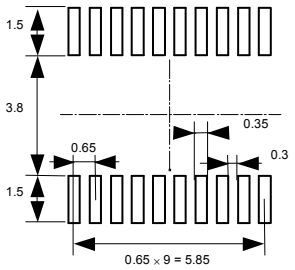
* The cylinder of the crystal oscillator can be seen in this area (front), but it has no affect on the performance of the device.

RTC - 4574 JE (VSOJ - 20 pin)

• External dimensions



• Recommended soldering pattern

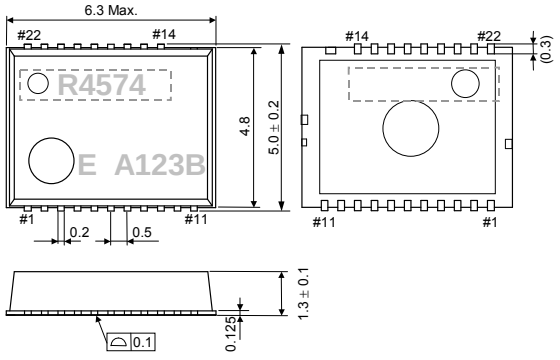


Unit : mm

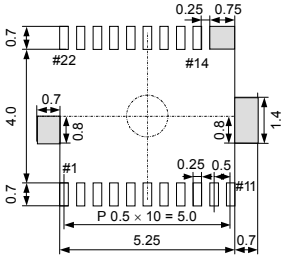
* The cylinder of the liquid crystal oscillator can be seen in this area (back and front), but it has no affect on the performance of the device.

RTC - 4574 NB (SON - 22 pin)

• External dimensions



• Soldering pattern



Unit : mm

*1) The cylinder of the crystal oscillator can be seen in this area (back and front), but it has no affect on the performance of the device.

*2) In this area, At a parts side of electronic base, you must not do layout any signal line.

5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	−0.3 to +7.0	V
Input voltage	V_{IN}	input pin	GND−0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	/ TIRQ, / AIRQ pins	GND−0.3 to +8.0	V
Output voltage (2)	V_{OUT2}	FOUT, DATA	GND−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

6. Recommended Operating Conditions

GND = 0 V V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	–	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.6	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

7. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Frequency precision	$\Delta f / f$	Ta = +25 °C, V_{DD} = 3.0 V	5 ± 23 (*1)	$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C, V_{DD} = 1.6 V ~ 5.5 V	± 2 Max.	$\times 10^{-6}$ / V
Frequency/temperature characteristics	Top	Ta = −20 °C ~ +70 °C, V_{DD} = 3.0 V ; +25 °C reference	+10 / −120	$\times 10^{-6}$
Oscillation start time	t_{STA}	Ta = +25 °C, V_{DD} = 1.6 V	3 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 5.0 V ; first year	± 5 Max.	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

8. Electrical Characteristics

8.1. DC characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

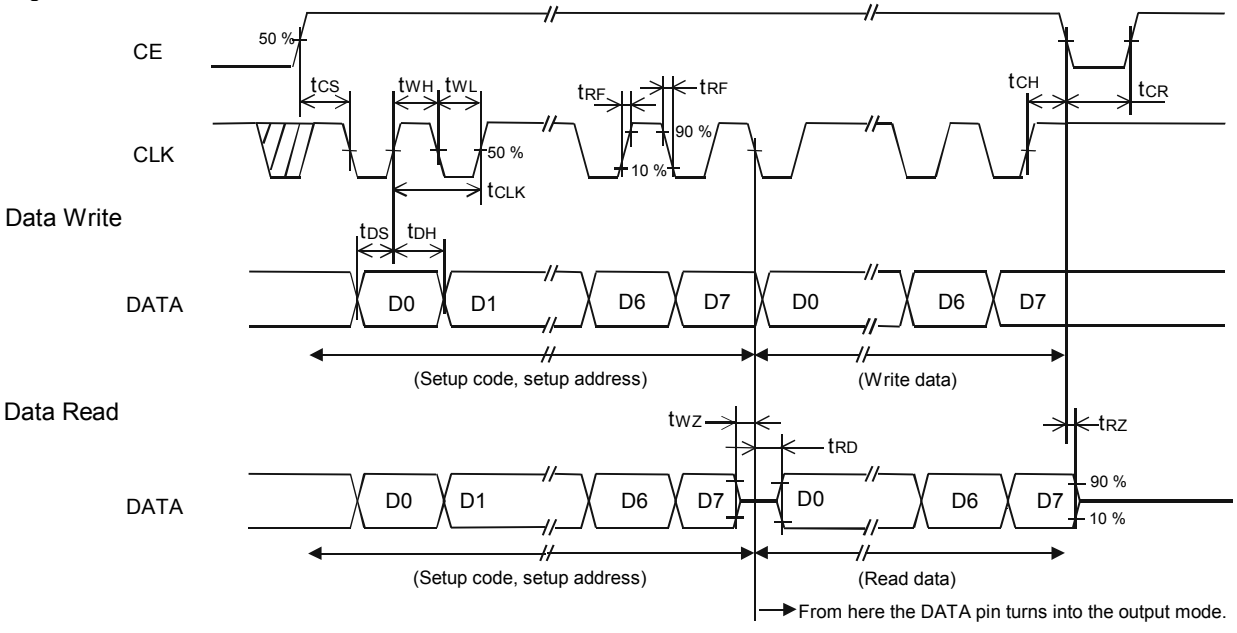
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE0, CE1 = GND DATA, /AIRQ, /TIRQ = V_{DD} FOUT ; output OFF (Hi - z)	V_{DD} = 5 V		1.0	2.0	μA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V		0.5	1.0	
Current consumption (3)	I_{DD3}	CE0 = GND CE1, DATA, /AIRQ, /TIRQ = V_{DD} FOUT; 32.768 kHz output ON , CL = 0 pF	V_{DD} = 5 V		3.0	7.5	μA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		1.7	4.5	
Current consumption (5)	I_{DD5}	CE0 = GND CE1, DATA, /AIRQ, /TIRQ = V_{DD} FOUT ; 32.768 kHz output ON , CL = 30 pF	V_{DD} = 5 V		8.0	20.0	μA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		5.0	12.0	
High-level input voltage	V_{IH1}	CE0, CE1, CLK, DATA, FCON pins		0.7 × V_{DD}		V_{DD} + 0.3	V
	V_{IH2}	/ AIRQ, / TIRQ pins		0.8 × V_{DD}		V_{DD}+0.3	V
Low-level input voltage	V_{IL}	CE0, CE1, CLK, DATA, FCON pins		GND – 0.3		0.2 × V_{DD}	V
High-level output voltage	V_{OH1}	DATA, FOUT pins	V_{DD} = 5 V, I_{OH} = –1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA	2.0		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 μA	2.9		3.0	
Low-level output voltage	V_{OL1}	DATA, FOUT pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 μA	GND		GND+0.1	
	V_{OL4}	/ AIRQ and / TIRQ pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	
Input resistance (1)	R_{DWN1}	CE0 pin V_{IN} = V_{DD}	V_{DD} = 5 V	75	150	300	kΩ
Input resistance (2)	R_{DWN2}		V_{DD} = 3 V	150	300	600	kΩ
Input leakage current	I_{LK}	CE0 pin ; V_{IN} = GND CE1, CLK, FCON pins ; V_{IN} = V_{DD} or GND		–0.5		0.5	μA
Output leakage current	I_{OZ}	DATA, / AIRQ, / TIRQ, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	μA

8.2. AC characteristics

* Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	V_{DD} = 3 V ± 10 %			V_{DD} = 5 V ± 10 %			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK clock cycle	t_{CLK}		800			350			ns
CLK H pulse width	t_{WH}		400			175			ns
CLK L pulse width	t_{WL}		400			175			ns
CE setup time	t_{CS}		400			175			ns
CE hold time	t_{CH}		400			175			ns
CE recovery time	t_{CR}		600			300			ns
Write data setup time	t_{DS}		100			50			ns
Write data hold time	t_{DH}		80			50			ns
Write data disable time	t_{WZ}		0			0			ns
Read data delay time	t_{RD}	CL = 50 pF			300			120	ns
Output disable time	t_{RZ}	CL = 50 pF RL = 10 kΩ			200			100	ns
Input rise/fall time	t_{RF}				100			50	ns
FOUT duty (when output at 32.768 kHz)	tW / t	50 % V_{DD} level	35		65	40		60	%

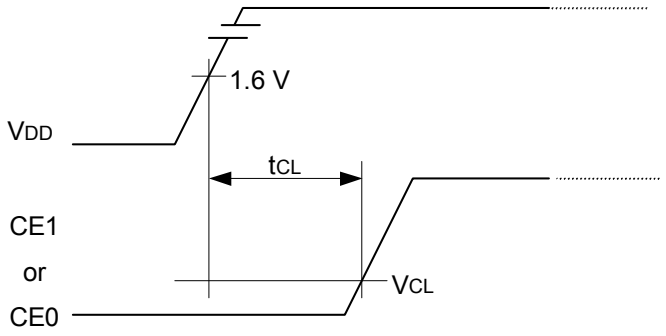
Timing chart



9. Matters that demand special attention on use

9.1. VDD and CE timing

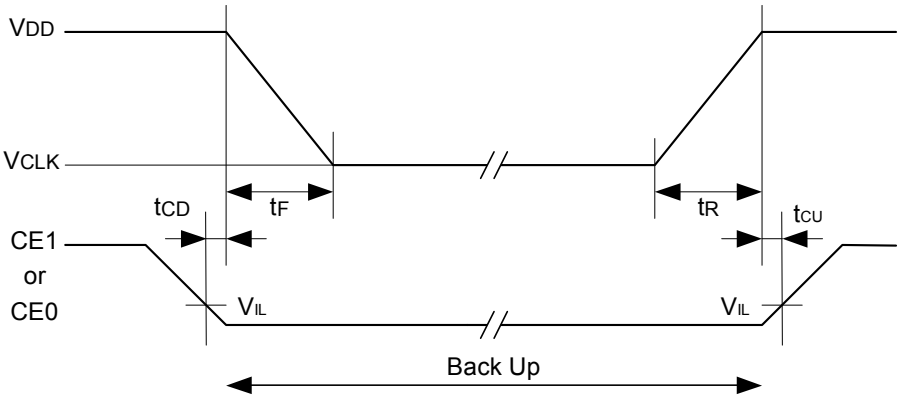
* When the power is turned to ON, use with CE = " L " (VCL[V] in the diagram) as illustrated in the following timing chart.



Item	Symbol	Remark	Specification	Unit
CE voltage when power is turned to ON	VCL	CE impressed voltage until VDD = 1.6 V	0.3 (Max.)	V
CE=VCL[V] time when power is turned to ON	tCL	Time to maintain CE=VCL[V] until VDD = 1.6 V	10 (Min.)	µs

9.2. Migrating to backup, and returning

* When migrating to backup, before switching the power source, make sure CE1 or CE0 is definitely LOW and RTC is not selected

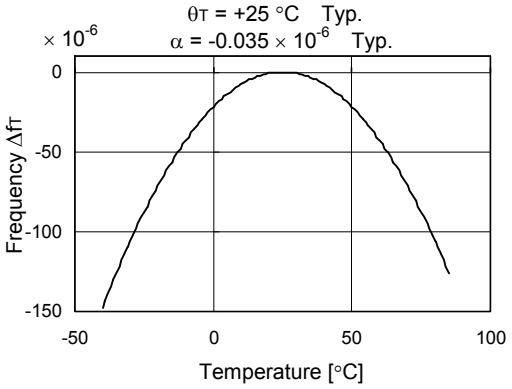


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power drop	tCD	–	0			µs
Power drop time	tF	(VDD – VCLK) ≤ 2.0 V	2			µs / V
		(VDD – VCLK) > 2.0 V	50			µs / V
Power rise time	tF	–	1			µs / V
CE time after power rise	tCU	–	0			µs

10. Reference information

10.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta fv$

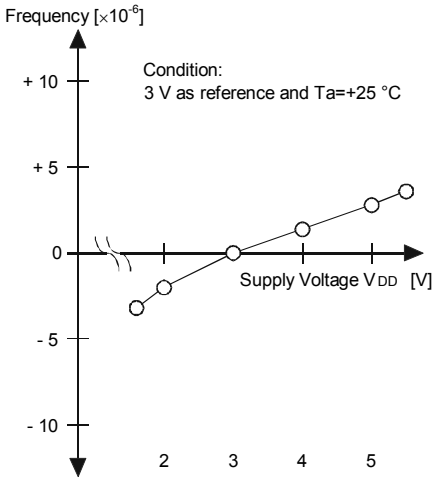
   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δfv : Frequency deviation in any voltage.

3. How to find the date difference

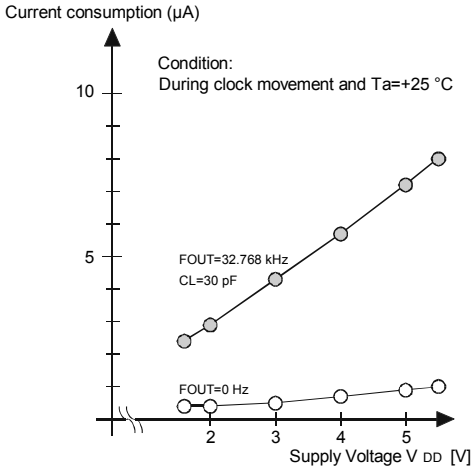
   Date Difference = $\Delta f/f \times$ 86400(Sec)

   * For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

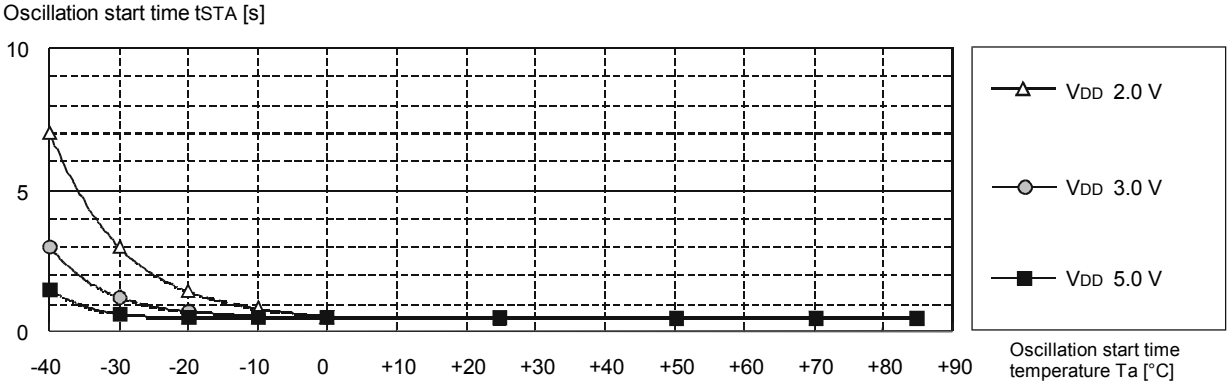
(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/voltage characteristics

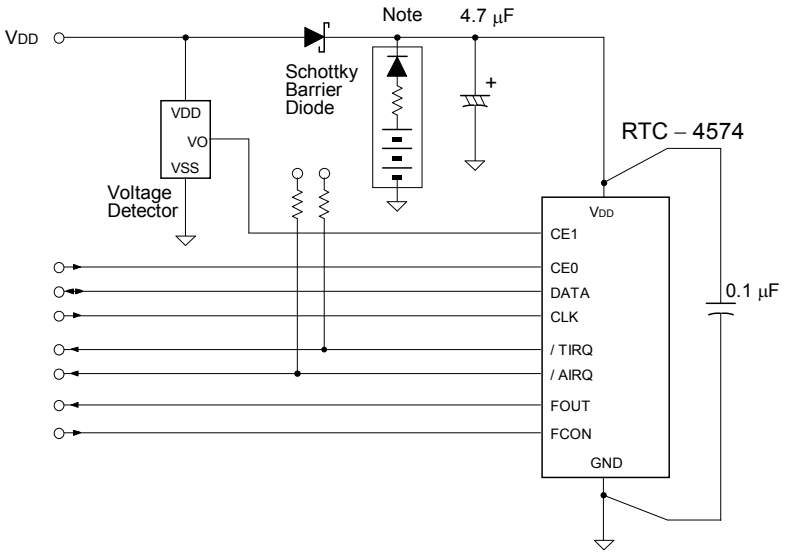


(4) Oscillation start time characteristics



Note: This data is taken from the sample lot. For the rated value, see the specification on [7. Frequency Characteristics] .

10.2. External connection example



Note :

It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required. For detailed value on the resistance, please consult a battery maker.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

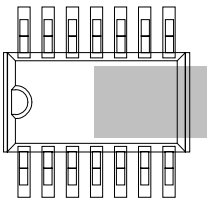
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

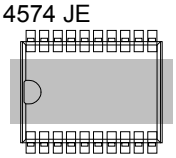
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

RTC - 4574 SA



RTC - 4574 JE



RTC - 4574 NB

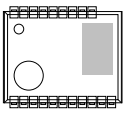
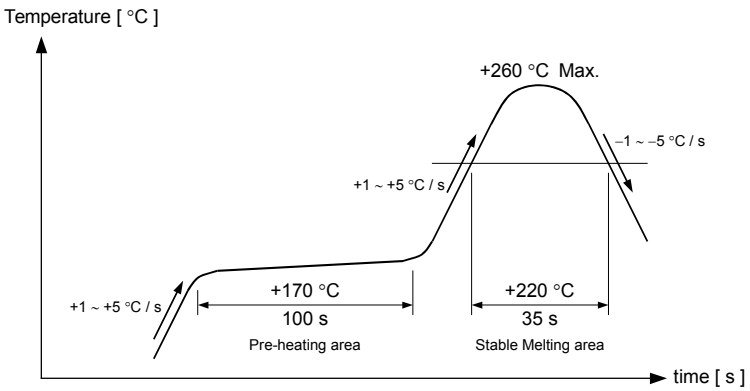


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



12. Overview of Functions and Description of Registers

12.1. Overview of Functions

1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

∗ For details, see "13.1. Description of Registers".

2) Fixed-cycle interrupt generation function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 255 minutes.

When an interrupt event is generated, the /TIRQ pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred..

This function can be selected from two types of operations (single-shot operations and repeated operations).

∗ For details, see "13.2. Fixed-cycle Interrupt Function". .

3) Alarm interrupt function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.

∗ For details, see "13.3. Alarm Interrupt Function".

4) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin (CMOS output).

In cases where another output frequency is required, 32 output frequencies can be selected in a range from 1/30 Hz to 32.768 kHz.

12.2. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Remark
0	SEC	fos	40	20	10	8	4	2	1	∗1
1	MIN	fr	40	20	10	8	4	2	1	–
2	HOUR	fr	○	20	10	8	4	2	1	∗3
3	WEEK	fr	6	5	4	3	2	1	0	–
4	DAY	fr	○	20	10	8	4	2	1	∗3
5	MONTH	fr	○	○	10	8	4	2	1	∗3
6	YEAR	80	40	20	10	8	4	2	1	–
7	MIN Alarm	AE	40	20	10	8	4	2	1	–
8	HOUR Alarm	AE	•	20	10	8	4	2	1	∗4
9	WEEK Alarm	AE	6	5	4	3	2	1	0	–
A	DAY Alarm	AE	•	20	10	8	4	2	1	∗4
B	Frequency Setup	FE	•	FD4	FD3	•	FD2	FD1	FD0	∗1, ∗4
C	Timer Setup	TE	•	TD1	TD0	•	•	•	•	∗1, ∗4
D	Timer Counter	128	64	32	16	8	4	2	1	–
E	Control Register 1	○	○	○	TI / TP	AF	TF	AIE	TIE	∗3
F	Control Register 2	○	TEST	STOP	RESET	HOLD	○	○	○	∗1, ∗2, ∗3

Note When after the initial power-up or when the result of read out the fos bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗1. During the initial power-up, the fos bit is set to "1".
∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.

∗2. The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

∗3. Any bit marked with ' ○ ' should be used with a value of "0" after initialization.

∗4. Any bit marked with ' • ' is a RAM bit that can be used to read or write any data.

13. Description of Functions

13.1. Description of registers

13.1.1. Clock counter (Reg - 0[h] ~ 2[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	SEC	fos	40	20	10	8	4	2	1
1	MIN	fr	40	20	10	8	4	2	1
2	HOUR	fr	○	20	10	8	4	2	1

- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.
- The fr bit is flag bit that indicates the operation status of the RTC's internal clock counter.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) Second counter (Reg - 0[h])
This counter counts seconds.
Count values are updated as: 00 seconds, 01 second, 02 to 59 seconds, 00 seconds, 01 second, etc. in that order.

2) Minute counter (Reg - 1[h])
This counter counts minutes.
Count values are updated as: 00 minutes, 01 minute, 02 to 59 minutes, 00 minutes, 01 minute, etc. in that order.

3) Hour counter (Reg - 2[h])
This counter counts hours.
Count values are updated as: 00 hours, 01 hour, 02 to 23 hours, 00 hours, 01 hour, etc. in that order.

4) fos bit (OSC Flag)
This is a flag bit that retains the result when this RTC's internal oscillation status is detected.
If the RTC's internal oscillation is stopped, such as when a drop occurs in the power supply voltage, the value of this bit changes from "0" to "1 ".
If this bit's value is "1" when read, this RTC's data is ignored, in which case all registers should be initialized before being used.

∗ This bit is set (= 1) during the initial power-on.
∗ After confirming that this bit's value is "1" when read, be sure to clear this fos bit to zero in preparation for the next detection operation.

5) fr bit (READ Flag)
This is a read-only flag bit that indicates the clock status when read.
If the clock counter is incremented during a read operation, the value of this bit changes from "0" to "1 ".
If this bit's value is "1" when read, it may be due to updating of other clock data, in which case all clock registers should be read again.

∗ This fr bit is automatically cleared to zero when the CE0 input pin or CE1 input pin goes to low level.
∗ The fr bits in Reg – 1 to 5 all have the same function.

13.1.2. . Day counter (Reg - 3[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	WEEK	fr	6	5	4	3	2	1	0

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

[WEEK]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data [h]
Write / Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	∗ Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

13.1.3. Calendar counter (Reg - 04[h] ~ 06[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	DAY	fr	○	20	10	8	4	2	1
5	MONTH	fr	○	○	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1) Date counter (Reg - 04[h])

- This is the date counter.
  Updating of this counter varies depending on the month.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

2) Month counter (Reg - 05[h])

- This is the month counter.
  It is updated in annual cycles of regularly ordered months (January, February, March, etc.).

3) Year counter (Reg - 06[h])

- This is the year counter.
  It is updated in 100-year cycles of regularly ordered years (00, 01, 02 to 99, etc.).
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

13.1.4. Alarm registers (Reg - 7[h] ~ A[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	MIN Alarm	AE	40	20	10	8	4	2	1
8	HOUR Alarm	AE	•	20	10	8	4	2	1
9	WEEK Alarm	AE	6	5	4	3	2	1	0
A	DAY Alarm	AE	•	20	10	8	4	2	1

- The AIE bit and AFT bit can both be set or used when using alarm interrupt function to set interrupt events for dates, days, hours, minutes, etc.
- When the current time matches the settings in the above alarm registers, the AF bit's value is "1" and the AIRQ pin's status is low to indicate that an alarm interrupt event has occurred.

∗ For details, see "13.3. Alarm Interrupt Function".

13.1.5. Timer setting and Timer counter register (Reg - C[h] ~ D[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	Timer Setup	TE	•	TD1	TD0	•	•	•	•
D	Timer Counter	128	64	32	16	8	4	2	1

- When using the fixed-cycle timer interrupt function, these registers are used to select the cycle (source clock) to control or serve as a basis for operations, and to set the initial value (preset value) for the countdown operation.
- When using the fixed-cycle timer interrupt function, these bits can be set or used along with the TI/TP, TE, TF, TIE, and TD1,0 bits.
- When the value of the above timer counter (Reg - D) goes from 01h to 00h, the TF bit value (= 1) and the /TIRQ pin's low status indicate the occurrence of a fixed-cycle timer interrupt event.

  At that time, if the TI/TP bit's value is "0" the operation ends after one execution (level interrupt mode). If the TI/TP bit's value is "1", execution of the operation is automatically repeated continuously (repeated interrupt mode).

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

13.1.6. Output frequency setup register (Reg - B[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Frequency Setup	FE	•	FD4	FD3	•	FD2	FD1	FD0

- This register is used to control the FOUT pin's clock output.
- When CE1 = "H" and FCON = "H" this register is valid and its settings determine whether or not clock output is stopped.

∗ Relationship between the FOUT output and RTC access, based on CE0, CE1, FCON pin and FE bit

CE0	CE1	FCON	FE	FOUT output	RTC access
L	L	X	X	high impedance	no
H	L	X	X	high impedance	
L	H	L	0	output at 32.768 kHz	
		L	1	output at 32.768 kHz	
		H	0	high impedance	
		H	1	FD bit selection frequency output	
H	H	L	0	output at 32.768 kHz	yes
		L	1	output at 32.768 kHz	
		H	0	high impedance	
		H	1	FD bit selection frequency output	

X : don't care

* When CE1 = "H" and FCON = "L" this register's settings are invalid and the FOUT pin outputs at 32.768 kHz.

1) FE bit (FOUT Enable)

The FOUT pin's output mode can be controlled only when this register is valid (when CE1 = "H" and FCON = "H").
When a "1" is written, the FOUT pin is set to output mode (CMOS output). At that time, the output consists of the frequency (source clock) set via the FD4 and FD3 bits, divided by the division rate specified via the FD2, FD1, and FD0 bits.
When "0" is written, the FOUT pin is set to output prohibit mode (high impedance).

2) FD4, FD3 bits

Use a combination of settings to the FD4 and FD3 bits to select the basic frequency (= source clock).

FD4	FD3	Source clock
0	0	32768 Hz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

3) FD2 to FD0 bits

Use a combination of settings to the FD2, FD1, and FD0 bits to select the division rate for the source clock.

FD2	FD1	FD0	Divided ratio	FOUT Duty
0	0	0	1 / 1	50 %
0	0	1	1 / 2	50 %
0	1	0	1 / 3	33 %
0	1	1	1 / 6	50 %
1	0	0	1 / 5	20 %
1	0	1	1 / 1 0	50 %
1	1	0	1 / 1 5	33 %
1	1	1	1 / 3 0	50 %

4) FOUT output frequency

The source clock specified via the FD4 and FD3 bits is divided using the division rate specified via the FD2, FD1, and FD0 bits before being output from the FOUT pin.

FD2	FD1	FD0	FD4,3 0,0	FD4,3 0,1	FD4,3 1,0	FD4,3 1,1	FOUT Duty [%]
0	0	0	32768 Hz	1024 Hz	32 Hz	1 Hz	50 %
0	0	1	16384 Hz	512.0 Hz	16.0 Hz	1/2 Hz	50 %
0	1	0	10922 Hz	341.3 Hz	10.67 Hz	1/3 Hz	33 %
0	1	1	5461 Hz	170.67 Hz	5.33 Hz	1/6 Hz	50 %
1	0	0	6553.6 Hz	204.8 Hz	6.4 Hz	1/5 Hz	20 %
1	0	1	3276.8 Hz	102.4 Hz	3.2 Hz	1/10 Hz	50 %
1	1	0	2184.5 Hz	68.27 Hz	2.13 Hz	1/15 Hz	33 %
1	1	1	1092.3 Hz	34.13 Hz	1.07 Hz	1/30 Hz	50 %

13.1.7. Control register 1 (Reg - E[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control Register 1	○	○	○	TI / TP	AF	TF	AIE	TIE

- This register is used to record the result of various interrupt event detection operations, or to control the interrupt signal that is externally output when an interrupt event occurs.

1) TI / TP bit (Interrupt Signal Output Mode Select. Interrupt / Periodic)

When a fixed-cycle timer interrupt event occurs (when the TF bit goes from "0" to 1") , this bit specifies whether the interrupt operation occurs just once or repeatedly.
Writing "1" to this bit sets repeated operation.
Writing "0" to this bit sets single-shot operation.

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

2) AF bit (Alarm Flag)

This is a flag bit that retains the result when an alarm interrupt event has been detected.
When an alarm interrupt event occurs, this bit's value changes from "0" to "1".

∗ For details, see "13.3. Alarm Interrupt Function".

3) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event has been detected.
When a fixed-cycle timer interrupt event occurs, this bit's value changes from "0" to "1".

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

4) AIE bit (Alarm Interrupt Enable)

This bit sets the operation of the /AIRQ interrupt signal when an alarm interrupt event has occurred (the AF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /AIRQ pin.
Writing "0" to this bit prohibits low-level output from the /AIRQ pin.

∗ For details, see "13.3. Alarm Interrupt Function".

5) TIE bit (Timer Interrupt Enable)

This bit sets the operation of the /TIRQ interrupt signal when a fixed-cycle interrupt event has occurred (the TF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /TIRQ pin.
Writing "0" to this bit prohibits low-level output from the /TIRQ pin.

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

13.1.8. Control register 2 (Reg - F[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control Register 2	○	TEST	STOP	RESET	HOLD	○	○	○

• This register is used to control stop and resume operations (of the clock and calendar function, etc.).

1) TEST bit

This is the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

* If this bit is inadvertently set (= "1") there is a safety function that auto-clears the TEST bit to zero when the CE0 pin or CE1 pin goes to low level.

2) STOP bit

This bit stops the clock's operation.
Writing "1" to this bit stops the clock.
Writing "0" to this bit restarts the clock (cancels stop mode).
When an STOP bit was set to 1, please perform the next write access after the 62 micro-seconds (Min.).

* This type of function should only be used for clock and calendar settings.

3) RESET bit

Like the STOP function described above, this bit stops the counter operation and resets the internal counter when its value is less than one second.
Writing "1" to this bit stops the counter's operation and resets the RTC's internal counter when its value is less than one second.
Writing a "0" to this bit or setting the CE0 pin or CE1 pin to low level automatically clears (resets) this bit to zero.

∗ This type of function should only be used for clock and calendar settings.

4) Relation between STOP/RESET bits and other operations

When either the STOP bit or the RESET bit has a value of "1", the clock function, calendar function, and various interrupt functions are stopped and cannot operate correctly.

∗ Do not leave the STOP bit value or RESET bit value as "1".

5) HOLD bit

This bit pauses updating of the clock register.
Writing "1" to this bit stops incrementation of the ones column.
Writing "0" to this bit cancels pause mode (resumes clock updates). When this bit's value is returned from "1" to "0", if an internal update has occurred in the meantime, an auto compensation function automatically performs a one-second clock update.

* Even if the time during which HOLD = "1" is two or more seconds, the auto compensation function only compensates the clock update by one second, so using the HOLD bit for one second or less is recommended.

6) STOP, RESET, HOLD bit settings and operation of functions

bit			Function			
STOP	RESET	HOLD	Clock	Timer	Alarm	FOUT
0	0	0	runs	runs	runs	runs
0	0	1	*1	*2	stops	runs
0	1	0	stops	*3	stops	*4
0	1	1	stops	*3	stops	*4
1	0	0	stops	*3	stops	*4
1	0	1	stops	*3	stops	*4
1	1	0	stops	*3	stops	*4
1	1	1	stops	*3	stops	*4

*1: If the deviation is within one second, the automatic compensation function will kick in to perform the automatic compensation.
*2: Runs at source clock other than source clock at 1/60 Hz (1 min).
*3: Runs when the source clock is at 4096 Hz.
*4: Runs when the source clock is at 32768 Hz.

13.2. Fixed-cycle Timer Interrupt Function

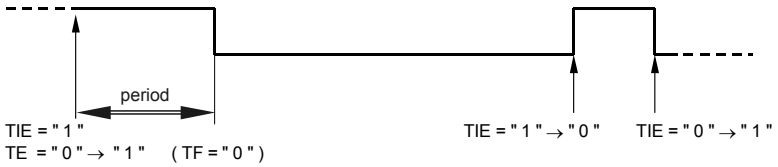
The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 255 minutes.

When an interrupt event occurs, the TF bit value changes to "1" and the /TIRQ pin goes to low level to indicate that an event has occurred.
At that time, if the TI/TP bit value is "0" the current operation ends after one iteration (level interrupt mode is set *1).
If the TI/TP bit value is "1" the current operation is automatically repeated continuously (repeated interrupt mode *2).

∗1) Outline drawing of level interrupt mode (TI/TP = "0")

After an interrupt event occurs, the operation is performed only once.

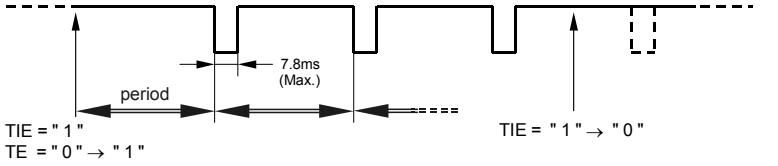
∗Example of /TIRQ operation



∗2) Outline drawing of repeated interrupt mode (TI/TP = "1")

After an interrupt event occurs, the operation is performed repeatedly.

∗Example of /TIRQ operation



13.2.1. Related registers for function of timer interrupts.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	Timer Setup	**TE**	•	**TD1**	**TD0**	•	•	•	•
D	Timer Counter	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
E	Control Register 1	○	○	○	**TI / TP**	AF	**TF**	AIE	**TIE**

∗ Before entering settings for operations, we recommend writing a "0" to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the timer interrupt function is not being used, the fixed-cycle timer counter register (Reg – D) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TI / TP bit (Interrupt Signal Output Mode Select. Interrupt / Periodic)

When a fixed-cycle timer interrupt event occurs (TF value changes from "0" to 1"), this bit specifies whether the interrupt operation will be performed only once or repeatedly.

TI / TP	Data	Description
Write / Read	0	[Level interrupt mode] Fixed-cycle timer interrupt function operates only once
	1	[Repeated interrupt mode] Fixed-cycle timer interrupt function operates repeatedly

2) TD1, TD0 bits

These bits specify the fixed-cycle timer interrupt function's countdown period (source clock).
Four different periods can be selected via combinations of these two bit values.

TD1, TD0	TD1 (bit 5)	TD0 (bit 4)	Source clock	Auto reset time tRTN
W / R	0	0	4096 Hz / Once per 244.14 μs	122 μs
	0	1	64 Hz / Once per 15.625 ms	7.813 ms
	1	0	1 Hz / Once per second	7.813 ms
	1	1	1/60 Hz / Once per minute	7.813 ms

∗1) The /TIRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) An interrupt that occurs when the source clock is in 1/60 Hz mode is linked to the internal clock's "minute" update operation.

∗3) An interrupt that occurs when the source clock is in 1 Hz mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)

3) Down counter for fixed-cycle timer (Timer Counter)

This register is used to set the default (preset) value for the counter. Any count value from 1 (01 h) to 255 (FFh) can be set

The counter counts down based on the source clock's period, and when the count value changes from 01h to 00h, the TF bit value becomes "1".

∗1. The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.
(Status cannot be read during countdown.)

∗2. When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – D) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

4) TE bit (Timer Enable)

This bit enables operation of the of the fixed-cycle timer interrupt function to start.

TE	Data	Description
Write/Read	0	Stops fixed-cycle timer interrupt function
	1	Starts fixed-cycle timer interrupt function ∗ Countdown enabled when the TE bit value changes from "0" to "1" starts at a preset value. (Note) During level interrupt mode (single-shot operation mode), the TF bit first should be cleared to zero, then the TE bit value should be changed from "0" to "1".

5) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

The value of this bit changes from "0" to "1" when a fixed-cycle timer interrupt event occurs. If the TIE bit value is “1" at that time, the /TIRQ pin goes to low level to indicate that an event has occurred.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ∗ When this bit is cleared to zero, low level output of /TIRQ is canceled (Hi-Z mode is set).
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. ∗ Result is retained until this bit is cleared to zero

6) TIE bit (Timer Interrupt Enable)

This bit sets the operation of the /TIRQ interrupt signal when a fixed-cycle timer interrupt event has occurred (TF bit value changes from "0" to "1").

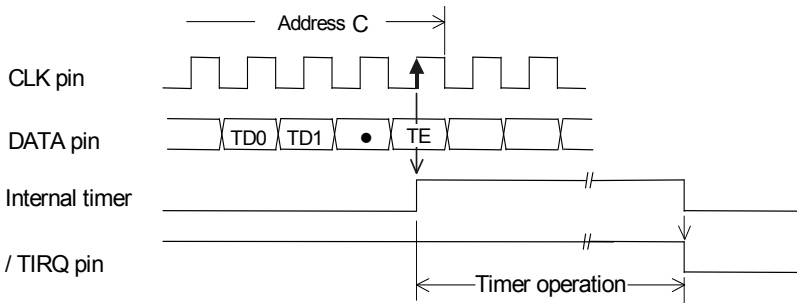
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /TIRQ pin.

When a "0" is written to this bit, output from the /TIRQ pin is prohibited (disabled).

TIE	Data	Description
Write / Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).

13.2.2. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the CLK signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



13.2.3. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings (settings in TD1 and TD0) and fixed-cycle timer countdown setting (Reg–C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting	Source clock			
	4096 Hz TD1,0 = 0,0	64 Hz TD1,0 = 0,1	1 Hz TD1,0 = 1,0	1/60 Hz TD1,0 = 1,1
0 (00h)	–	–	–	–
1 (01h)	244.14 μs	15.625 ms	1 s	1 min
2 (02h)	488.28 μs	31.250 ms	2 s	2 min
3 (03h)	732.42 μs	46.875 ms	3 s	3 min
⋮	⋮	⋮	⋮	⋮
255 (FFh)	62.26 ms	3.984 s	255 s	255 min

- Fixed-cycle timer interrupt time error and fixed-cycle timer interrupt interval time

A fixed-cycle timer interrupt time error is an error in the selected source clock's $^{+0}/_{-1}$ interval time. Accordingly, the fixed-cycle timer interrupt's interval (one cycle) falls within the following range in relation to the set time.

Fixed-cycle timer interrupt's interval

(Fixed-cycle timer interrupt's set time(∗) – source clock interval) to (fixed-cycle timer interrupt set time)

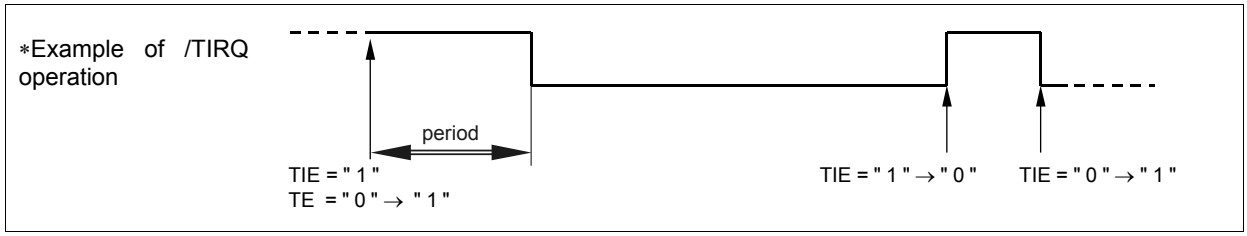
∗) Fixed-cycle timer interrupt's set time = Source clock setting × Countdown timer setting for fixed-cycle timer

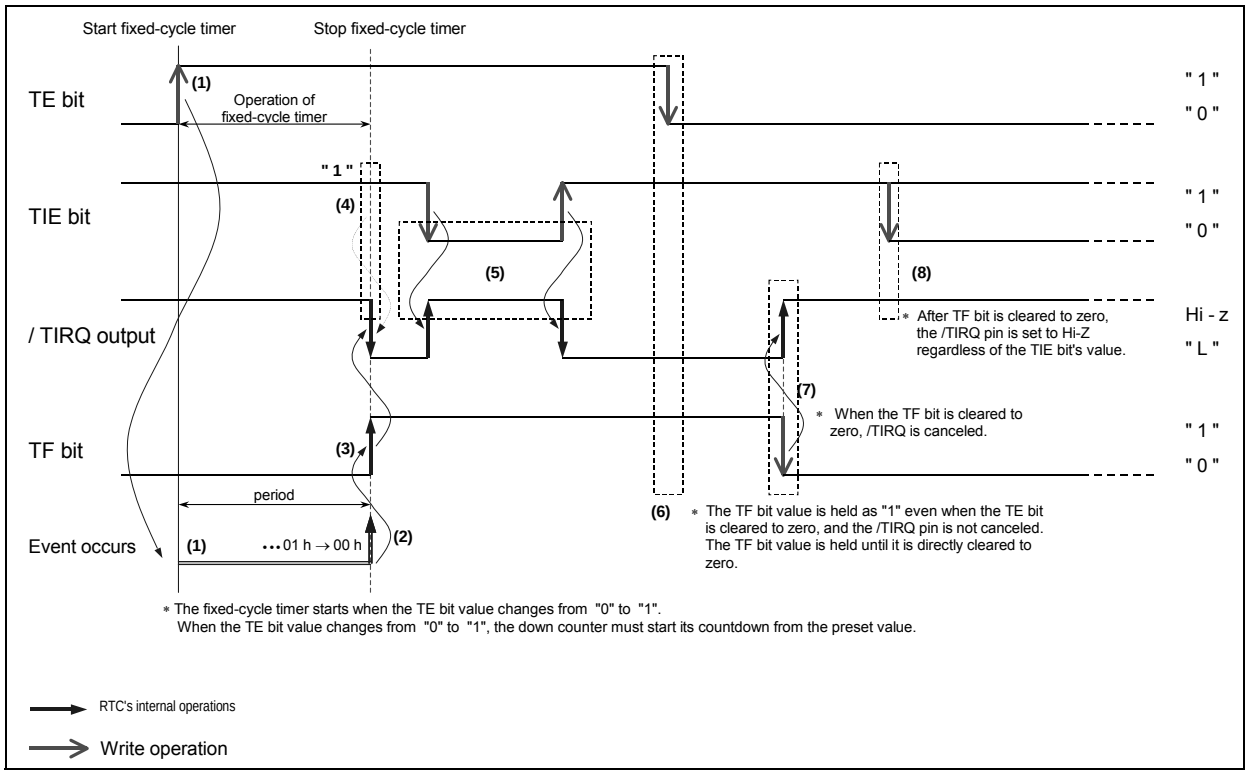
∗ The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

13.2.4. Diagram of fixed-cycle timer interrupt function

13.2.4.1. Level interrupt mode (TI / TP = "0")

- After an interrupt event has occurred, this function operates only once.





∗) Before using level interrupt mode (TI / TP = "0") , be sure to clear the TE bit and the TF bit to zero each time.

(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 01h to 00h, an interrupt event occurs.

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /TIRQ pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /TIRQ pin output remains Hi-Z.

(5) During the period when the TF bit value is "1" following the occurrence of an interrupt event, the TIE bit can be set to switch the /TIRQ pin to any status.

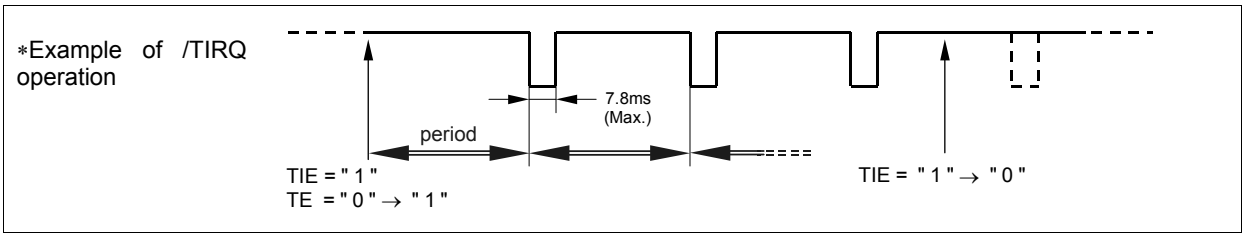
(6) When the TF bit = "1" its value is retained until it is cleared to zero.
Even when the TE bit is cleared to zero, the TF bit value is retained as "1" and the /TIRQ pin status is not reset.

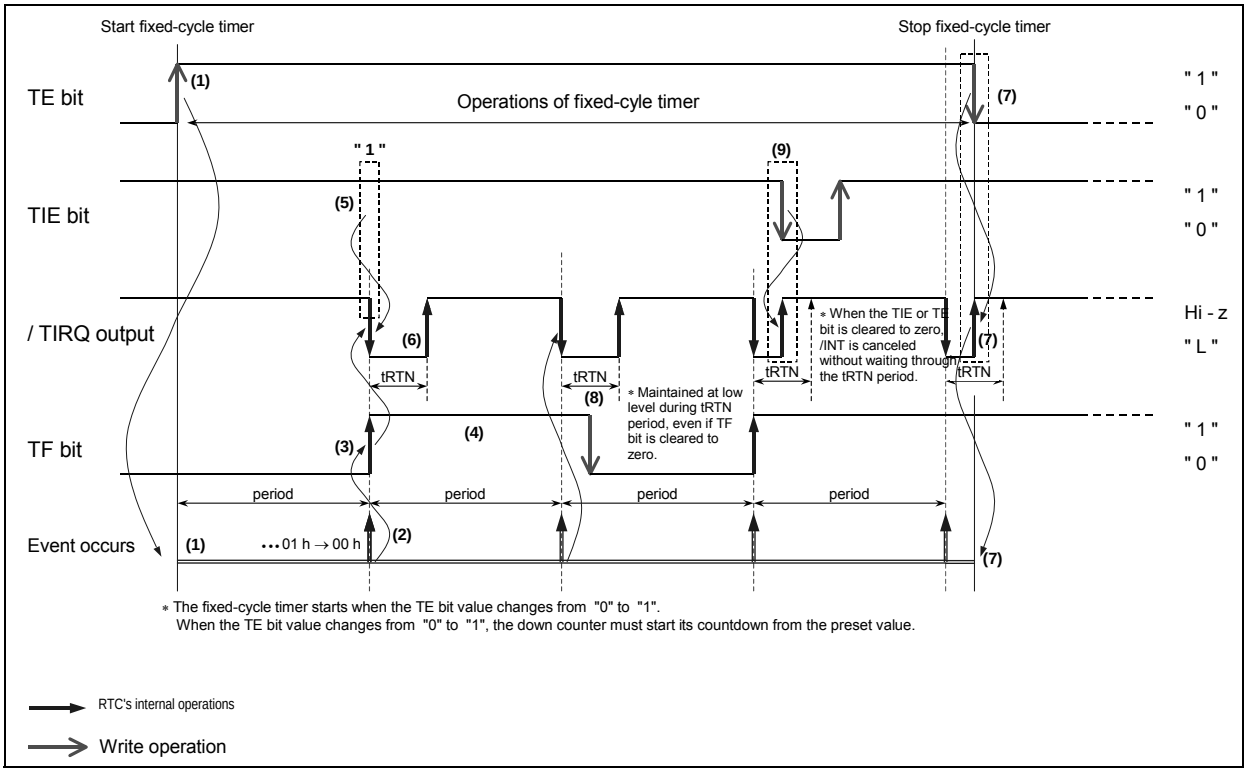
(7) When the TF bit is cleared to zero, the /TIRQ pin status is reset (is switched from low level to Hi-Z).

(8) After the TF bit is cleared to zero, the /TIRQ pin is set to Hi-Z status regardless of the TIE bit's value.

13.2.4.2. Repeated interrupt mode (TI/TP = "1")

- After an interrupt event has occurred, execution of the operation is automatically repeated continuously.





(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 01h to 00h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.
(Even when the TE bit is cleared to zero, the TF bit value is retained as "1".)

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /TIRQ pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /TIRQ pin output remains Hi-Z.

(6) Output from the /TIRQ pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /TIRQ is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /TIRQ pin is set to Hi-Z status.

(8) When /TIRQ is at low level and the TF is changed from "1" to “0", / TIRQ remains at low level and is not reset to Hi-Z status.

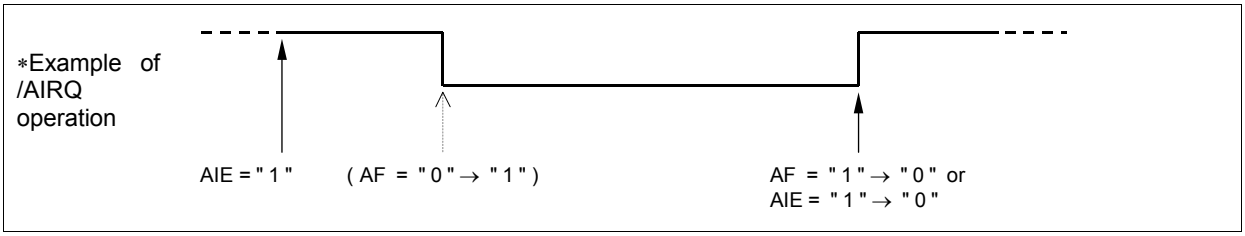
(9) When /TIRQ = low, the /TIRQ pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

13.3. Alarm Interrupt Function

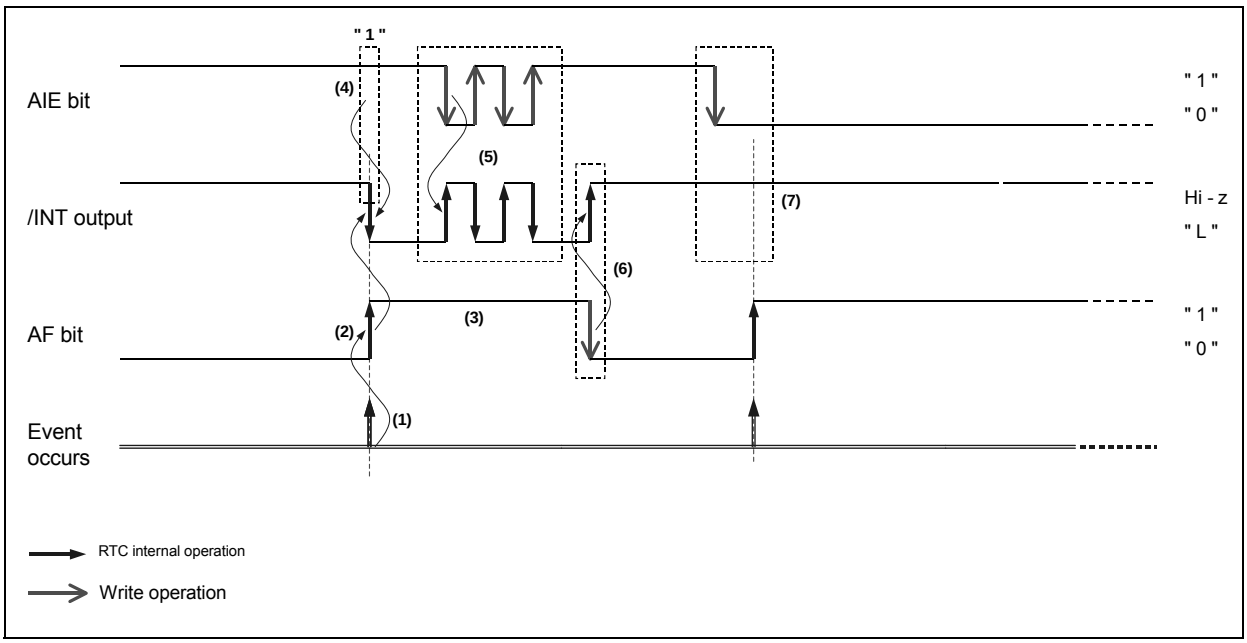
The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.

∗ When an alarm interrupt event occurs, low-level output from /AIRQ is not automatically reset (it can be reset only intentionally) and the low-level status of /AIRQ is retained.



13.3.1. Diagram of alarm interrupt function



(1) The minute, hour, day of week, and date at which an alarm interrupt event will occur is set in advance, and the interrupt event occurs when the current time matches this pre-set time.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /AIRQ pin output goes low.
∗ When an alarm interrupt event occurs, /AIRQ pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /AIRQ is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /AIRQ status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /AIRQ status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /AIRQ pin status remains Hi-Z.

13.3.2. Alarm interrupt function registers

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	MIN	fr	**40**	**20**	**10**	**8**	**4**	**2**	**1**
2	HOUR	fr	○	**20**	**10**	**8**	**4**	**2**	**1**
3	WEEK	fr	**6**	**5**	**4**	**3**	**2**	**1**	**0**
4	DAY	fr	○	**20**	**10**	**8**	**4**	**2**	**1**
7	MIN Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
8	HOUR Alarm	**AE**	•	**20**	**10**	**8**	**4**	**2**	**1**
9	WEEK Alarm	**AE**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A	DAY Alarm	**AE**	•	**20**	**10**	**8**	**4**	**2**	**1**
E	Control Register 1	○	○	○	TI / TP	**AF**	TF	**AIE**	TIE

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 7 to A) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ Even when the alarm registers (Reg - 7 to A) are used as a RAM register, it is handled as the RTC's internal alarm setting, so when "0" is written to the AIE bit it prevents any alarms from occurring (when /AIRQ goes to low level) due to unintended matches between the write data and the time status.

1) Alarm registers (Reg - 7[h] ~ A[h])

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the AE bit.

Multiple "day" settings can be entered, such as "Monday, Wednesday, Friday, Saturday".

When the settings made in the alarm registers match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /AIRQ pin goes low.

∗1) To prevent an alarm from occurring for a certain item, write "1" to AE bit in that item's register. When AE = "1", the data for that item is ignored and is not used as a comparison target for the alarm function.
(Example) Write 80h (AE = "1") to the DAY Alarm register (Reg - A):
→ Only the hour, minute, and day settings are used as alarm comparison targets. The date setting is not used as an alarm comparison target.

∗2) If all four AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

2) AF bit (Alarm Flag)

This is a flag bit that retains the result when an alarm interrupt event has been detected.

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1".

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /AIRQ low output to be canceled (/AIRQ remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. ∗ Result is retained until this bit is cleared to zero.

3) AIE bit (Alarm IRQ Interrupt Enable)

This bit sets the operation of the /AIRQ interrupt signal when an alarm interrupt event occurs (when the TF bit value changes from "0" to "1").

Writing "1" to this bit causes a low-level interrupt signal to be output from the /AIRQ pin when an interrupt event occurs.
When a "0" is written to this bit, output from the /AIRQ pin is prohibited (disabled).

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/AIRQ status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/AIRQ status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/AIRQ status changes from Hi-Z to low).

∗ To detect occurrence of an alarm interrupt event without setting /AIRQ to low level, monitor the AF bit value (note when it changes from "0" to "1") while AIE = "0".

13.3.3. Examples of alarm settings

1) Basic information about alarm settings

- Four parameters can be set as alarm objects: minute, hour, day, and date.
- Hour settings are based on a 24-hour clock.
- Multiple day settings can be made at once.
- To exclude an item as an alarm object, write "1" to the AE bit in the corresponding register.
  ∗ When the AE bit = 1 for all objects (minute, hour, day, and date), an alarm interrupt event occurs once per minute.

2) Examples of alarm settings are listed below.

Examples of alarm settings	Reg - A	Reg - 9								Reg - 8	Reg - 7
	DAY Alarm	bit								HOUR Alarm	MIN Alarm
		7	6	5	4	3	2	1	0		
		AE	S	F	T	W	T	M	S		
• First day of each month, at 11:45 PM: [Date] Date 01 [Day] Ignored [Hour] 11:00 PM (23:00 when using 24-hour clock) [Minute] 45 minutes	01 h	1	X	X	X	X	X	X	X	23 h	45 h
• Monday to Saturday of each week, at 7:00 AM: [Date] Ignored [Day] Mon, Tues, Wed, Thu, Fri, Sat [Hour] 7:00 AM (07:00 when using 24-hour clock) [Minute] 00 minutes, or Ignored	80h to FFh AE = "1"	0	0	1	1	1	1	1	0	07 h	80h to FFh AE = "1"
• Every minute: [Date] Ignored [Day] Ignored [Hour] Ignored [Minute] Ignored	80h to FFh AE = "1"	1	X	X	X	X	X	X	X	80h to FFh AE = "1"	80h to FFh AE = "1"

X : don't care

∗ The register settings shown above are merely examples.
Various other settings can be made, depending on the desired operation.

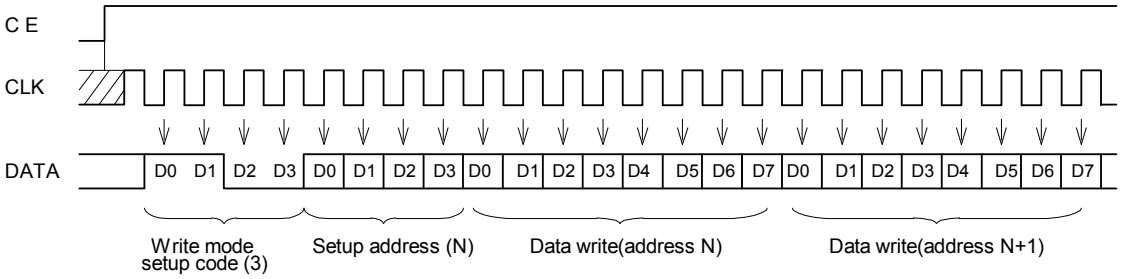
13.4. Read/Write of data

For both read and write, first set up chip condition (internally CE="H") to CE0="H" and CE1="H", then specify the 4-bits address, and finally read or write in 8-bits units.

Both read and write use LSB-first. In continuous operation, objected address is auto incremented.
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

13.4.1. Write of data

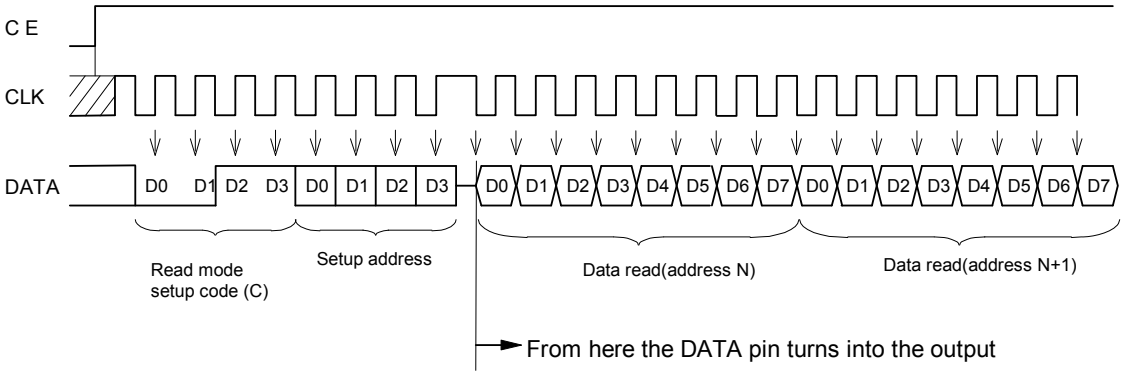
1) Take "3" as the write mode in the first four bits after the CE input rise, and set the address to write to the next four bits.
2) The next 8 bits of write data is written to the address set earlier, and the next 8 bits of data is written to the address which is automatically incremented from the last one.



* When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

13.4.2. Read of data

1) Take "C" as the read mode in the first four bits after the CE input rise, and set the address to read to the next four bits.
2) The next 8 bits of read data is read from the address set earlier, and the next 8 bits of data is read from the address which is automatically incremented from the last one.



13.4.3. Write/Read mode setup code.

Mode	Setup Code
Write	3 h
Read	C h

∗ In the mode setting code, if a value other than those listed above is used, the subsequent data will be ignored and the DATA pin remains in the input state.

EPSON TOYOCOM

Application Manual

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