ETM04E-02

EPSON TOYOCOM

# *Application Manual*

## Real Time Clock Module

# RTC-4701JE/NB

| Model | Product Number |
|---|---|
| RTC-4701JE | Q41470171000200 |
| RTC-4701NB | Q41470191000200 |

EPSON TOYOCOM CORPORATION

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  We apologize for the inconvenience, but we will eventually have a unified part numbering system for Epson Toyocom which will be user friendly.

CONTENTS

Serial RTC module with alarm and timer function

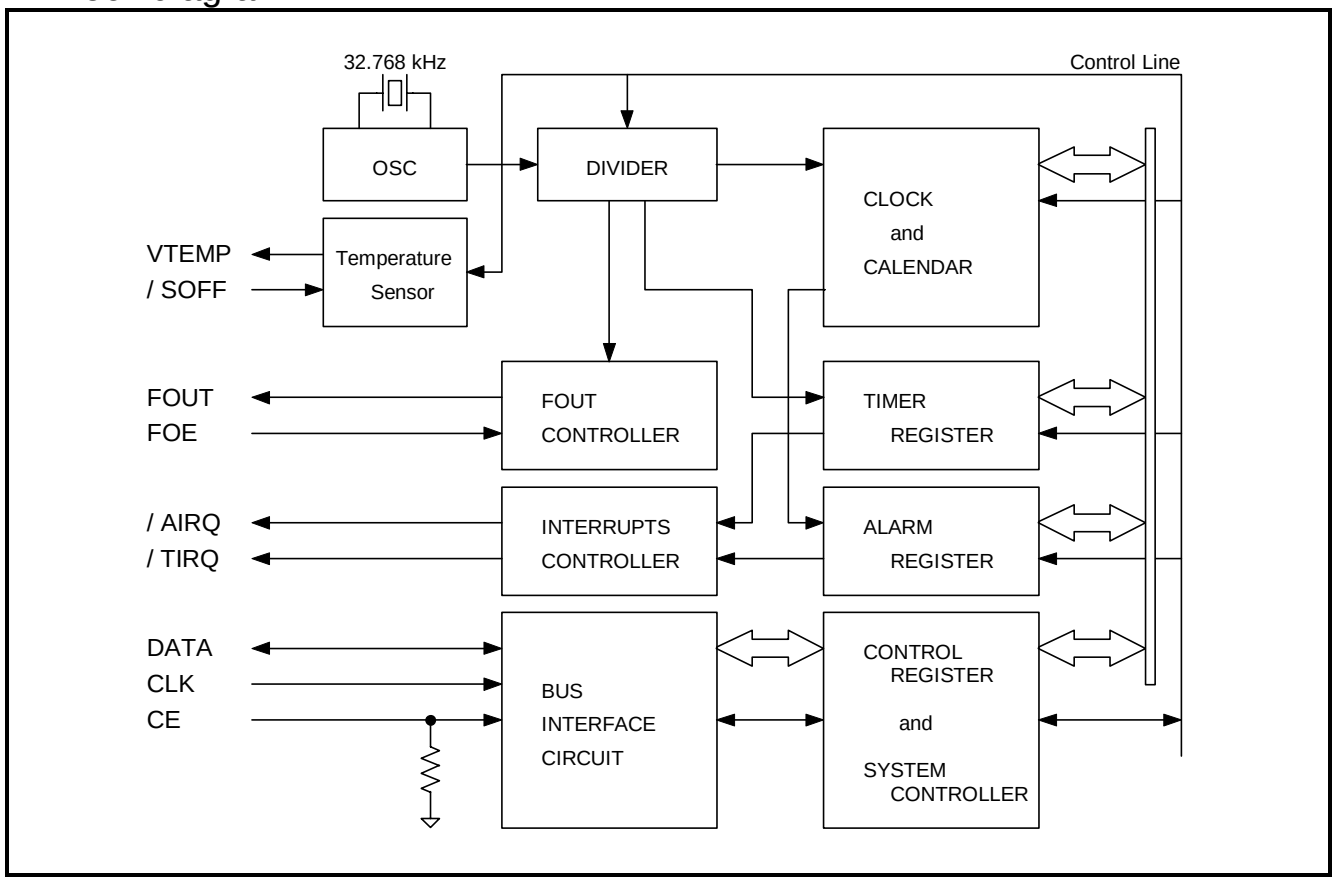
# RTC - 4701 JE/NB

- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Alarm interrupt function for day of week, day, hour, and minute
- Timer interrupt function which can be set up between 1/4096 second and 255 minutes
- OVF interrupt function based on 12-bit additional counter
- Ability to detect stopping of oscillation and time update
- Automatic adjustment for leap year
- Built-in temperature sensor ( voltage output : –7.6 mV / °C Typ.)
- Wide range of interface voltage between 1.6 V and 5.5 V
- Wide range of clock voltage between 1.6 V and 5.5 V
- Low power consumption at 0.5 μA / 3 V ( Typ.)
- Available as small package ( JE : VSOJ-20 pin , NB : SON-22pin )

## 1. Overview

This module is a serial interface real time clock that has a built-in crystal oscillator. The module offers many functions such as clock & calendar circuitry with automatic leap year adjustment (from seconds to year), additional counter, alarm, Timer interrupt, stopping of oscillation, and time update. In addition, it is equipped with a diode temperature sensor (analog voltage output).
The serial interface can be controlled by three signal lines, and it saves the port which a system uses most. Because it is available in small package SON(VSOJ) in high density mounting, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

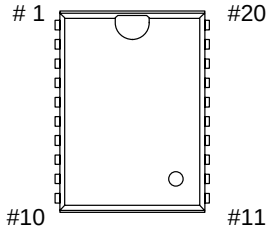
## 2. Block diagram



# 3. Terminal description

## 3.1. Terminal connections

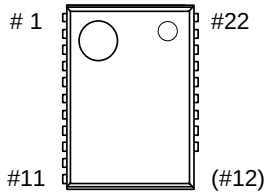
RTC - 4701 JE




| | | | |
|---|---|---|---|
| 1. | $V_{DD}$ | 20. | N.C. |
| 2. | FOUT | 19. | N.C. |
| 3. | CE | 18. | N.C. |
| 4. | / AIRQ | 17. | N.C. |
| 5. | / TIRQ | 16. | N.C. |
| 6. | CLK | 15. | N.C. |
| 7. | DATA | 14. | N.C. |
| 8. | FOE | 13. | N.C. |
| 9. | VTEMP | 12. | N.C. |
| 10. | / SOFF | 11. | GND |

VSOJ - 20 pin

RTC - 4701 NB




| | | | |
|---|---|---|---|
| 1. | GND | 22. | N.C. |
| 2. | / SOFF | 21. | N.C. |
| 3. | VTEMP | 20. | N.C. |
| 4. | FOE | 19. | N.C. |
| 5. | DATA | 18. | N.C. |
| 6. | CLK | 17. | N.C. |
| 7. | / TIRQ | 16. | N.C. |
| 8. | / AIRQ | 15. | N.C. |
| 9. | CE | 14. | N.C. |
| 10. | FOUT | (13) | – |
| 11. | $V_{DD}$ | (12) | – |

SON - 22 pin

## 3.2. Terminal functions

| Signal name | I / O | Signal description |
|---|---|---|
| CE | Input | This is a chip enabled input pin with the builit-in pull-down resistance.<br>When the CE pin is at the "H" level, access to this RTC becomes possible.<br>When the CE pin is at the "L" level, the DATA pin is at the high impedance level and the CLK and DATA pins cannot accept input. |
| CLK | Input | This is a shift clock input pin for serial data transmission. In the write mode, it takes in data from the DATA pin using the CLK signal rise edge. In the read mode, it outputs data from the DATA pin using the fall edge. |
| DATA | Bi-directional | This is a data input/output pin for serial data transmission. After the input rise of CE, by using the first 8-bit write data to set the write or read mode, this pin can be set as either input pin or output pin. |
| FOUT | Output | This pin outputs the clock signal of frequency. (32.768 kHz CMOS output). Depending on the FOE input pin, output from the FOUT pin can be prohibited. |
| FOE | Input | This is the input pin for the FOUT output control. When the FOE pin is at the "H" level, the FOUT pin goes into the output state; when it is at the "L" level, the FOUT pin is at the high impedance level. |
| VTEMP | Output | This is the voltage output pin for the temperature sensor (analog). |
| / SOFF | Input | This is the input pin for the temperature sensor control. When the /SOFF pin is at the "H" level and the SON bit is 1, the temperature sensor circuitry starts and outputs a voltage according to the temperature of the VTEMP pin. When the /SOFF pin is at the "L" level, the temperature sensor circuitry stops and the VTEMP pin is at the high impedance level. |
| / AIRQ | Output | This is an open drain output pin for alarm and additional counter interrupt. |
| / TIRQ | Output | This is an open drain output pin for Timer interrupt. |
| $V_{DD}$ | – | This pin connects to the plus side of the power. |
| GND | – | This pin connects to the minus side (ground) of the power. |
| N.C. | – | This pin is not connected internally.<br>But , In RTC-4701NB( SON-22pin ), all pins from 14 pin to 22 pin are connected with inside frame mutually.<br>Use OPEN, or GND or $V_{DD}$ to connect. |

* Be sure to connect a filter capacity of at least 0.1 µF close to $V_{DD}$ – GND.

## 4. Absolute maximum ratings

GND=0 V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power voltage | $V_{DD}$ | – | –0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | input pin | GND–0.3 to $V_{DD}$+0.3 | V |
| Output voltage 1 | $V_{OUT1}$ | /AIRQ , /TIRQ pins | GND–0.3 to +8.0 | V |
| Output voltage 2 | $V_{OUT2}$ | FOUT, DATA pins | GND–0.3 to $V_{DD}$+0.3 | V |
| Storage temperature | $T_{STG}$ | Stored bare product after unpacking | –55 to +125 | °C |

## 5. Recommended operating conditions

GND=0 V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power voltage | $V_{DD}$ | – | 1.6 to 5.5 | V |
| Clock voltage | $V_{CLK}$ | – | 1.6 to 5.5 | V |
| Operating temperature | $T_{OPR}$ | No condensation | –40 to +85 | °C |

## 6. Frequency characteristics

GND=0 V

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Frequency stability | $\Delta$ f / fo | Ta= +25 °C, $V_{DD}$=3.0 V | $5 \pm 23$ (*1) | $\times 10^{-6}$ |
| Oscillation start time | f / V | Ta= +25 °C, $V_{DD}$=1.6 V to 5.5 V | $\pm$ 2 Max. | $\times 10^{-6}$ / V |
| Frequency temperature characteristics | Top | Ta= –20 °C to +70 °C, $V_{DD}$= 3.0 V ; Reference at +25 °C | +10 / –120 | $\times 10^{-6}$ |
| Frequency voltage characteristics | tSTA | Ta= +25 °C, $V_{DD}$=3.0 V | 3 Max. | s |
| Aging | fa | Ta= +25 °C, $V_{DD}$=3.0 V ; first year | $\pm$ 5 Max. | $\times 10^{-6}$ / year |

*1) Equivalent to 1 minute of monthly deviation. ( excluding offset )

## 7. Electrical characteristics

∗ If not specifically indicated, GND=0 V, $V_{DD}$=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

### 7.1. DC electrical characteristics

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Current consumption (1) | $I_{DD1}$ | $V_{DD}$=5 V | CE, FOE, /SOFF = GND /AIRQ, /TIRQ = $V_{DD}$ 32.768 kHz output is OFF Sensor output is OFF | | 1.0 | 2.0 | µA |
| Current consumption (2) | $I_{DD2}$ | $V_{DD}$=3 V | | | 0.5 | 1.0 | µA |
| Current consumption (3) | $I_{DD3}$ | $V_{DD}$=5 V, CL= 0 pF | CE, /SOFF = GND FOE, /AIRQ, /TIRQ = $V_{DD}$ 32.768 kHz output is ON Sensor output is OFF | | 3.0 | 7.5 | µA |
| Current consumption (4) | $I_{DD4}$ | $V_{DD}$=3 V, CL= 0 pF | | | 1.7 | 4.5 | µA |
| Current consumption (5) | $I_{DD5}$ | $V_{DD}$=5 V, CL=30 pF | | | 8.0 | 20.0 | µA |
| Current consumption (6) | $I_{DD6}$ | $V_{DD}$=3 V, CL=30 pF | | | 5.0 | 12.0 | µA |
| Current consumption (7) | $I_{DD7}$ | $V_{DD}$=5 V | CE, FOE, = GND /SOFF, /AIRQ, /TIRQ = $V_{DD}$ 32.768 kHz output is OFF Sensor output is ON | | 50 | 75 | µA |
| Current consumption (8) | $I_{DD8}$ | $V_{DD}$=3 V | | | 40 | 60 | µA |
| Input voltage | $V_{IH}$ | Input pin | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IL}$ | | | 0 | | 0.2$V_{DD}$ | V |
| Input leakage current | $I_{LK}$ | Input Pin except CE, $V_{IN}$= $V_{DD}$ or GND | | –0.5 | | 0.5 | µA |
| Input resistance (1) | $R_{DWN1}$ | $V_{DD}$=5 V | CE pin $V_{IN}$=$V_{DD}$ | 75 | 150 | 300 | kΩ |
| Input resistance (2) | $R_{DWN2}$ | $V_{DD}$=3 V | | 150 | 300 | 600 | kΩ |
| Output voltage (1) | $V_{OH1}$ | $V_{DD}$=5 V, $I_{OH}$=–1 mA | DATA , FOUT pins | 4.5 | | 5.0 | V |
| | $V_{OH2}$ | $V_{DD}$=3 V, $I_{OH}$=–1 mA | | 2.0 | | 3.0 | V |
| | $V_{OH3}$ | $V_{DD}$=3 V, $I_{OH}$=–100 µA | | 2.9 | | 3.0 | V |
| Output voltage (2) | $V_{OL1}$ | $V_{DD}$=5 V, $I_{OL}$= 1 mA | DATA , FOUT pins | GND | | GND+0.5 | V |
| | $V_{OL2}$ | $V_{DD}$=3 V, $I_{OL}$= 1 mA | | GND | | GND+0.8 | V |
| | $V_{OL3}$ | $V_{DD}$=3 V, $I_{OL}$= 100 µA | | GND | | GND+0.1 | V |
| | $V_{OL4}$ | $V_{DD}$=5 V, $I_{OL}$= 1 mA | /AIRQ, /TIRQ pins | GND | | GND+0.25 | V |
| | $V_{OL5}$ | $V_{DD}$=3 V, $I_{OL}$= 1 mA | | GND | | GND+0.4 | V |
| Output leakage current | $I_{OZ}$ | Output pins other than VTEMP $V_{OUT}$= $V_{DD}$ or GND | | –0.5 | | 0.5 | µA |

## 7.2. Temperature sensor characteristics

∗ If not specifically indicated, GND=0 V, $V_{DD}$=1.6 V to 5.5 V , Ta= –40 °C to +85 °C

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Temperature output voltage | $V_{TEMP}$ | VTEMP pin, Ta=+25 °C, $V_{DD}$= 2.7 V to 5.5 V GND based output voltage | | 1.480 | | V |
| Output precision | $T_{ACR}$ | Ta=+25 °C , $V_{DD}$= 2.7 V to 5.5 V | | | ± 5.0 | °C |
| Temperature sensitivity (∗1) | $V_{SE}$ | –40 °C ≤ Ta ≤ +85 °C , $V_{DD}$= 2.7 V to 5.5 V | –7.1 | –7.6 | –8.1 | mV / °C |
| Linearity (∗2) | ΔNL | –40 °C ≤ Ta ≤ +85 °C , $V_{DD}$= 2.7 V to 5.5 V | | | ± 2.0 | % |
| Temperature detection range | $T_{SOP}$ | ΔNL ≤ ±2.0 % , $V_{DD}$= 2.7 V to 5.5 V | –40 | | + 85 | °C |
| Output resistance (∗3) | $R_O$ | VTEMP pin, Ta=+25 °C, $V_{DD}$= 2.7 V to 5.5 V GND standard and $V_{DD}$ standard | | 1.0 | 3.0 | kΩ |
| Load condition | $C_L$ | $V_{DD}$= 2.7 V to 5.5 V | | | 100 | pF |
| | $R_L$ | $V_{DD}$= 2.7 V to 5.5 V | 500 | | | kΩ |
| Response time | $t_{RSP}$ | $V_{DD}$= 3.0 V , $C_L$=100 pF , $R_L$=500 kΩ , within ±1 °C | | | 200 | µs |

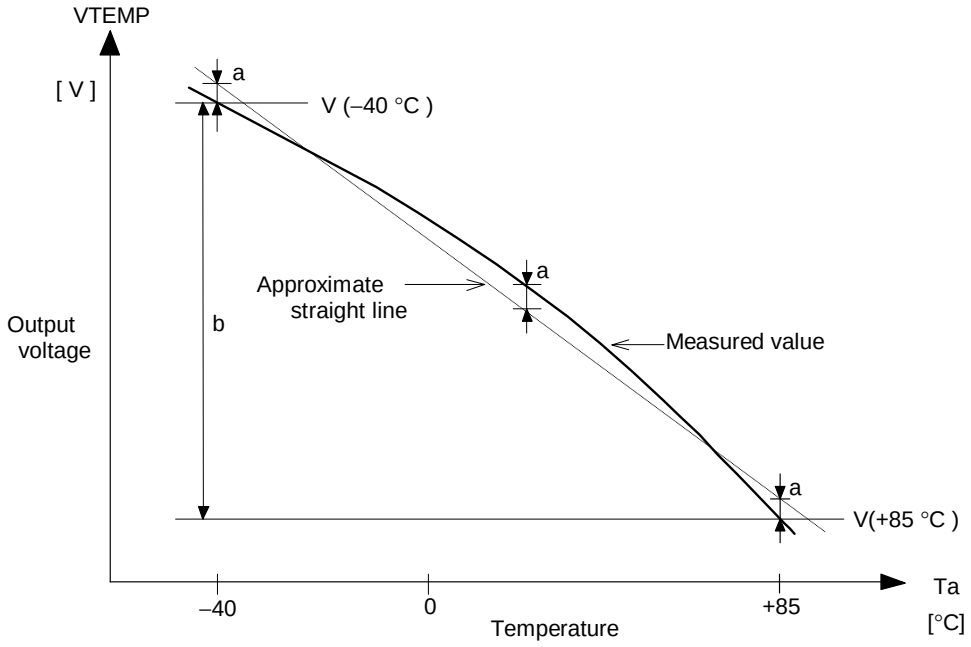
∗1) Temperature sensitivity $V_{SE}$ = ( V (+85 °C) – V (–40 °C) ) / 125 [ mV / °C ]

∗2) Linearity

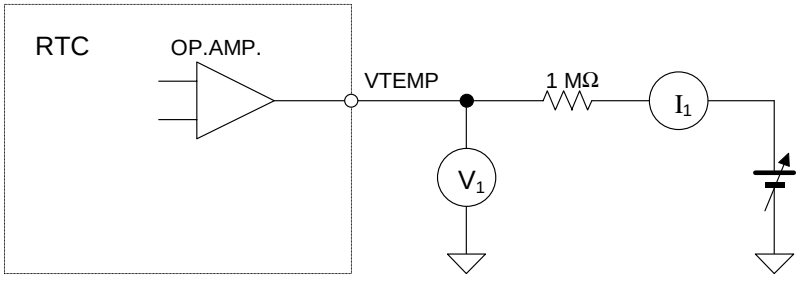
$$\Delta NL = \frac{a}{b} \times 100\ [\%]$$

a : Maximum deviation between the measured value of VTEMP and the approximate straight line

b : Difference between the measured values at -40 °C and +85 °C




∗3) Output resistance ( Ro ) $Ro = \frac{\Delta V_1}{\Delta I_1}$

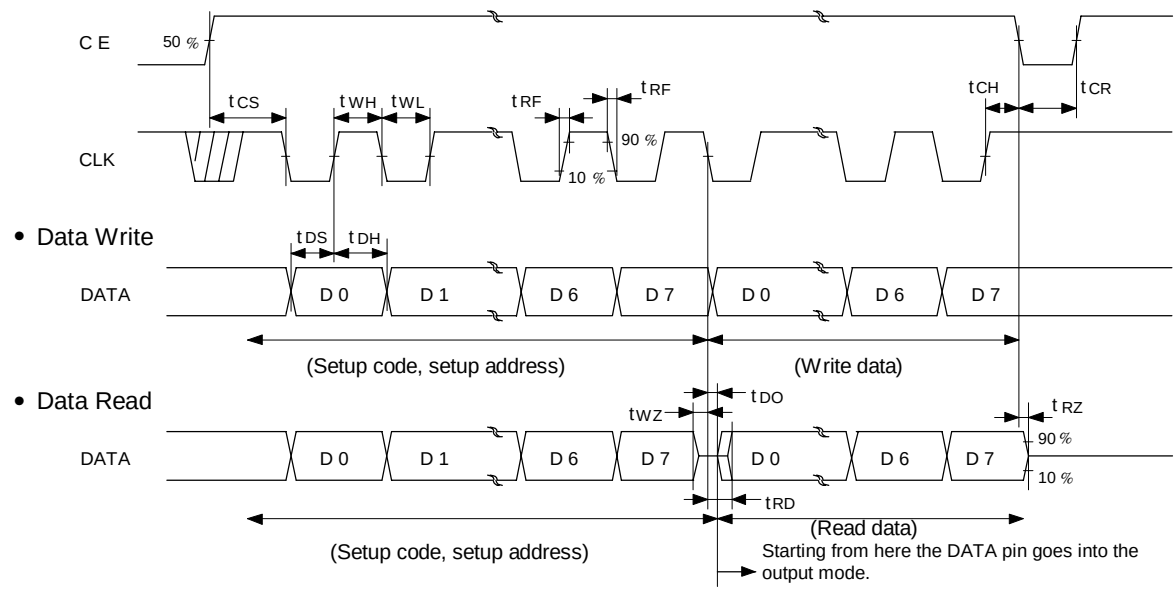


## 7.3. AC electrical characteristics

∗ If not specifically indicated, GND=0 V, Ta= –40 °C to +85 °C

| Parameter | Symbol | Condition | $V_{DD}$=3 V ± 10 % | | | $V_{DD}$=5 V ± 10 % | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| CLK clock cycle | $t_{CLK}$ | | 600 | | | 350 | | | ns |
| CLK H pulse width | $t_{WH}$ | | 300 | | | 175 | | | ns |
| CLK L pulse width | $t_{WL}$ | | 300 | | | 175 | | | ns |
| CE setup time | $t_{CS}$ | | 300 | | | 175 | | | ns |
| CE hold time | $t_{CH}$ | | 300 | | | 175 | | | ns |
| CE recovery time | $t_{CR}$ | | 400 | | | 300 | | | ns |
| Write data setup time | $t_{DS}$ | | 75 | | | 50 | | | ns |
| Write data hold time | $t_{DH}$ | | 75 | | | 50 | | | ns |
| Write data disable time | $t_{WZ}$ | | 0 | | | 0 | | | ns |
| Output mode switching time | $t_{DO}$ | | 0 | | | 0 | | | ns |
| Read data delay time | $t_{RD}$ | CL=50 pF | | | 300 | | | 120 | ns |
| Output disable time | $t_{RZ}$ | CL=50 pF<br>RL=10 kΩ | | | 200 | | | 100 | ns |
| Input rise/fall time | $t_{RF}$ | | | | 100 | | | 50 | ns |
| FOUT duty | tW / t | 50% $V_{DD}$ level | 40 | | 60 | 40 | | 60 | % |

Timing chart



# 8. How to use

## 8.1. Register table

Bank 0

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Read | Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | second | fos | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 1 | minute | fr | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | only bit 7 not permitted |
| 2 | hour | fr | ○ | 20 | 10 | 8 | 4 | 2 | 1 | permitted | |
| 3 | day of week | fr | 6 | 5 | 4 | 3 | 2 | 1 | 0 | permitted | |
| 4 | day | fr | ○ | 20 | 10 | 8 | 4 | 2 | 1 | permitted | |
| 5 | month | fr | C | ○ | 10 | 8 | 4 | 2 | 1 | permitted | |
| 6 | year | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 7 | minute alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 8 | hour alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 9 | day of week alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | permitted | permitted |
| A | day alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| B | – | – | – | – | – | – | – | – | – | – | – |
| C | Timer setup | TE | • | TD1 | TD0 | • | • | • | • | permitted | permitted |
| D | Timer counter | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | permitted | permitted |
| E | control 1 | ○ | ○ | ○ | TI/TP | AF | TF | AIE | TIE | permitted | permitted (note 3) |
| F | control 2 | ○ | TEST | STOP | RESET | HOLD | ○ | ○ | ○ | permitted | permitted (note 6) |

Bank 1

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Read | Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | second | fos | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 1 | minute | fr | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | only bit 7 not permitted |
| 2 | hour | fr | ○ | 20 | 10 | 8 | 4 | 2 | 1 | permitted | |
| 3 | day of week | fr | 6 | 5 | 4 | 3 | 2 | 1 | 0 | permitted | |
| 4 | day | fr | ○ | 20 | 10 | 8 | 4 | 2 | 1 | permitted | |
| 5 | month | fr | C | ○ | 10 | 8 | 4 | 2 | 1 | permitted | |
| 6 | year | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 7 | minute alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 8 | hour alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| 9 | day of week alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | permitted | permitted |
| A | day alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | permitted | permitted |
| B | additional counter 1 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | permitted | permitted |
| C | additional counter 2 | fr | AC1 | AC0 | OVF | 2048 | 1024 | 512 | 256 | permitted | only bit 7 not permitted |
| D | – | – | – | – | – | – | – | – | – | – | – |
| E | – | – | – | – | – | – | – | – | – | – | – |
| F | control 3 | FOES | TEST | – | – | – | ACIE | ACE | SON | permitted | permitted (note 6) |

Note 1. Registers 0A are the same in Bank 0 and, Bank 1.
Access to Bank 0 and Bank 1 are specified by the first 4 bits in the serial communication.

| Mode | Bank 0 | Bank 1 |
|---|---|---|
| Write | 3 h | 1 h |
| Read | C h | 8 h |

Note 2. At the initial power supply, the FOES, ACE, and SON bits are reset to 0. For the other bits, because their register values are not fixed, be sure to initialize them before use. During the initialization, do not use data other than date and time; otherwise there is no guarantee that the clock will operate.

Note 3. Write is possible only when the AF, TF, and OVF bits are 0.

Note 4. For bits indicated with " – ", write cannot be performed and the read-out value is not fixed. For bits indicated with " ○ ", after initialization use them at 0.

Note 5. For bits indicated with " • ", they can be used as memory.

Note 6. The TEST bit is reserved for testing work by EPSON. Be sure to it to 0 before use.

Note 7. When the Timer counter (Bank 0,Address D) is read, the data value preset previously can be read.

## 8.2. Register description

### 8.2.1. Clock and calendar registers ( Same in Bank 0 and Bank1 : Reg-0 to Reg-6 )

Data is in the BCD format. For example, if the second register is "0101 1001", this means 59 seconds. The time measurement uses the 24-hour format (fixed).

If the alarm interrupt is not used, registers 7 to A can be used as 7-bit memory register. In this case, be sure to set the AIE(Alarm Interrupt Enable) bit to 0 and forbid use of the alarm interrupt.

If the Timer interrupt is not used, register D can be used as an 8-bit memory register. In this case, be sure to set the TIE (Timer Interrupt Enable) bit to 0 and forbid use of the Timer interrupt.

- Year register and leap year, and year-digit carry bits

  If the year register's 2-digit BCD is divided by four and the remainder is 0, this year is determined as the leap year. This works automatically for both the Western calendar as well as the Japanese Heisei calendar. (Year 00 is taken as a leap year.)
  Also, for the year register, 99 is followed by 00. At this time, the year-digit carry bit C (bit 6 of register 5) is set to 1.

- Day of week register

  The day of week register makes use of the 7 bits from 0 to 6. The bits are assigned as shown in the following table. Be sure not to set multiple days of week to 1.

| bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Day of week |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | Sunday |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | Monday |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | Tuesday |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | Wednesday |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | Thursday |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | Friday |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | Saturday |

- fos ( OSC Flag )

  This flag is a bit for recording when the oscillation stops. This bit is used to detect when decrease in the power voltage causes the oscillation to stop. 1 indicates oscillation has stopped and this information is kept until 0 is written to it. This flag is not affected even when other bits (STOP, RESET) are 1.

- fr ( READ Flag )

  This flag is a bit which becomes 0 when the RTC is set to the non-selection state (CE input pin becomes "L"), or 1 when the RTC is set to the selection state (CE becomes "H") during which there is a 1 second digit increase. Because of this characteristic, it becomes possible to determine whether a 1 second digit increase has occurred during read-out of the clock register. If fr is 1, it becomes necessary to read all the clock registers again.

- C ( Year-digit Carry bit in register5.)

  When the year register advances from 99 to 00, if 0 is written to the value before the advance in year, this bit is set to 1. Even thought the year register of this RTC uses the lower 2 digits of the Western calendar, by looking at the year-digit carry bit, it becomes possible to handle the upper two digits of the Western calendar also.
  For example, the year-digit carry bit can be used to handle the four-digit year value in a way so that if it is 0, the upper two digits are considered as 19, or if it is 1 the upper two digits are considered as 20.

### 8.2.2. Alarm registers (Same in Bank 0 and Bank1: Reg-7 to Reg-A )

Alarm can be set to day of week, day, hour, or minute. Each of the respective alarm register has the AE bit (Alarm Enable bit) attached to bit 7. By taking advantage of this bit, the hourly alarm and daily alarm can easily be set up. The day of week alarm can be set to any multiple days of the week. When the AE bit is 0, the appropriate register and the clock register are compared; when the bit is 1, this means "don't care" and the data is ignored and the two are regarded as the same. When the alarm goes off, the AF (Alarm Flag) bit is set to 1; if at this moment the AIE (Alarm Interrupt Enable) bit is 1, the /AIRQ pin is set to the low level and the interrupt signal occurs. If the AIE bit is 0, the alarm interrupt output from the /AIRQ pin will be prohibited.

- The relationship between the day of week alarm bit and each day of the week is shown as follows:

| bit | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| Day of week | Saturday | Friday | Thursday | Wednesday | Tuesday | Monday | Sunday |

8.2.3. Timer counter and control register 1 ( Bank 0 : Reg-C to Reg-E )

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| C | TE | • | TD1 | TD0 | • | • | • | • |
| D | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| E | ○ | ○ | ○ | TI/TP | AF | TF | AIE | TIE |

This is the register for controlling the presettable down counter of the 8 bits used during the Timer interrupt. TD0 and TD1 of Reg-C specify the count cycle of the down counter (source clock), and Reg-D specifies the preset value (split cycle) of this down counter. When the TE bit becomes 0, the presettable counter loads the content of the Timer counter and stops the counting. When the TE bit becomes 1, counting starts. During a source clock cycle, the down counter continues the countdown and when the data becomes zero, the TF (Timer Flag) is set to 1. At this moment, if the TIE (Timer Interrupt Enable) bit of Reg-E is 1 the /TIRQ pin is set to the low level and the interrupt signal occurs. When the TIE bit of becomes 0, output from the /TIRQ pin is prohibited. Also, when the TI/TP bit is 1, it reloads the data of the Timer counter register and then starts the countdown again (a repeat operation). On the other hand, when the TE bit is 1, even if the Timer counter (Reg-D) is set with the 0 data, the Timer interrupt from the /TIRQ pin does not occur. In order to operate the Timer as planned, it is necessary to set up the TE, TI/TP and TIE bits.

- Timer interrupt and source clock selection

| TD1 | TD0 | Source clock |
|---|---|---|
| 0 | 0 | 4096 Hz |
| 0 | 1 | 64 Hz |
| 1 | 0 | Update in seconds |
| 1 | 1 | Update in minutes |

- Timer interrupt interval

| Timer counter setting value | Source clock | | | |
|---|---|---|---|---|
| | 4096 Hz | 64 Hz | Update in seconds | Update in minutes |
| 0 | – | – | – | – |
| 1 | 244.14 μs | 15.625 ms | 1 s | 1 min |
| 2 | 488.28 μs | 31.250 ms | 2 s | 2 min |
| 3 | 732.42 μs | 46.875 ms | 3 s | 3 min |
| • | • | • | • | • |
| • | • | • | • | • |
| • | • | • | • | • |
| 255 | 62.26 ms | 3.984 s | 255 s | 255 min |

- TE bit ( Timer Enable )

  When the TE bit is set to 1, the presettable counter starts the countdown. When this bit becomes 0, the presettable counter stops the countdown.

- TI / TP bit: ( Interrupt Signal Output Mode Select. Interrupt / Periodic )

  This bit sets up the output mode of the Timer interrupt signal.

| TI / TP | 0 | 1 |
|---|---|---|
| Function | Level interrupt mode<br>As soon as the Timer interrupt occurs, the /TIRQ pin becomes "L" and the TF bit becomes 1. The /TIRQ pin remains at "L" until 0 is written to the TF bit. (However TIE=1) | Repeat interrupt mode<br>As soon as the Timer interrupt occurs, the /TIRQ pin becomes "L" (however TIE=1) and the TF bit becomes 1. Then, the /TIRQ pin automatically returns to the high impedance level, and the TF bit remains at 1 until 0 is written to it. |

- AF and TF bits ( Alarm Flag , Timer Flag )

  When an alarm occurs the AF bit becomes 1, and the TF bit is set to 1 when the down counter for the Timer interrupt becomes zero. Data is kept until 0 is written to both bits. 1 cannot be written to both bits.

- AIE and TIE bits ( Alarm , Timer Interrupt Enable )

  These two bits determine whether to trigger each interrupt signal when the alarm and Timer interrupt events occur. The AIE bit controls the alarm interrupt and the TIE bit controls the Timer interrupt.

8.2.4. Control register 2 ( Bank 0 : Reg-F )

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| F | ○ | TEST | STOP | RESET | HOLD | ○ | ○ | ○ |

- TEST bit : this bit is reserved for testing work by EPSON.
  Be sure to always set this bit to 0. Be careful not to set this bit to 1 accidentally when writing to other bits of Reg-F. It can be cleared by setting the CE pin to "L".
- STOP bit
  When this bit is set to 1, the clock stops after 2 kHz of split cycle counter. When this bit becomes 0 the clock resumes. When you needs stop to the clock update, set " 1" to STOP bit and RESET bit both.
- RESET bit
  When this bit is set to 1, the counter between 2 kHz and 1 Hz is reset and the clock also stops. After 1 is written to this bit, this can be released by setting CE to "L". This bit is not influenced by states of the other bits. When you use this bit, and update stops, use STOP bit simultaneously.
- HOLD bit
  When this bit is set to 1, second digit increase is prohibited. If second digit increase happens while this bit is set to 1, when this bit returns to 0 the automatic compensation will work to correct by one unit. It is recommended that the HOLD bit be within one second.
- Function description table

| Bit | | | Function | | | |
|---|---|---|---|---|---|---|
| STOP | RESET | HOLD | Clock | Alarm | Timer counter | Additional counter |
| 0 | 0 | 0 | runs | runs | runs | runs ∗4 |
| 0 | 0 | 1 | ∗1 | stops | ∗2 | stops |
| 0 | 1 | 0 | stops | stops | ∗3 | stops |
| 0 | 1 | 1 | stops | stops | ∗3 | stops |
| 1 | 0 | 0 | stops | stops | ∗3 | stops |
| 1 | 0 | 1 | stops | stops | ∗3 | stops |
| 1 | 1 | 0 | stops | stops | ∗3 | stops |
| 1 | 1 | 1 | stops | stops | ∗3 | stops |

∗1 : If the deviation is within one second, the automatic compensation function will kick in to perform the automatic compensation.
∗2: Runs at source clock other than source clock for Timer interrupt at 1/60 Hz (1 min).
∗3: Runs only when the source clock for Timer interrupt is at 4096 Hz.
∗4: Runs only the ACE( Additional Counter Enable ) bit is 1.

8.2.5. Additional counter ( Bank1 : Reg-B,C )

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| B | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| C | fr | AC1 | AC0 | OVF | 2048 | 1024 | 512 | 256 |

This is a 12-bit presettable count-up counter. After the initial value is set, when the ACE (Additional Counter Enable) bit of control register 3 is set to 1, at the timing of the source clock selected at the AC0 and AC1 bits of Reg-C, count-up continues as long as the ACE bit is 1.

When the above Additional counter overflows (FFFh -> 000h), the OVF bit becomes 1. At this moment, if the ACIE (Additional Counter Interrupt Enable) bit of control register 3 has been set to 1, it is possible to trigger the additional counter overflow interrupt at the /AIRQ pin. As long as the count-up operation is not stopped by the register operation, the clock operation continues even if the RTC is in the non-selection state (during backup), and interrupt from this state can happen.

During data read of the additional counter, if the fr flag is 1, this indicates the counter has been updated during the read operation; therefore it is necessary to read the counter data again. Also, if 16 Hz is selected for the source clock, because the update timing cannot be caught at the fr flag when the counter is operating, an update check with data read at 2 times is required. However, while the counter is stopping, such data read at 2 times is not required.

By using the additional counter function, time lapse measurement, various cooking Timer operations of interrupt after n minutes, and long Timer can be made possible.

When you set data to this counter, set data to register B first.Set data to register C next.Set data to both register by all means.

- additional counter and source clock selection

| AC1 | AC0 | Source clock | Possible count range |
|---|---|---|---|
| 0 | 0 | 16 Hz | 0 to 255.93 seconds |
| 0 | 1 | Update in seconds | 0 to 4095 seconds |
| 1 | 0 | Update in minutes | 0 to 4095 minutes |
| 1 | 1 | Update in hours | 0 to 4095 hours |

8.2.6. Control register 3 ( Bank 1 : Reg-F )

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| F | FOES | TEST | – | – | – | ACIE | ACE | SON |

- FOES bit ( FOE Start Mode )

  When this bit is set to 1, the additional counter will not start at the time 1 is written to the ACE( Additional Counter Enable) bit of control register 3. With the ACE bit in 1, when the FOE input pin changes from the "H" level to the "L" level (fall edge), the additional counter will start.
  When the FOES bit is set to 0, the additional counter will start at the time the 1 is written to the ACE( Additional Counter Enable) bit of control register 3. When the power is supplied initially, this bit is reset to 0.

- ACIE bit ( Additional Counter Interrupt Enable )

  This bit determines whether the interrupt signal should be generated from the /AIRQ pin when the overflow interrupt event of the additional counter occurs. When the ACIE bit is 1, the interrupt signal is generated.

- ACE bit ( Additional Counter Enable )

  When this bit is set to 1, the additional counter starts the count-up. When this bit is set to 0, the additional counter stops the count-up. When the power is supplied initially, this bit is reset to 0.

- SON bit ( Sensor ON )

  When this bit is 1 and, furthermore, the /SOFF pin is at the "H" level, the builit-in temperature sensor circuitry starts and the analog voltage is output from the VTEMP pin according to the temperature. When this bit is 0, the temperature sensor circuitry stops and the VTEMP pin is at the high impedance level. When the power is supplied initially, this bit is reset to 0.

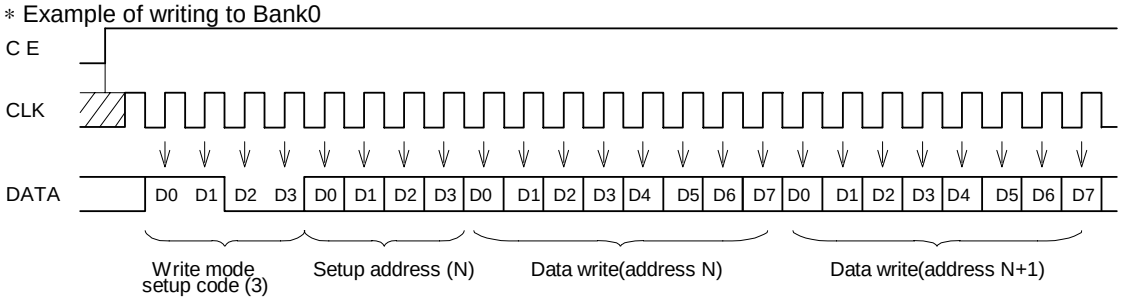
## 8.3. Read/write of data

After read/write and the CE input rise, the 4-bit mode is set up and then the 4-bit address is specified. Then, data read/write in units of 8 bits is performed. If input of unit of 8-bit data is not finished before the CE input falls, the 8-bit write data will be ignored at the time CE input falls. (The previous data is undetermined.) Both read and write use LSB-First.
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

### 8.3.1. Write of data

1) Take 3 or 1 as the write mode in the first four bits after the CE input rise, and set the address to write to the next four bits.
2) The next 8 bits of write data is written to the address set earlier, and the next 8 bits of data is written to the address which is automatically incremented from the last one.

∗ Example of writing to Bank0

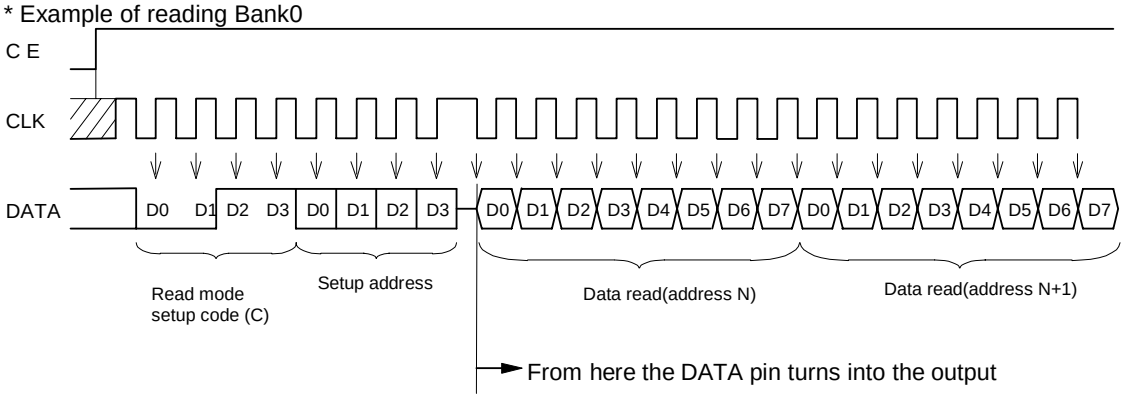



* When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

### 8.3.2. Read of data

1) Take "C" or 8 as the read mode in the first four bits after the CE input rise, and set the address to read to the next four bits.
2) The next 8 bits of read data is read from the address set earlier, and the next 8 bits of data is read from the address which is automatically incremented from the last one.

* Example of reading Bank0




### 8.3.3. Write/Read mode setup code of bank 0 and bank 1

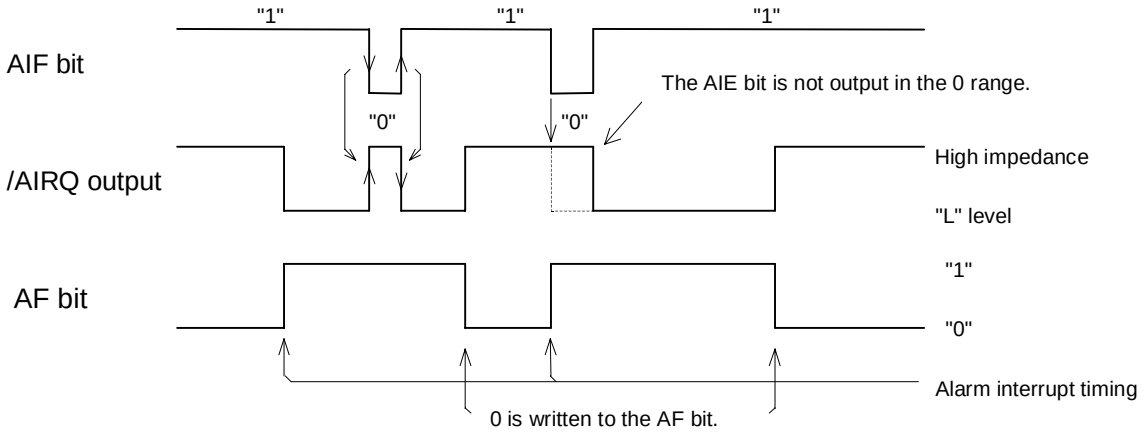
| Mode | Bank 0 | Bank 1 |
|---|---|---|
| Write | 3 h | 1 h |
| Read | C h | 8 h |

∗ In the mode setting code, if a value other than those listed above is used, the subsequent data will be ignored and the DATA pin remains in the input state.

## 8.4. Alarm interrupt / Timer interrupt

### 8.4.1. Alarm interrupt

When the alarm matches and AIE=1, the /AIRQ pin outputs "L"; when AIE=0, the /AIRQ pin is at the high impedance level. The alarm interrupt is output when "carry" from the 10-second digit to minute digit occurs




- How to use it

  The day of week, day, hour, and minute can be set. For day of week, multiple days can be set at a time. To avoid unintended hardware interrupt during the alarm setup, it is recommended that initially both the AF bit and AIE bit be set to 0. Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize the alarm circuitry with certainty. Afterwards, set the AIE bit to 1. If no hardware interrupt is desired to be used, set the AIE bit to 0, and monitor the AF bit with software as required.

- Usage example

  1 ) Set the alarm to go off at 6 PM tomorrow
  - · Write 0 to the AIE bit and the AF bit.
  - · Write 1 to the AE bit of the day alarm.
  - · Get the current day of week stored in register 3 in the day of week alarm register, left shift the data by 1 bit and then perform the write operation. (Be careful with the fr bit. If bit 6 is 1 (Saturday), write 01h (Sunday).)
  - · Write 18h to the hour alarm register.
  - · Write 00h to the minute alarm register.
  - · Apply zero clear to the AF bit.
  - · Write 1 to the AIE bit.

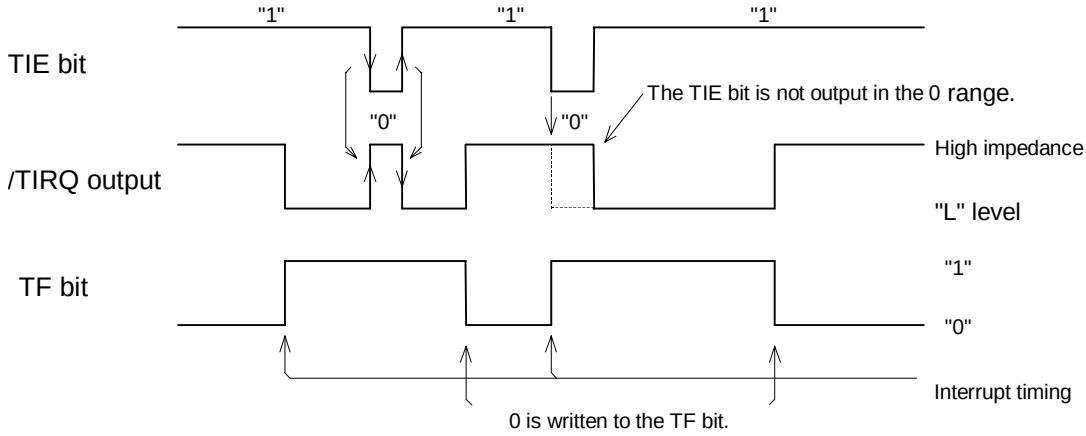
  2 ) Set the alarm to go off at 6 am everyday except Saturday and Sunday
  - · Write 0 to the AIE bit and the AF bit.
  - · Write 1 to the AE bit of the day alarm.
  - · Write 3Eh to the day of week alarm register.
  - · Write 06h to the hour alarm register.
  - · Write 00h to the minute alarm register.
  - · Apply zero clear to the AF bit.
  - · Write 1 to the AIE bit.

8.4.2. Timer interrupt

By setting the TI/TP bit, it is possible to select the level interrupt mode as well as the repeat interrupt mode.

( 1 ) Level interrupt mode ( TI/TP = 0 )

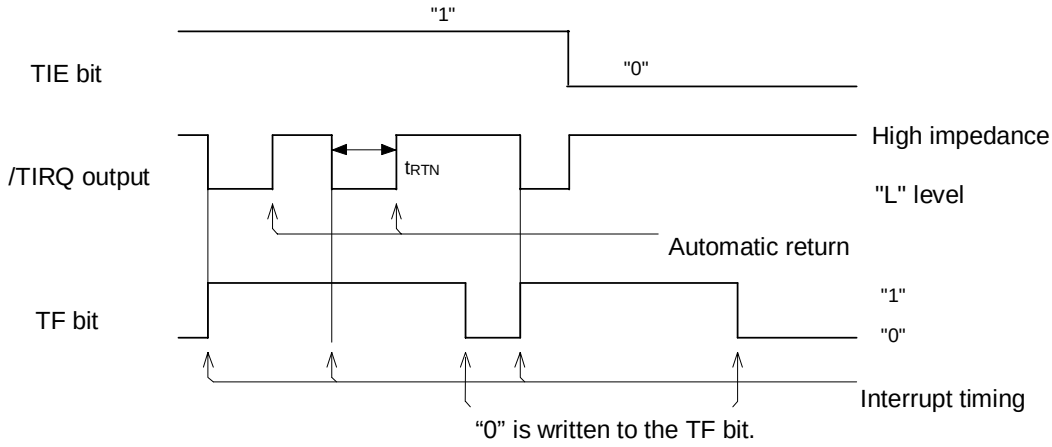
If TIE=1 when interrupt occurs, the /TIRQ pin becomes "L" output; if TIE=0, the /TIRQ pin enters the high impedance state.




( 2 ) Repeat interrupt mode ( TI/TP = 1 )

When interrupt occurs, if TIE = 1, the /TIRQ pin outputs "L"

When interrupt occurs, if TIE= 0, the /TIRQ pin remains at the high impedance level; only the TF bit becomes "1" and stays that way.




- Automatic return

  The automatic return time (tRTN) in the repeat interrupt mode is determined by the source clock specified at Reg-C.

| Source clock | Automatic return time (tRTN) |
|---|---|
| 4069 Hz | 0.122 ms |
| 64 Hz | 7.81 ms |
| Update in seconds | 7.81 ms |
| Update in minutes | 7.81 ms |

- Timer measurement error

  Because the Timer error is the $^{+0}/_{-1}$ cycle time of the selected source clock, the Timer's set time falls into the following range:

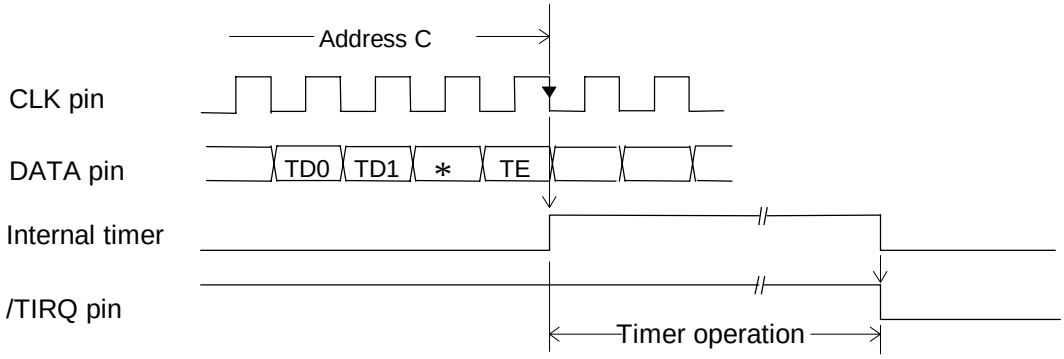
  ( Timer's set time - source clock cycle ) to ( Timer's set time )

  * Timer's set time = source clock cycle x value of the split cycle of Reg-D

  Also, the actual time of the Timer is the above time, plus the communication duration of the serial data transfer clock

- Timer start timing

  In the data write mode, the Timer starts counting from the fall edge of the CLK for the TE bit in the following time chart.




- How to use

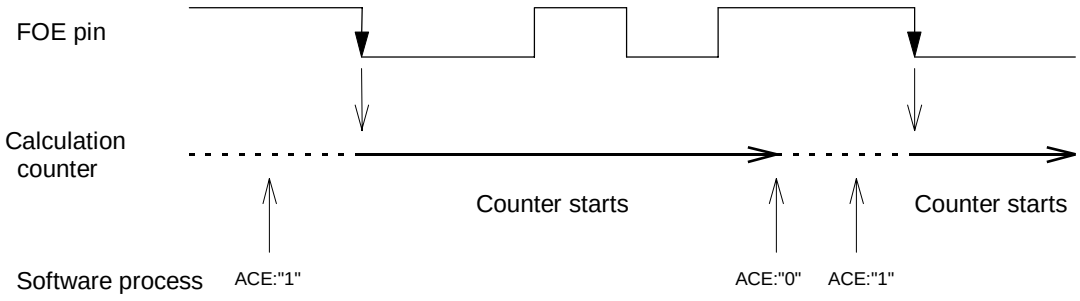
  At the cycle (source clock) specified at the Timer interrupt setup register, countdown starts from the value of the Timer counter register. When the data becomes zero, the /TIRQ pin becomes "L" and interrupt occurs.

  It can be used as an interval Timer between a minimum of 1/4096 second to a maximum of 255 minutes. To avoid unintended hardware interrupt during the Timer setup, it is recommended that initially both the TF bit and the TIE bit be set to 0.

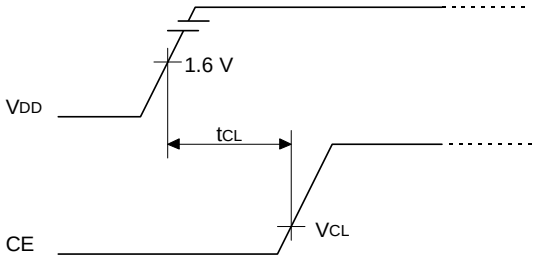
  If no regular interrupt is desired to be used, set the TIE bit to 0, and monitor the TF bit with software as required.

## 8.5. FOE start function

When the FOES(FOE Start Mode) bit of control register 3 is set to 1, the additional counter function triggered by FOE starts. While this mode is selected, the additional counter does not starts when 1 is written to the ACE (Additional Counter Enable) bit of control register 3.
With the ACE bit being 1, the additional counter starts when the FOE input pin changes from the "H" level to the "L" level (fall edge). After the additional counter starts, regardless of the state of the FOE pin, as long as it is not stopped by the register operation (ACE bit being 0), it will continue even if RTC is in the non-selected state. When the power is supplied initially, the FOES bit is reset to 0.



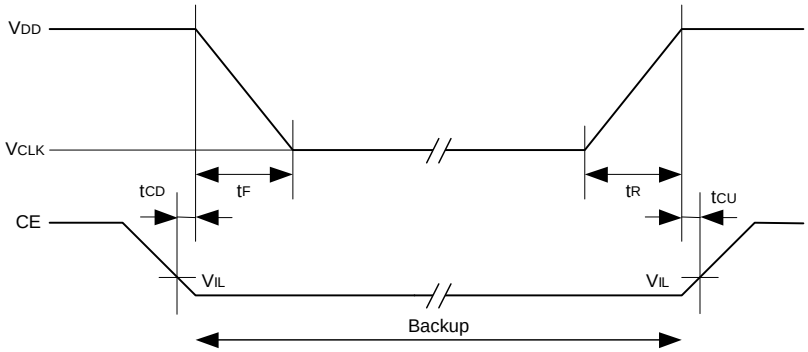
## 8.6. VDD and CE timing




* When the power is turned to ON, use with CE = "L" ( VCL[V] in the diagram ) as illustrated in the following timing chart.

| Item | Symbol | Remark | Specification | Unit |
|---|---|---|---|---|
| CE voltage when power is turned to ON | VCL | CE impressed voltage until VDD= 1.6 V | 0.3 (Max.) | V |
| CE=VCL [V] time when power is turned to ON | tCL | Time to maintain CE=VCL [V] until VDD= 1.6 V | 10 (Min.) | µs |

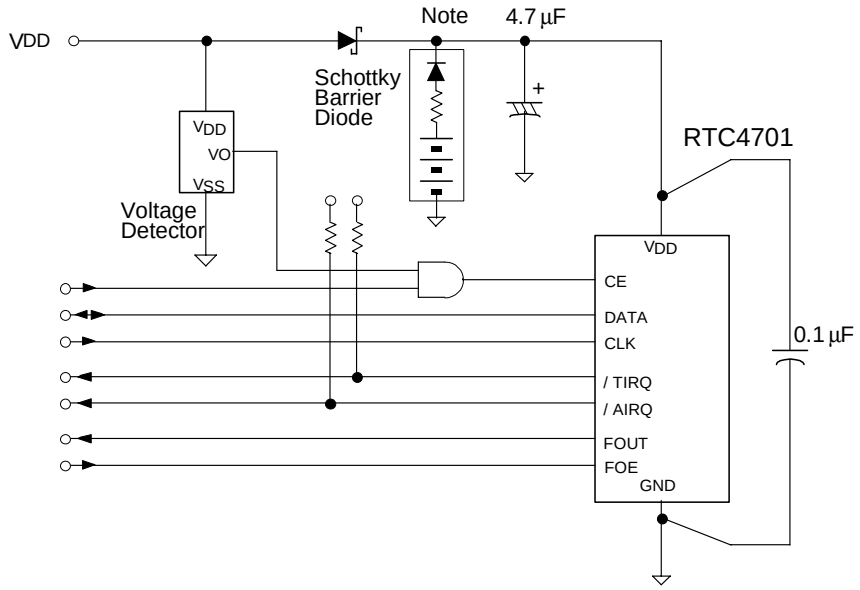
## 8.7. Power Down / power Up Timing.




| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CE time before power drop | tCD | – | 0 | | | µs |
| Power drop time | tF | – | 2 | | | µs / V |
| Power rise time | tR | – | 1 | | | µs / V |
| CE time after power rise | tCU | – | 0 | | | µs |

* When main power souce input to VDD from backup condition, CE should be definitely LOW

## 8.8. External connection example



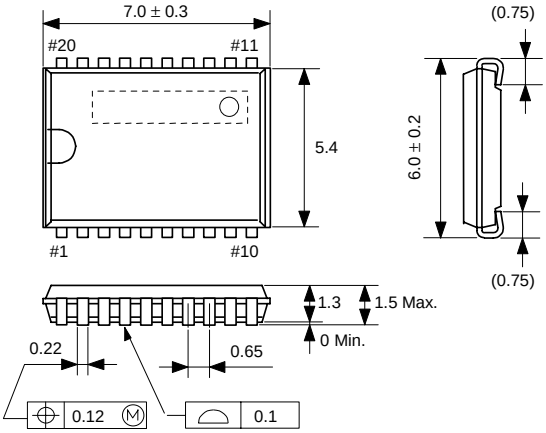

Note :
It uses the secondary battery or a lithium battery. When using the secondary battery, the diode is not required.
When using the lithium battery, the diode is required.
For detailed value on the resistance, please consult a battery manufacturer.

# 9. External dimensions / Marking layout

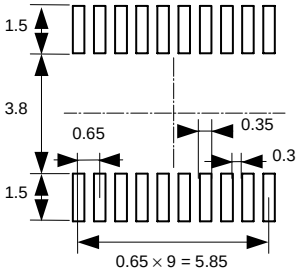
## 9.1. External dimensions

### RTC - 4701 JE ( VSOJ-20pin )

• External dimensions




• Recommended soldering pattern

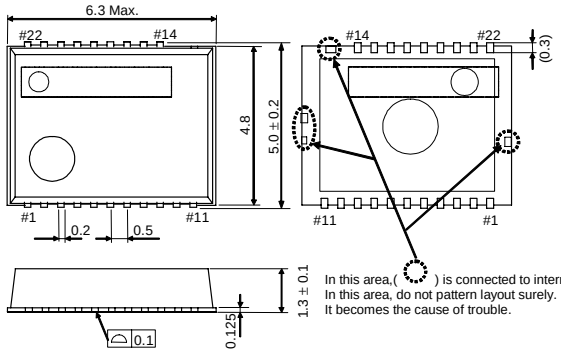



Unit : mm

* The cylinder of the crystal oscillator can be seen in this area ( back and front ), but it has no affect on the performance of the device.

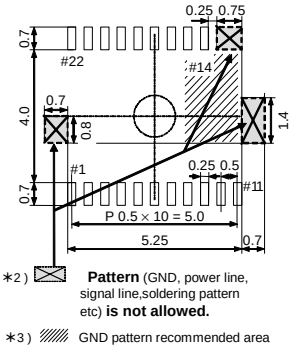
### RTC - 4701 NB ( SON-22pin )

• External dimensions




• Soldering pattern

Unit : mm



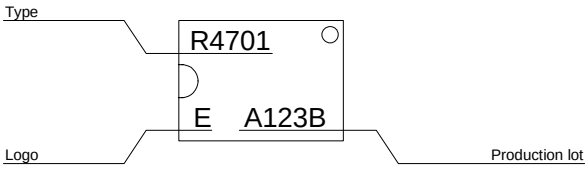

∗1) The cylinder of the crystal oscillator may be exposed in this area ( top and bottom ), however it has no affect on the performance of the device.

∗2) Pattern (GND, power line, signal line, soldering pattern, etc) is not allowed.
In this area, at a parts side of board, do not pattern layout surely.
∗ In an area ( ) of the product bottom side, a terminal connected to an IC inside is exposed.
When the circuit pattern contacts those terminal, it will cause serious obstruction to the oscillation, function or electronic spec.

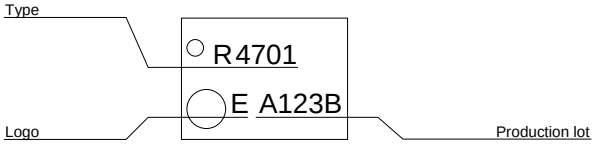
∗3) It is the best design that there is no signal line in this area. Please fill it up with GND pattern if possible.

## 9.2. Marking layout

### RTC - 4701 JE ( VSOJ-20pin )




### RTC - 4701 NB ( SON-22pin )



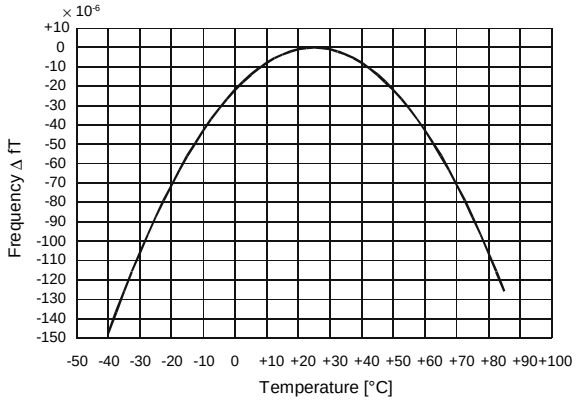

∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

# 10. Reference data

(1) Example of frequency and temperature characteristics

$\theta T$ = +25 °C Typ.

$\alpha$ = –0.035 × $10^{-6}$ / $°C^2$ Typ.




[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta fT = \alpha ( \theta T - \theta X )^2$

| | | |
|---|---|---|
| $\Delta fT$ | | : Frequency deviation in any temperature |
| $\alpha$ | ( 1 / $°C^2$ ) | : Coefficient of secondary temperature ( –0.035 ± 0.005 ) × $10^{-6}$ / $°C^2$ |
| $\theta T$ | ( °C ) | : Ultimate temperature (+25 ± 5 °C) |
| $\theta X$ | ( °C ) | : Any temperature |

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta fT + \Delta fV$

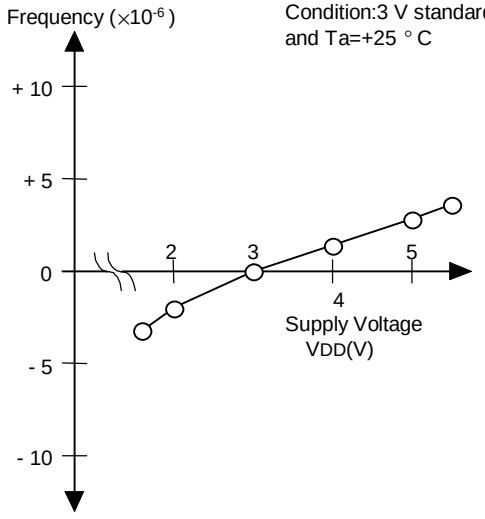
| | |
|---|---|
| $\Delta f/f$ | : Clock accuracy (stable frequency) in any temperature and voltage. |
| $\Delta f/fo$ | : Frequency precision |
| $\Delta fT$ | : Frequency deviation in any temperature. |
| $\Delta fV$ | : Frequency deviation in any voltage. |

3. How to find the date difference

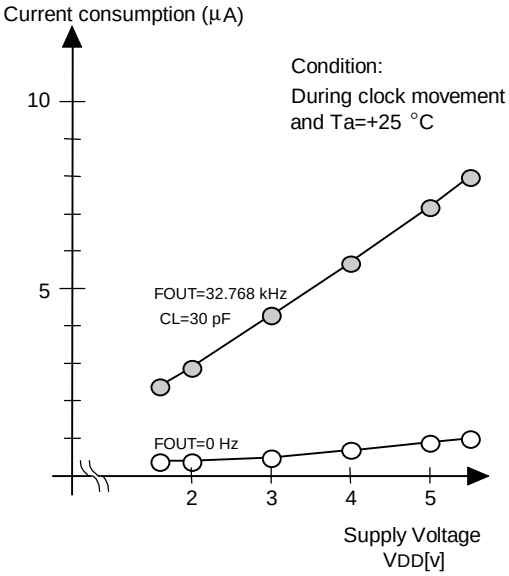
Date Difference = $\Delta f/f$ × 86400(s)

* For example: $\Delta f/f$ = 11.574 × $10^{-6}$ is an error of approximately 1 second/day.

(2) Example of the frequency/voltage characteristics




(3) Example of the current consumption/voltage characteristics



# 11. Application notes

## 1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1F as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

## 2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

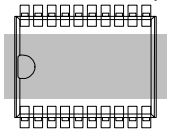
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

RTC - 4701 JE ( VSOJ-20pin )



RTC - 4701 NB ( SON-22pin )

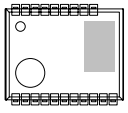
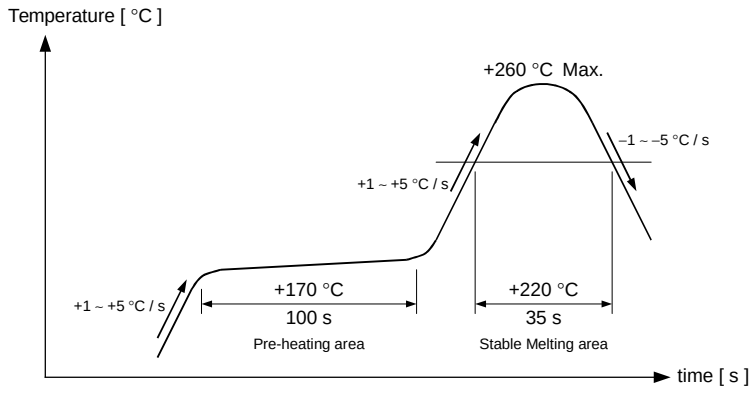


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.




∗ In addition, please confirm the Notes of an individual specification.

EPSON TOYOCOM

# Application Manual

## AMERICA


**EPSON ELECTRONICS AMERICA, INC.**

| | |
|---|---|
| HEADQUARTER | 150 River Oaks Parkway, San Jose, CA 95134, U.S.A.<br>Phone: (1)800-228-3964 (Toll free) : (1)408-922-0200 (Main)<br>Fax: (1)408-922-0238<br>http://www.eea.epson.com |
| Atlanta Office | One Crown Center 1895 Phoenix Blvd. Suite 348 Atlanta,GA 30349<br>Phone: (1)800-228-3964 (Toll free) : (1)770-907-7667 (Main) |
| Boston Office | 301Edgewater Place, Ste. 120, Wakefield, MA 01880, U.S.A.<br>Phone: (1)800-922-7667 (Toll free) : (1)781-246-3600 (Main)<br>Fax: (1)781-246-5443 |
| Chicago Office | 101 Virginia St., Ste. 290, Crystal Lake, IL 60014, U.S.A.<br>Phone: (1)800-853-3588 (Toll free) : (1)815-455-7630 (Main)<br>Fax: (1)815-455-7633 |
| El Segundo Office | 1960 E. Grand Ave., 2nd Floor, El Segundo, CA 90245, U.S.A.<br>Phone: (1)800-249-7730 (Toll free) : (1)310-955-5300 (Main)<br>Fax: (1)310-955-5400 |


## EUROPE


**EPSON EUROPE ELECTRONICS GmbH**

| | |
|---|---|
| HEADQUARTER | Riesstrasse 15, 80992 Munich, Germany<br>Phone: (49)-(0)89-14005-0 Fax: (49)-(0)89-14005-110<br>http://www.epson-electronics.de |
| Düsseldorf Branch Office | Altstadtstrasse 176, 51379 Leverkusen, Germany<br>Phone: (49)-(0)2171-5045-0 Fax: (49)-(0)2171-5045-10 |
| UK & Ireland Branch Office | Unit 2.4, Doncastle House, Doncastle Road, Bracknell,Berkshire RG12 8PE, England<br>Phone: (44)-(0)1344-381700 Fax: (44)-(0)1344-381701 |
| French Branch Office | LP 915 Les Conquérants, 1 Avenue de l' Atlantique, Z.A. de Courtaboeuf 2<br>91976 Les Ulis Cedex, France<br>Phone: (33)-(0)1-64862350 Fax: (33)-(0)1-64862355 |


## ASIA


**EPSON (CHINA) CO., LTD.**
23F, Beijing Silver Tower 2# North RD DongSangHuan ChaoYang District, Beijing, China
Phone: (86) 10-6410-6655 Fax: (86) 10-6410-7319
http://www.epson.com.cn

Shinghai Branch: High-Tech Building,900 Yishan Road Shanghai 200233,China
Phone: (86) 21-5423-5577 Fax: (86) 21-5423-4677

**EPSON HONG KONG LTD.**
20/F., Harbour Centre, 25 Harbour Road, Wanchai,Hong kong
Phone: (852) 2585-4600 Fax: (852) 2827-2152
http://www.epson.com.hk

**EPSON ELECTRONIC TECHNOLOGY DEVELOPMENT (SHENZHEN )CO., LTD.**
12/F, Dawning Mansion,#12 Keji South Road, Hi-Tech Park,Shenzhen, China
Phone: (86) 755-26993828 Fax: (86) 755-26993838

**EPSON TAIWAN TECHNOLOGY & TRADING LTD.**
14F, No.7, Song Ren Road, Taipei 110
Phone: (886) 2-8786-6688 Fax: (886)2-8786-6660
http://www.epson.com.tw

**EPSON SINGAPORE PTE. LTD.**
No 1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633.
Tel: (65)- 6-586-5500 Fax: (65) 6-271-3182
http://www.epson.com.sg

**SEIKO EPSON CORPORATION KOREA Office**
50F, KLI 63 Building,60 Yoido-dong, Youngdeungpo-Ku, Seoul, 150-763, Korea
Phone: (82) 2-784-6027 Fax: (82) 2-767-3677
http://www.epson-device.co.kr

Gumi Branch Office: 2F, Grand Bldg,457-4, Songjeong-dong Gumi-City,Gyongsangbuk-Do,
730-090, Korea
Phone: (82) 54-454-6027 Fax: (82) 54-454-6093


EPSON TOYOCOM CORPORATION

**Distributor**

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