High-stability Gyro Sensor: XV7021BB

Features

- Excellent bias temperature coefficient 0.0016 (°/s)/°C Typ.
- Low angle random walk 0.065 °/√h Typ.
- SPI/I²C serial interface
- Integrated user-selectable digital filter
- Notch filter for detuning frequency
- Angular rate output (16 or 24 bits resolution)
- Embedded temperature sensor
- Wide supply voltage range 2.7 to 3.6 V
- Low power consumption 900 µA Typ.
- Rate range ±400 °/s

Applications

- Anti-vibration, attitude control for industrial applications
- Autonomous machines
- Robotics control
- Optical image stabilization
- Motion detection for human machine interface

Typical Performance

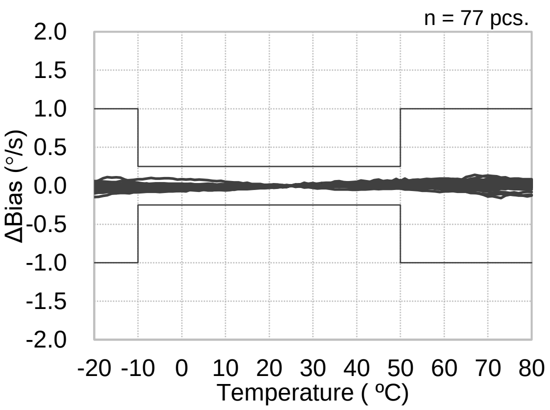


Figure. Bias Variation over Temperature

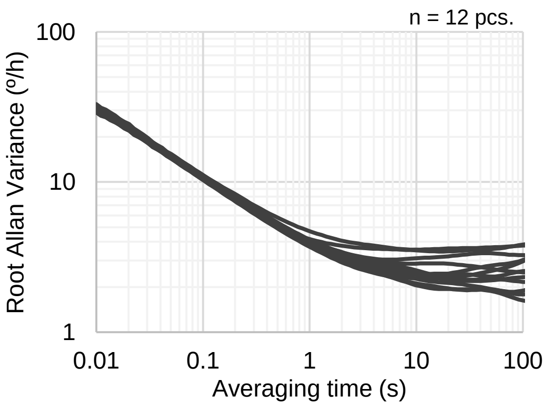


Figure. Allan Variance

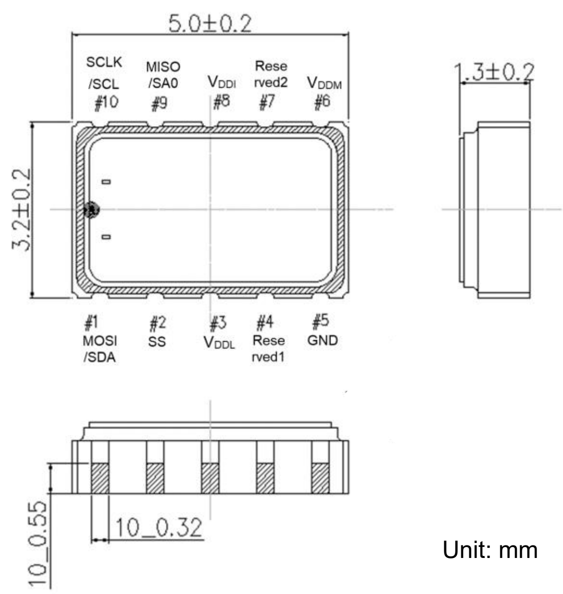
Description

The XV7021BB has superior performance characteristics especially with bias output stability and low noise while consumption less than 1 mA of current. Epson achieves these performances by using Epson's original quartz sensor element.

This sensor has digital output interface (SPI and I²C) that is compatible with various interface logic levels enabled by interface power supply voltage settings (V_{DDI}) that are independent of the main power supply voltage (V_{DDM}).

User-selectable low-pass filters and high-pass filters are available for wide range of cut-off frequencies. Additionally, a notch filter for detuning frequency is available exclusively for XV7021BB. The XV7021BB is suitable for various applications from consumer electronics such as wearable devices to industrial equipment.

Outline Drawing and Terminal Assignment



Unit: mm

Figure. Outline Dimensions

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Revision History

Rev. No.	Date	Page	Description
1.0	Mar. 15th, 2021		New release.
1.1	July 12th, 2024	All P.8 P.14 P.57	-Change the font size -order guide add the 53kHz product -3.5 Gyro Sensor characteristics Add the Frequency code L (53kHz) specification in the Bias variation over temperature A -Correct each address

Ordering Information

Available product codes are shown in a following table. The product codes are selected depending on number of axes to be detected in customer's system. If the system needs to be integrated with several gyro sensors, for example IMU (Inertial Measurement Units), mechanical or electrical coupling between their drive frequencies may affect system performance. It is therefore recommended to use combination of different drive frequencies as shown in the following table.

Table. Select of the Product Code

Number of axis	Product code	Product name	Serial interface	Slave device address
1 axis	- Please contact us	XV7021BB 49.600kHz F	4-wire SPI, 3-wire SPI, I^2C	-
2 axes	X2A0003110031	XV7021BB 49.600kHz C	4-wire SPI with multi-slave function -Global angular rate read operation is not available. Refer to Section 6.5.2.	01
	X2A0003110032	XV7021BB 51.000kHz D		10
3 axes	X2A0003110031	XV7021BB 49.600kHz C	4-wire SPI with multi-slave function	01
	X2A0003110032	XV7021BB 51.000kHz D		10
	X2A0003110033	XV7021BB 53.600kHz E		11

Product name: XV7021BB **.***kHz *
① ② ③

① Model code, ② Frequency, ③ Custom recognition

The product code can be identified by a marking on the product. Please refer to Section 4.3 Marking Description for the marking.

Symbols

	• **A lead-free product.**
	• **Compliant with the EU RoHS directive.** * About products without the Pb-Free label Product terminals are lead-free but the internal components of the product contain lead (high melting point solder lead as well as the lead contained in the glass of an electronic component are both not applicable under the EU RoHS directive).
	• **Indicates a product intended for use in an automobile (body, information systems, etc.). The product has been designed and manufactured in accordance with a quality assurance program suited for the on-board environment of an automobile.**
	• **Indicates a product intended for use to further the safe operation of an automobile (driving, stopping, turning). The product has been designed and manufactured in accordance with a quality assurance program suited for the on-board safety of an automobile.**

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1. Block Diagram

The block diagram of the sensor is shown in Figure 1.1 and Figure 1.2.

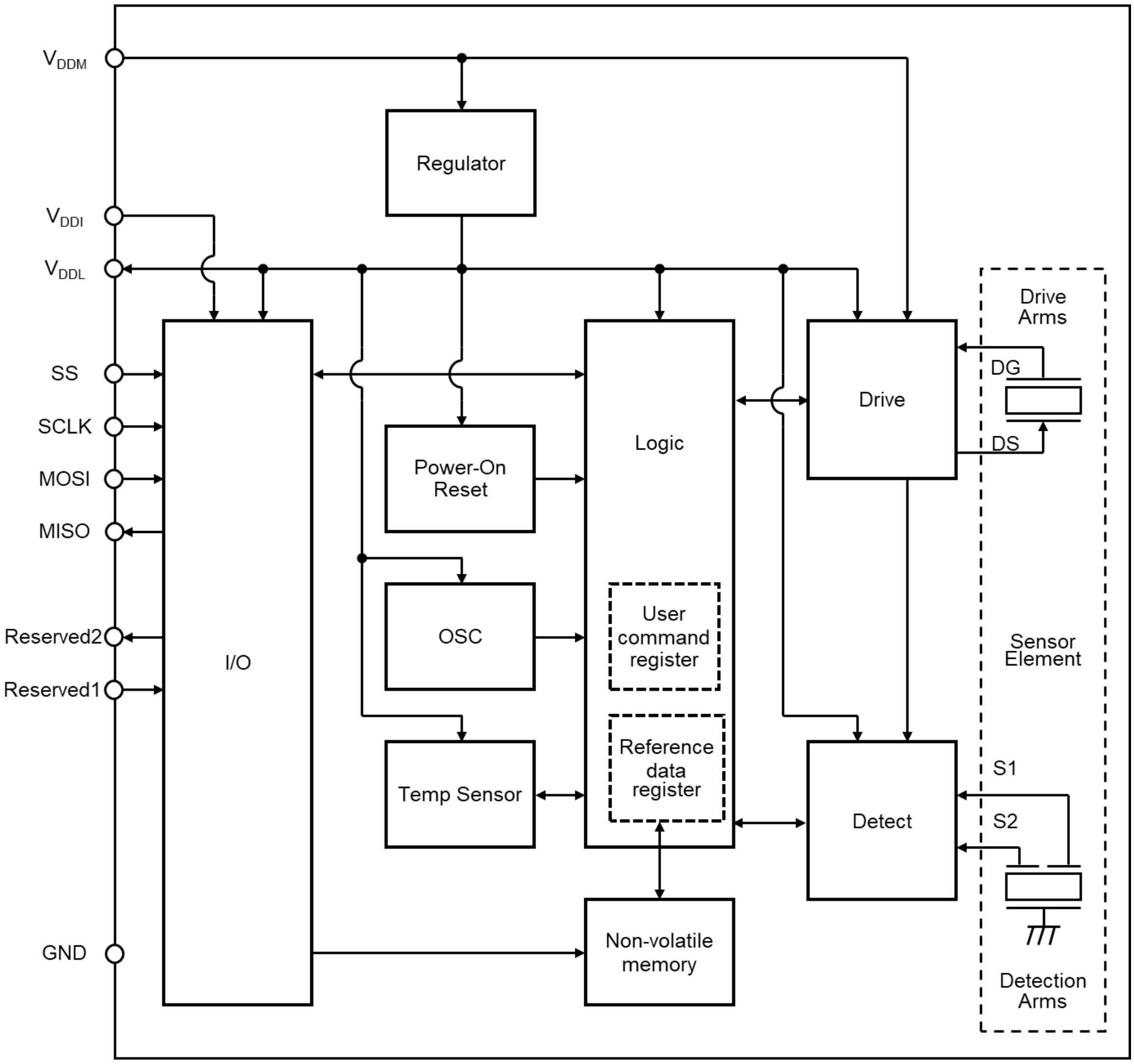


Figure 1.1. Functional Block Diagram

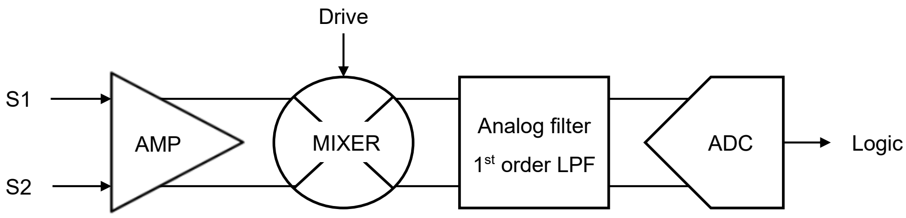


Figure 1.2. Block Diagram of Detecting Part

2. Functional Explanation

2.1. Detecting Axis and Output Polarity

This product detects an angular rate of a rotational movement. The correlation between a detecting axis of the angular rate and an output polarity is shown in Figure 2.1.

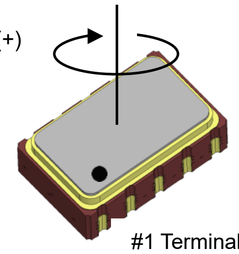


Figure 2.1. Detecting Axis and Output Polarity

2.2. Interface

This product is compatible with SPI (4-wire, 3-wire) and I^2C. Available only in SPI 4-wire mode expansion function, this sensor includes a multi-slave function for use in systems that detect two or more axes at once. This makes it possible to reduce I/O ports and board circuity. This sensor allows for interface power supply voltage settings (V_{DDI}) that are independent of the power supply voltage (V_{DDM}) to enable communications with interfaces of various logic levels. The multi-slave function is available only through factory settings implemented by Epson.

2.3. Angular Rate Output

The angular rate output data is provided in a 2's compliment format. 16 bits or 24 bits can be selected from the register settings. The AD converter sampling frequency f_s is 13.770 kHz at frequency code H, L and 14.160 kHz at frequency code J. The angular rate output data can also be provided after processing through the low-pass filter (LPF) or the high-pass filter (HPF). In addition, the notch-filter (NF) is available and can be enabled to suppress residual output of detuning frequency after mechanical shock.

Sampling frequency: The sampling frequency can be selected from the following options:
f_s =13.770 kHz (frequency code H, L), f_s=14.160 kHz (frequency code J)
(f_s, f_s/2, f_s/4, f_s/8, f_s/16, f_s/32, f_s/64, f_s/128 kHz)

LPF: This is a 2nd, 3rd or 4th order filter, the cutoff frequency can be selected from the following 14 stages.
(10, 35, 45, 50, 70, 85, 100, 140, 175, 200, 285, 345, 400, 500 Hz)

HPF: This is a 1st order filter. When enabled, the cutoff frequency can be selected from the following 7 stages.
(0.01, 0.03, 0.1, 0.3, 1, 3, 10 Hz)

NF: Either enable or disable can be selected. The center frequency of the notch filter is already set at our factory individually.

2.4. Temperature Sensor Output

Temperature output data is provided in a 2's compliment format. 8 bits, 10 bits or 12 bits can be selected from the register settings.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	V_{DDM}	-0.3	-	+4.0	V	GND = 0 V
Supply voltage for interface	V_{DDI}	-0.3	-	+4.0	V	GND = 0 V
Storage temperature	T_{STG}	-40	-	+85	ºC	
Condition for soldering	-	+350 ºC, 3 s			-	

3.2. Operating Conditions

Table 3.2. Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	V_{DDM}	+2.7	-	+3.6	V	GND = 0 V
Supply voltage for interface	V_{DDI}	+1.65	-	+3.6	V	GND = 0 V
Operating temperature	T_{OPR}	-20	-	+80	ºC	
Supply voltage start up time	t_{Pu}	0.01	-	100	ms	V_{DDM} 0 % to 90 %
4-wire SPI clock frequency	f_{SCLK}	-	-	10	MHz	V_{DDI} > +2.4 V
4-wire SPI clock frequency	f_{SCLK}	-	-	5	MHz	V_{DDI} ≤ +2.4 V
3-wire SPI clock frequency	f_{SCLK}	-	-	5	MHz	
I^2C clock frequency	f_{SCL}	-	-	400	kHz	
Sampling frequency	f_s	-	13.770	-	kHz	Frequency code: H, L
		-	14.160	-	kHz	Frequency code: J

(Note) Using the drive frequency integral multiplier as communications clock may result in fluctuations in the angular rate output.

(Note) Acquiring angular rate data as a frequency that is a fraction of the integer for the drive frequency can result in fluctuations in the angular rate output.

3.3. DC Characteristics

Table 3.3. DC Characteristics

V_{DDM} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Logic input voltage	V_{IH}	V_{DDI} × 0.7	-	-	V	
	V_{IL}	-	-	V_{DDI} × 0.3	V	
Logic output voltage	V_{OH}	V_{DDI} - 0.4	-	-	V	V_{DDI} = Min., Load = +1 mA
	V_{OL}	-	-	+0.4	V	V_{DDI} = Min., Load = -1 mA

3.4. Operating Sequence at Start-Up

Table 3.4. Operating Sequence at Start-Up

V_{DDM} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial communication wait time	t_{IF}	-	1	-	-	ms
Temperature sensor data read start time	t_{TSEN}	-	-	-	80	ms
Start-up time	t_{STA}	Output code ±1 °/s	-	-	200	ms

(Note) Conduct serial communication after t_{IF}.

(Note) Conduct temperature sensor data acquisition after t_{TSEN}.

(Note) Conduct angular rate data acquisition after t_{STA}.

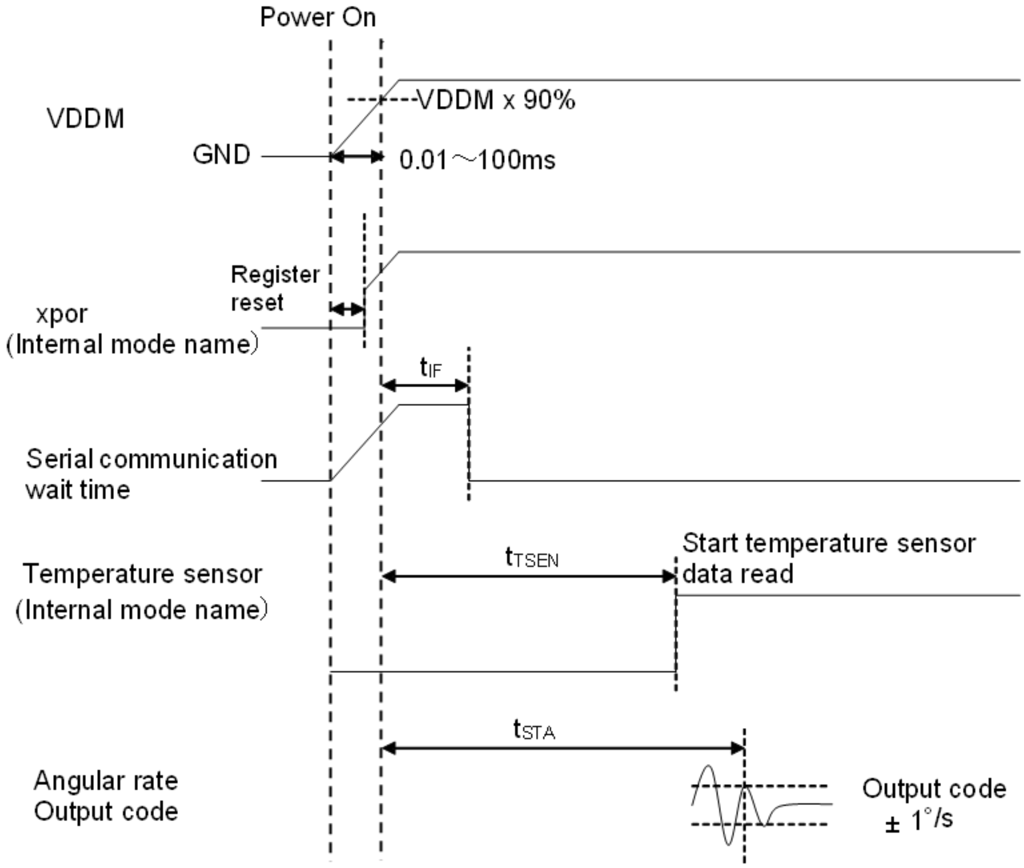


Figure 3.1. Operating Sequence at Start-Up

3.5. Gyro Sensor Characteristics

Table 3.5. Gyro Sensor Characteristics

Unless otherwise specified, V_{DDM} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drive frequency	F_d	Frequency code: H	49.000	49.575	50.150	kHz
		Frequency code: J	50.450	51.025	51.600	kHz
		Frequency code: L	52.900	53.550	54.200	kHz
Detuning frequency	D_f		0.7	0.9	1.1	kHz
Scale factor	S_o	16 bits	-	70	-	LSB/(°/s)
		24 bits	-	17920	-	
Scale factor tolerance	S_p	T_a = +25 ºC	-2	-	+2	%
Scale factor variation over temperature	S_{pt}	V_{DDM} = 3 V, T_a = +25 ºC reference	-3	-	+3	%
Bias	ZRL	T_a = +25 ºC	-	0	-	LSB
Bias tolerance	ZRL	T_a = +25 ºC	-1	-	+1	°/s
Bias variation over temperature A	ZRL_{ta}	V_{DDM} = 3 V, T_a = +25 ºC reference, T_a = -10 ~ +50 °C [Frequency code: H (49.575kHz, Frequency code: J (51.025kHz)]	-0.25	-	+0.25	°/s
		V_{DDM} = 3 V, T_a = +25 ºC reference, T_a = -10 ~ +50 °C [Frequency code: L (53.550kHz)]	-0.45	-	+0.45	°/s
Bias variation over temperature B	ZRL_{tb}	V_{DDM} = 3 V, T_a = +25 ºC reference T_a = -20 ~ +80 °C	-1	-	+1	°/s
Bias temperature coefficient	ZRL_s	V_{DDM} = 3 V, Average of absolute value, ΔT = 1 ºC	-	0.0016	-	(°/s)/ºC
Rate range	I		-400	-	+400	°/s
Non-linearity	NI	T_a = +25 ºC	-0.5	-	+0.5	%FS
Cross-axis sensitivity	CS	T_a = +25 ºC	-5	-	+5	%
Current consumption	I_{op1}		-	900	1300	μA
Standby current	I_{op2}		-	160	340	μA
Sleep current	I_{op3}		-	3	25	μA
Noise density	N_d	@ 10 Hz, LPF default setting	-	0.0015	-	(°/s)/√Hz
Angle random walk	N		-	0.065	-	°/√h

3.6. Temperature Sensor Characteristics

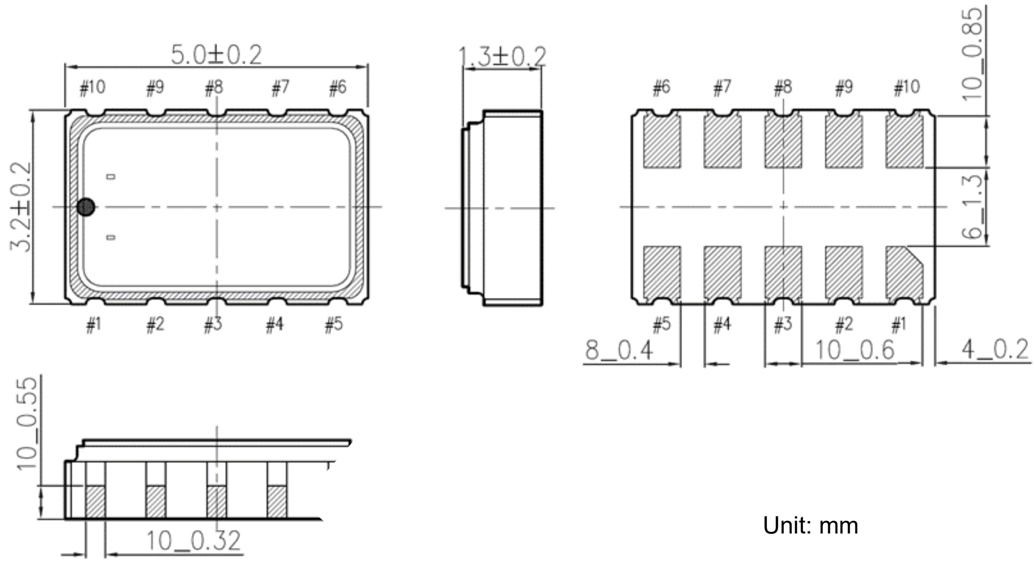
Table 3.6. Temperature Sensor Characteristics

Unless otherwise specified, V_{DDM} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output code	T_{out}	8 bits mode, T_a = +25 ºC	20	25	30	LSB
		10 bits mode, T_a = +25 ºC	80	100	120	
		12 bits mode, T_a = +25 ºC	320	400	480	
Temperature output accuracy	T_{acc}	T_a = +25 ºC	-5	-	+5	ºC
Temperature coefficient	T_{sen}	8 bits mode	0.9	1.0	1.1	LSB/ºC
		10 bits mode	3.6	4.0	4.4	
		12 bits mode	14.4	16.0	17.6	

4. Dimensions and Pin Description

4.1. Outline Dimensions



Unit: mm

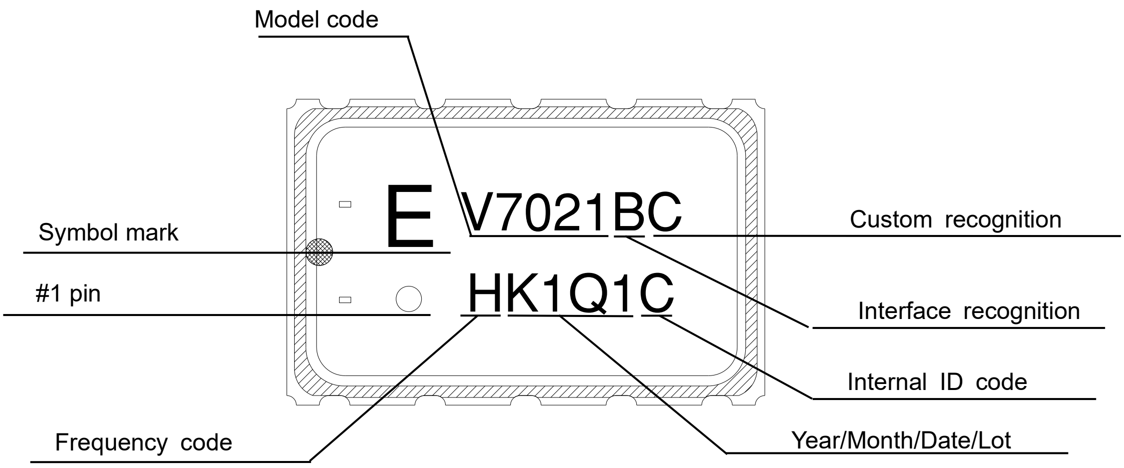
Figure 4.1. Outline Dimensions

4.2. Pin Name and Description

Table 4.1. Pin Name and Description

Pin number.	Pin name	Input/Output	Pin description
#1	MOSI/SDA	Input/Output	4-wire SPI communications mode: serial data input 3-wire SPI communications mode: serial data input/output I^2C communications mode: serial data input/output
#2	SS	Input	4-wire SPI communications mode: slave select 3-wire SPI communications mode: slave select I^2C communications mode: connect to V_{DDI}.
#3	V_{DDL}	Output	Internal regulator voltage output Connect to the bypass capacitor 1μF.
#4	Reserved1	Input	Connect to GND.
#5	GND	-	GND
#6	V_{DDM}	-	Power supply voltage
#7	Reserved2	Output	Logic "L" level output Do not connect.
#8	V_{DDI}	-	Power supply voltage for digital interface
#9	MISO/SA0	Input/Output	4-wire SPI communications mode: serial data output 3-wire SPI communications mode: Do not connect. I^2C communications mode: select lowest bit of slave address. Default status set to pull down (approx. 100 kΩ).
#10	SCLK/SCL	Input	Serial clock (4-wire, 3-wire and I^2C)

4.3. Marking Description



Frequency code	Drive frequency	Custom recognition	Slave address
H	49.600 kHz	C	01
J	51.000 kHz	D	10
L	53.600 kHz	E	11

Figure 4.2. Marking Description

4.4. Pin Equivalent Circuits

An equivalent circuit for SS, SCLK, MOSI, MISO and Reserved2 is shown in Figure 4.3.

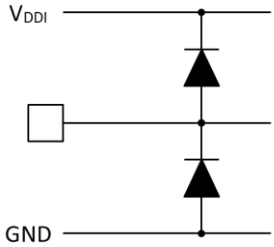


Figure 4.3. The Equivalent Circuit: SS, SCLK, MISO and Reserved2

An equivalent circuit for V_{DDL} and Reserved1 is shown in Figure 4.4.

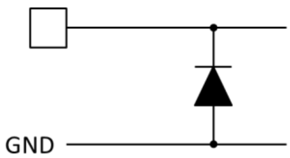


Figure 4.4. The Equivalent Circuit: V_{DDL} and Reserved1

An equivalent circuit for V_{DDM} and V_{DDI} is shown in Figure 4.5.

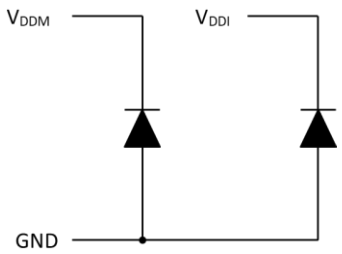


Figure 4.5. The Equivalent Circuit: V_{DDM} and V_{DDI}

4.5. Soldering Pattern

An example of a recommended soldering pattern for this product is shown in Figure 4.6. During actual board design, give due consideration to design aspects such as mounting density and solder mount reliability to ensure optimal design.

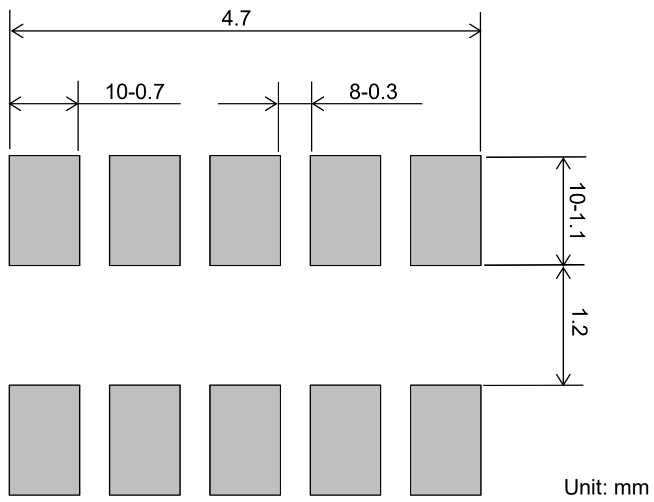


Figure 4.6. The Recommended Soldering Pattern

5. Typical Performance Characteristics

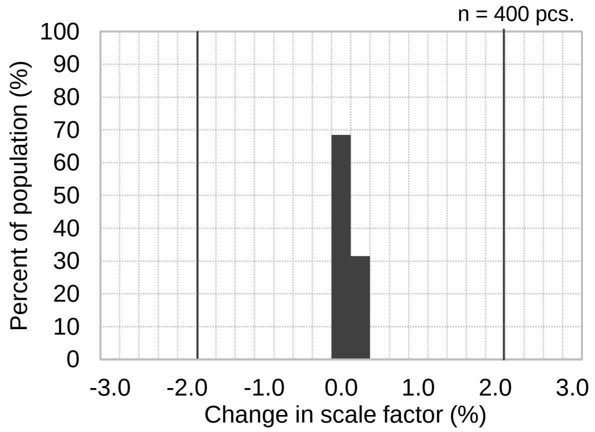


Figure 5.1. Scale Factor Tolerance at T_a = +25 ºC

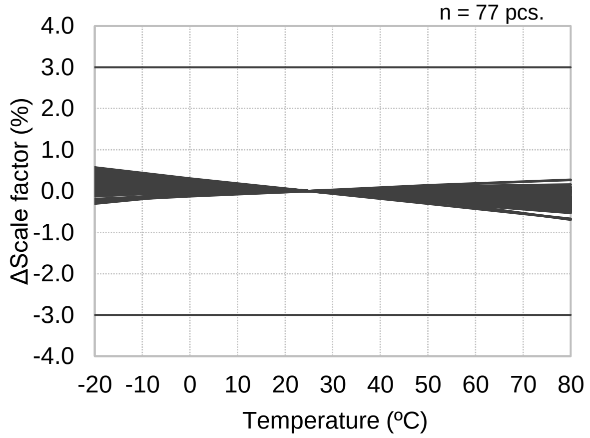


Figure 5.2. Scale Factor Variation over Temperature

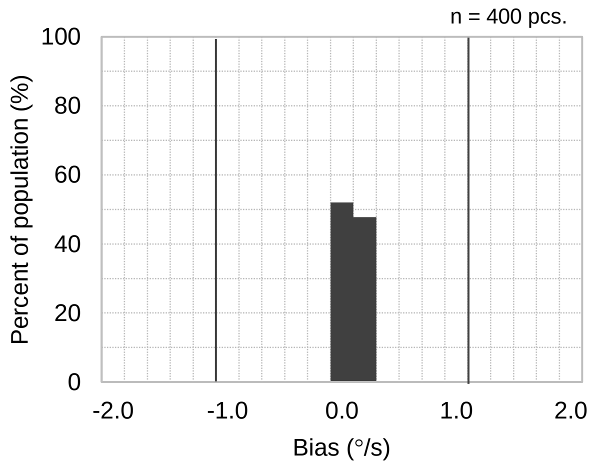


Figure 5.3. Bias Tolerance at T_a = +25 ºC

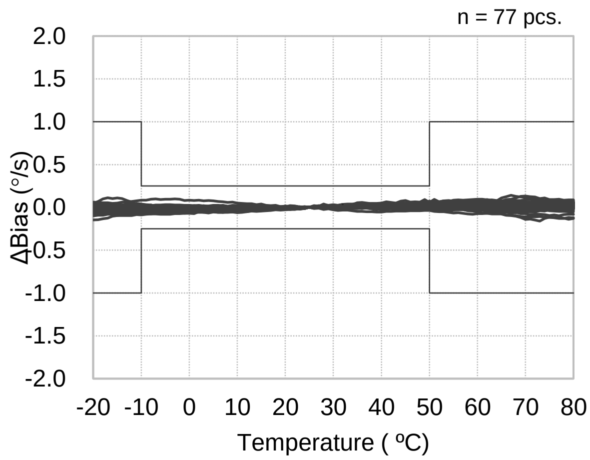


Figure 5.4. Bias Variation over Temperature

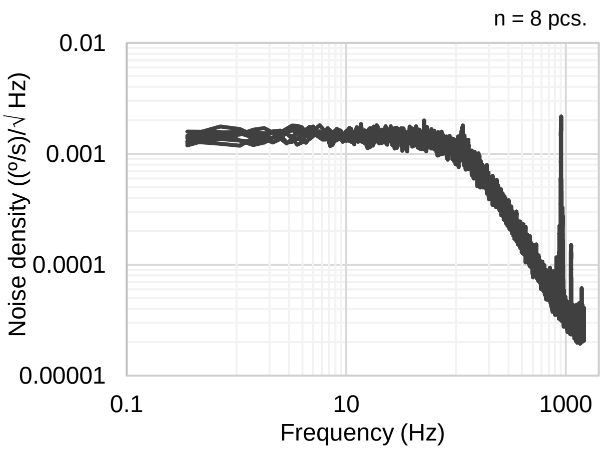


Figure 5.5. Noise Density

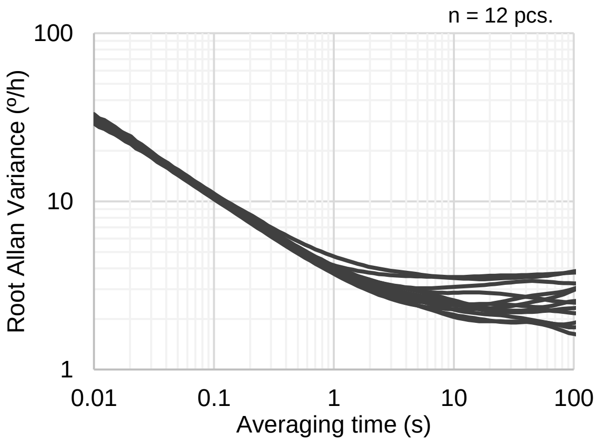


Figure 5.6. Allan Deviation

6. Serial Interface

Access to the sensor is accomplished via serial communication. There are three methods for the serial interface: 4-wire SPI, 3-wire SPI or I²C.

4-wire SPI communication is enabled by turning on the power supply V_{DDM}, waiting for the serial communication wait time t_{IF} noted in Section 3.4 to elapse, and then setting the slave select (SS) to logic level "L" (refer to Section 7.13. SPISel register has a default value of "0" : 4-wire SPI). I²C communication is enabled by setting the SS to logic level "H" (refer to Section 7.13. I²C_EN register has a default value of "1" : I²C enable). 3-wire SPI communication is enabled by setting SPISel to "1": 3-wire SPI and setting the SS to logic level "L". However, setting SPISel to "1" : 3-wire SPI will disable I²C communication.

When the 4-wire SPI with multi-slave function denoted in Section 6.4 is enabled via factory settings, the 4-wire SPI, 3-wire SPI and I²C functions mentioned in Section 6.1 through Section 6.3 cannot be used.

6.1. 4-Wire SPI

4-wire SPI communication is 8 bits width serial communication based on the SS, clock signal (SCLK), data input signal (MOSI), and data output signal (MISO). Set SPISel (register for selecting 4-wire SPI or 3-wire SPI) indicated in Section 7.13 to "0" (the default value is "0" : 4-wire SPI). To use 4-wire SPI communication, set I²C_EN (register for enabling I²C) to "0" disable (default value is "1" : enable).

With falling edge of SS, the initial byte becomes the address. During serial data transfer, the SS must be maintained at logic level "L." If the SS is set to logic level "H," the serial data transfer will be canceled.

The initial address bit (MSB) is the write/read control bit. Set as "0" to write data to the register and set as "1" to read data from the register.

The subsequent bits 2 (A [6:5]) are the slave device (Gyro) address when the multi-slave function is enabled. Refer to Section 6.4 (4-wire SPI with multi-slave Function) and transfer the address of the slave device (Gyro) you want to access. Set to "00" when the multi-slave function is disabled.

Bits 5 (A <4:0>) on the LSB side of the address are the register address. Set the address of the register you want to access. The 2nd byte is the settings value for each register. Refer to the register map in Chapter 7 and transfer the values you want to set.

The register write sequence for 4-wire SPI is shown in Figure 6.1. Write data is transferred after the address. Maintain the SS at logic level "L" during the period between address and data transfer. During the write sequence, the MISO logic level is "L". X is "1" or "0".

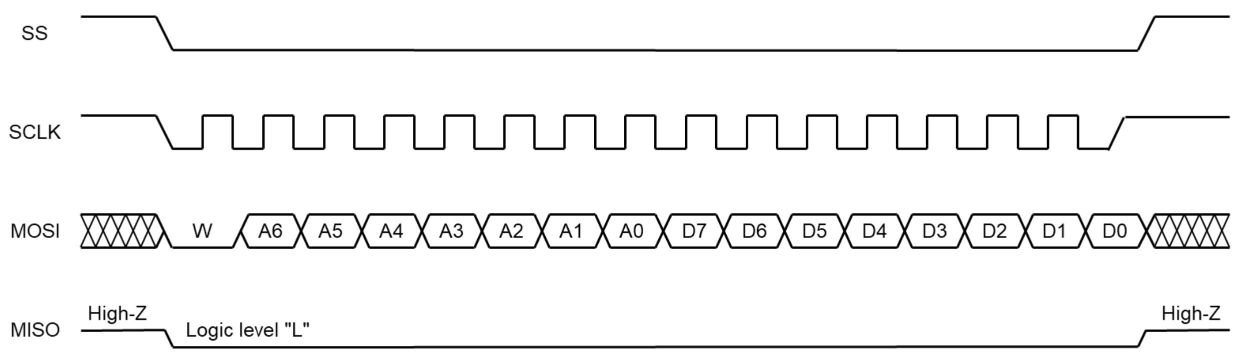


Figure 6.1. Write Sequence for 4-Wire SPI

The register read sequence for 4-wire SPI is shown in Figure 6.2. After the address transfer is complete, data will simultaneously output with the SCLK falling edge beginning with the 2nd byte. Similar to the write sequence, during data non-output, the MISO logic level is "L". X is "1" or "0". Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.11). After reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read (the same applies to reading the temperature sensor data).

The sequence for only the address transfer (command) is shown in Figure 6.3. The register map indicated in Chapter 7 includes the items for only a partial address transfer (command). Similar to the register write sequence, set the first bit (MSB) of the address to "0". Bits 5 (A <4:0>) on the LSB side of the address are the register address (command). Set the address (command) you want to execute. After transferring the address (command), set the SS from logic level "L" to logic level "H" and end the serial communication. During the address tranfer sequence, the MISO logic level is "L". X is "1" or "0".

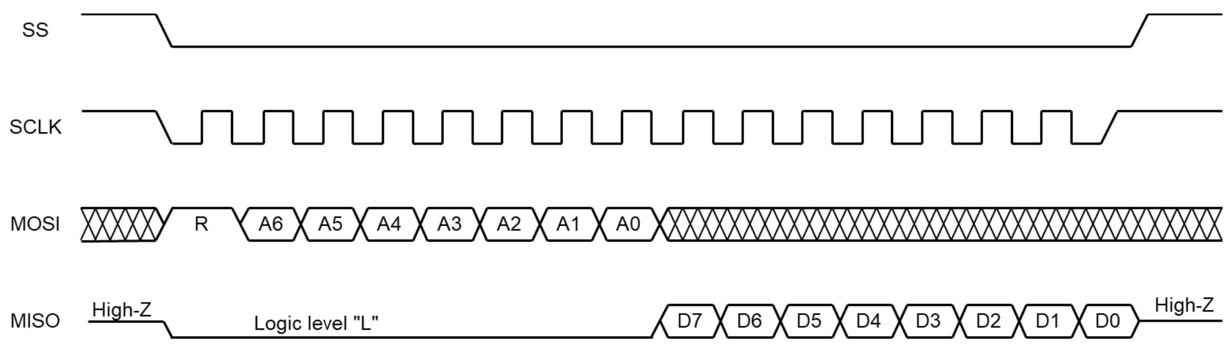


Figure 6.2. Read Sequence for 4-Wire SPI

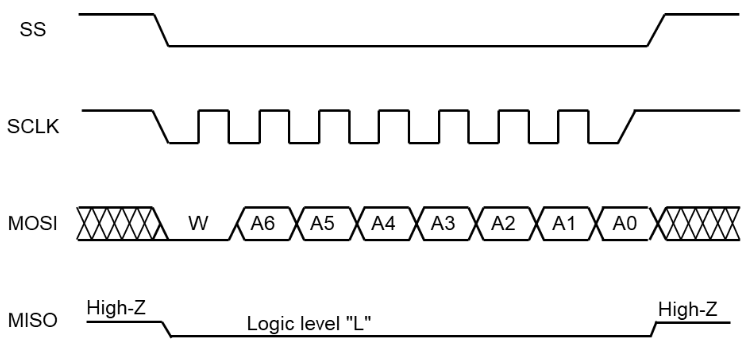


Figure 6.3. Address Setting Sequence for 4-Wire SPI

The timing diagrams for 4-wire SPI are indicated in Figure 6.4 and Figure 6.5.

Table 6.1. AC Characteristics for 4-Wire SPI

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Condition	V_{DDI} ≤ 2.4 V			V_{DDI} > 2.4 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SS setup time	t_{SSS}		15	-	-	15	-	-	ns
SS hold time	t_{SSH}		100	-	-	100	-	-	ns
SS high pulse width	t_{SSHW}		30	-	-	30	-	-	ns
Clock cycle	t_{SCYC}		200	-	-	100	-	-	ns
Clock high pulse width	t_{SHW}		90	-	-	40	-	-	ns
Clock low pulse width	t_{SLW}		90	-	-	40	-	-	ns
Data setup time	t_{SDS}		10	-	-	10	-	-	ns
Dat a hold time	t_{SDH}		10	-	-	10	-	-	ns
Read access time	t_{SACC}	Max. C_L = 30 pF	-	-	80	-	-	30	ns
Output disable time	t_{SOH}		-	-	30	-	-	30	ns

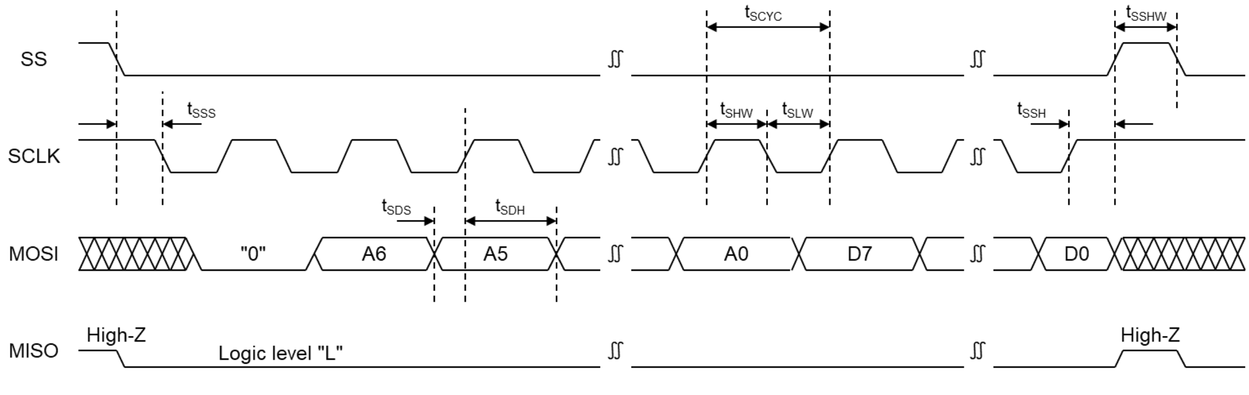


Figure 6.4. Timing Diagram of Writing for 4-Wire SPI

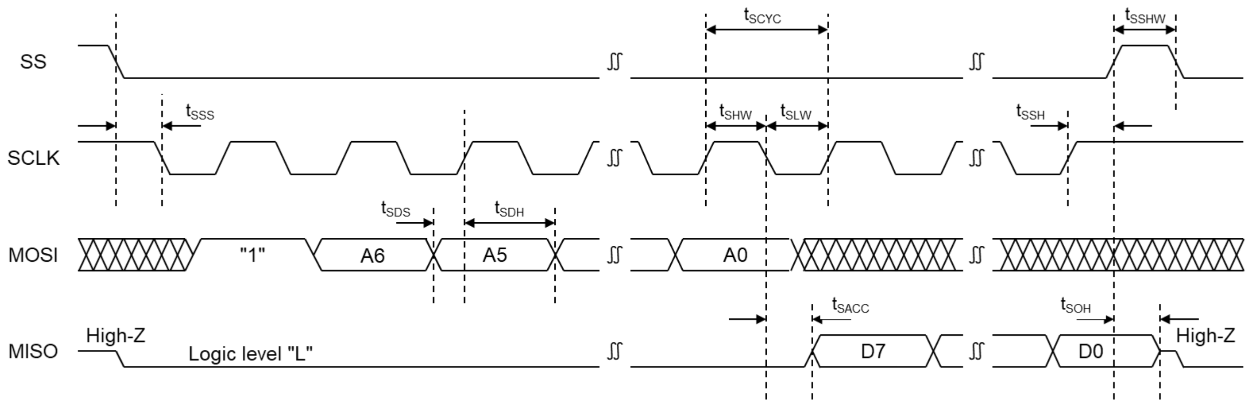


Figure 6.5. Timing Diagram of Reading for 4-Wire SPI

(Note) X is "1" or "0".

6.2. 3-Wire SPI

The 3-wire SPI communication is 8 bits width serial communication based on the slave select signal (SS), the clock signal (SCLK), and the data input/output signal (MOSI). Set SPISel (register for selecting 3-wire SPI or 4-wire SPI) indicated in Table 7.8 to "1" (the default value is "0" : 4-wire SPI). Setting SPISel to "1" will disable the I²C communication.

Similar to 4-wire SPI, with the falling edge of SS the initial byte becomes the address. During serial data transfer, the SS must be maintained at logic level "L". If the SS is set to logic level "H", the serial data transfer will be canceled.

The initial address bit (MSB) is the write/read control bit. Set as "0" to write data to the register and set as "1" to read data from the register. Bits 5 (A <4:0>) on the LSB side of the address is the register address. Set the address of the register you want to access. The 2nd byte is the settings value for each register. Refer to the register map in Chapter 7 and transfer the values you want to set.

The register write sequence for 3-wire SPI is shown in Figure 6.6. Write data is transferred after the address. Maintain the SS at logic level "L" during the period between address and data transfer. X is "1" or "0."

The register read sequence for 3-wire SPI is shown in Figure 6.7. After the address transfer is complete, data is simultaneously outputted with the SCLK fall beginning from the 2nd byte. Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.11). After reading the angular rate data from the 1st byte, maintain the SS at logic level "L" and continue clock input via the SCLK until the desired bit is read. The same applies to read the temperature sensor data. X is "1" or "0".

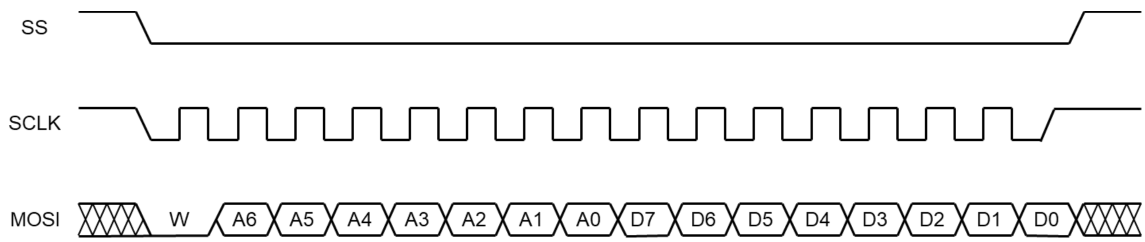


Figure 6.6. Write Sequence for 3-Wire SPI

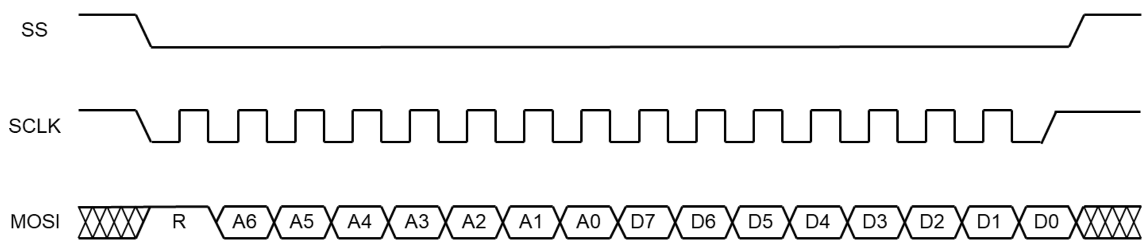


Figure 6.7. Read Sequence for 3-Wire SPI

The sequence for only the address transfer (command) is shown in Figure 6.8. The register map indicated in Chapter 7 includes the items for only a partial address transfer (command). Similar to the register write sequence, set the first bit (MSB) of the address to "0." Bits 5 (A<4:0>) on the LSB side of the address are the register address (command). Set the address (command) you want to execute. After transferring the address (command), set the SS from logic level "L" to logic level "H" and end the serial communication. X is "1" or "0."

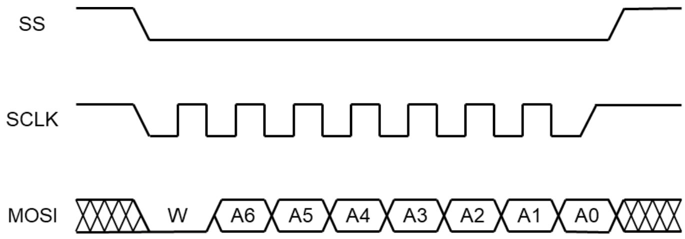


Figure 6.8. Address Setting Sequence for 3-Wire SPI

The timing diagrams for 3-wire SPI are indicated in Figure 6.9 and Figure 6.10.

Table 6.2. AC Characteristics for 3-Wire SPI

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Paramter	Symbol	Condition	V_{DDI} ≤ 2.4 V			V_{DDI} > 2.4 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SS setup time	t_{SSS}		15	-	-	15	-	-	ns
SS hold time	t_{SSH}		100	-	-	100	-	-	ns
SS high pulse width	t_{SSHW}		30	-	-	30	-	-	ns
Clock cycle	t_{SCYC}		200	-	-	100	-	-	ns
Clock high pulse width	t_{SHW}		90	-	-	40	-	-	ns
Clock low pulse width	t_{SLW}		90	-	-	40	-	-	ns
Data setup time	t_{SDS}		10	-	-	10	-	-	ns
Data hold time	t_{SDH}		10	-	-	10	-	-	ns
Read access time	t_{SACC}	Max. C_L = 30 pF	-	-	80	-	-	80	ns
Output disable time	t_{SOH}		-	-	30	-	-	30	ns

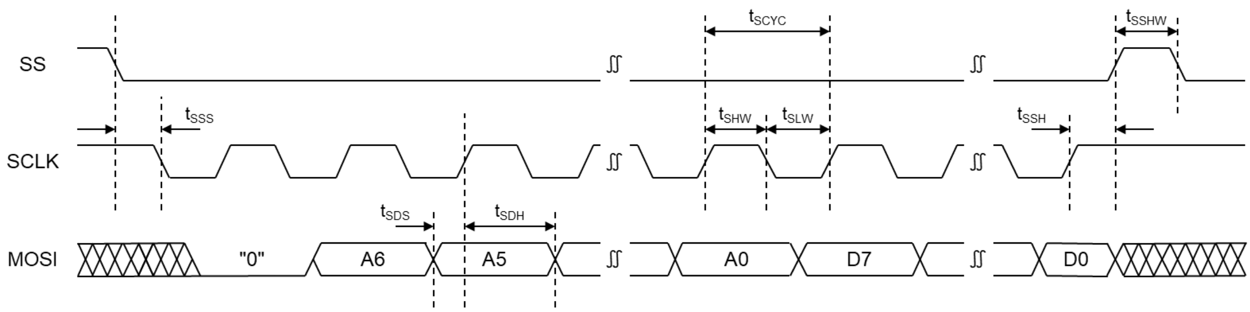


Figure 6.9. Timing Diagram of Writing for 3-Wire SPI

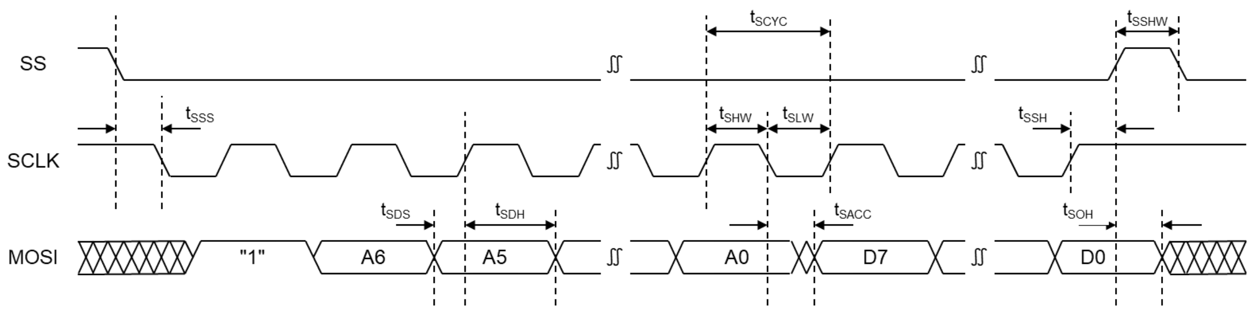


Figure 6.10. Timing Diagram of Reading for 3-Wire SPI

(Note) X is "1" or "0".

6.3. I^{2}C

I^{2}C communication is 8 bits width serial communication based on the clock signal (SCL) and data address signal (SDA). Set I^{2}C_EN (register enabling for I^{2}C) indicated in Table 7.8) to "1" (the default value is "1" : Enable). To use I^{2}C communication, fix the slave select signal (SS) used in 4-wire or 3-wire SPI communication to logic level "H" (interface power supply voltage V_{DDI}).

I^{2}C communication is initiated by issuing the start condition (ST, with SCL status at logic level "H", SDA is changed from logic level "H" to logic level "L") from the master. And communication is stopped by issuing the stop condition (SP, with SCL status at logic level "H", SDA is changed from logic level "L" to logic level "H") from the master.

To access the internal register, read (Read = ”1”) /write (Write = ”0”) the slave device address (ADR, address that adds the SA0 "0" or "1" to "110101") to/from the master and transmit the total 1 byte that includes 1 bit ID signal. After ADR receipt, the slave will check to see if the address matches its own address. If matching, the slave returns an ACK (acknowledge), after which communication is possible. If the address does not match, the slave returns to idle mode and waits until another ST is issued.

The SA0 terminal is set to pull down internally(approx. 100 kΩ). If the SA0 terminal is set to "0," then connect to N.C. or GND. Or, if the SA0 terminal is set to "1", then connect to V_{DDI}. In this case, a current of approximately 30 µA @ V_{DDI} = 3 V will flow to the SA0 terminal. To reduce the current, add a desired resistor to the V_{DDI} and the SA0 terminal. Alternatively, you can change the terminal setting from pull down to pull up by rewriting the SelMISO [1:0] indicated in Section 7.13 after turning the power ON and once the serial communication wait time t_{IF} indicated in Section 3.4 has elapsed. Refer to Section 6.7 the MISO/SA0 Terminal Control Methods for details on control methods.

Next, send the internal register address (SUB-ADR). Input "0" for the first bit (MSB) of the address (there is not function allocation). The remaining LSB-side 7 bits (A <6:0> are the register address (for detail, refer to register map in Chapter 7). After transferring the addres of the register you wish to access, return an ACK.

The following sequence differs between register write, register read, and address (command) transfer. Please refer to the sequences in Figure 6.11 through Figure 6.13.

Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.11). After reading the angular rate data from the 1st byte, set the master to return an ACK (acknowledge) instead of a NACK (non-acknowledge) and then read the 2nd byte or the 3rd byte. The same applies to read the temperature sensor data.

Master	ST	ADR	W		SUB-ADR		DATA		SP
Slave				ACK		ACK		ACK	

Figure 6.11. Write Protocol for I^{2}C

Master	ST	ADR	W		SUB-ADR		ST	ADR	R			NACK	SP
Slave				ACK		ACK				ACK	DATA		

Figure 6.12. Read Protocol for I^{2}C

Master	ST	ADR	W		SUB-ADR		SP
Slave				ACK		ACK	

Figure 6.13. Address Setting Protocol for I^{2}C

ST : Start condition
SP : Stop condition
ADR : Slave device address (110101 + SA0)
R/W : Read = “1”, Write = “0”
SUB-ADR : Internal register address
DATA : Internal register read/write data
ACK : “Low”
NACK : “High”, send at read complete.

As an example of a waveform, register write, register read, and address setting sequence are shown in Figure 6.14 through Figure 6.16.

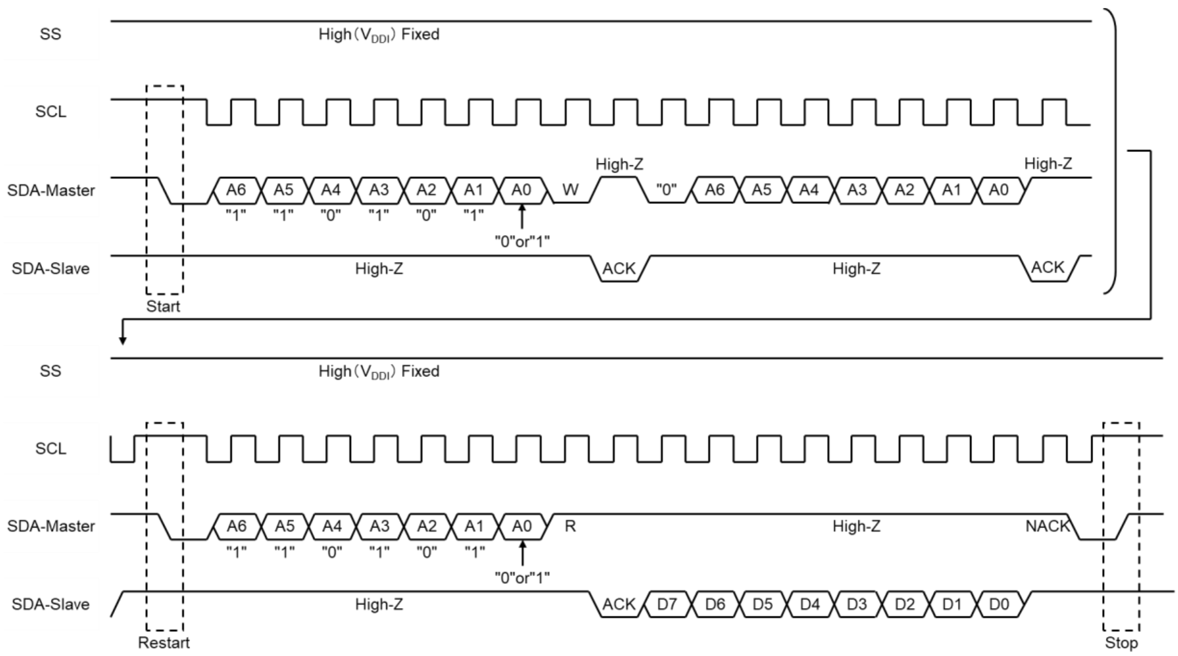


Figure 6.14. Write Sequence for I^2C

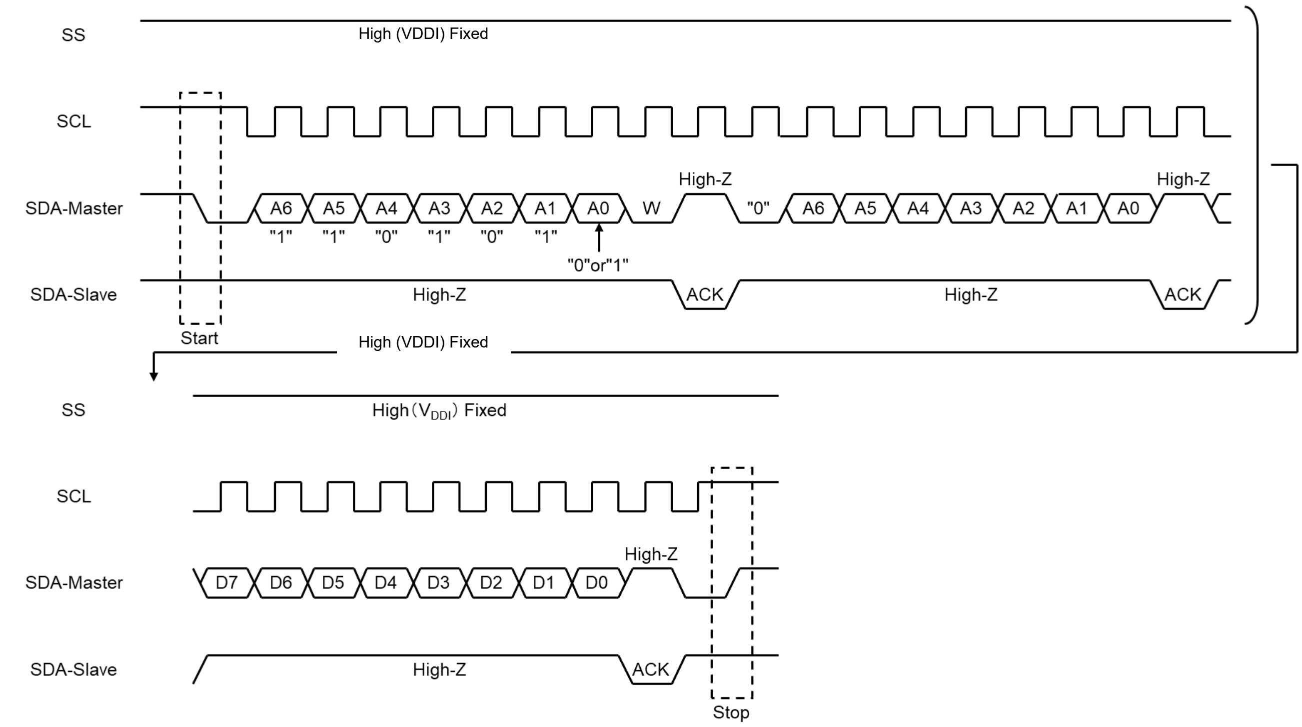


Figure 6.15. Read Sequence for I²C

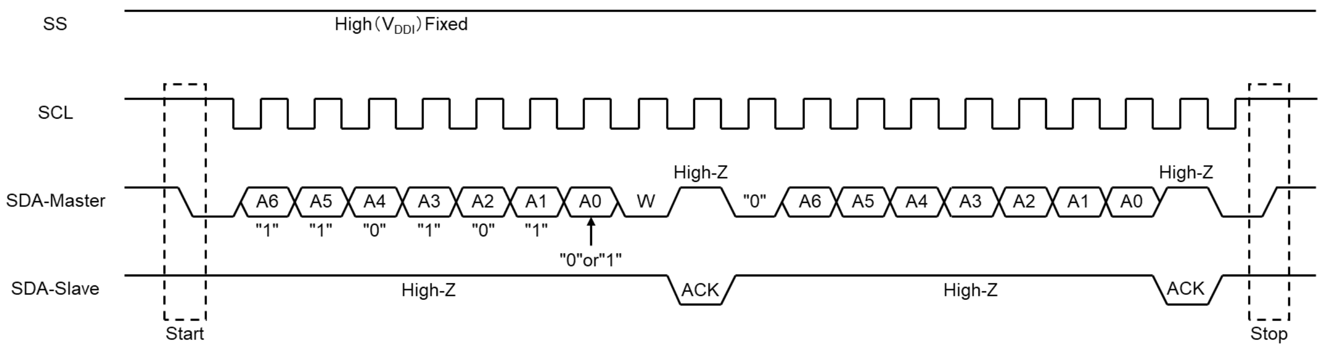


Figure 6.16. Address Setting Sequence for I²C

The timing diagram for I²C is indicated in the Figure 6.17.

Table 6.3. AC Characteristic for I²C

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock cycle	t_{SCL}	2.5	-	-	μs
Clock high pulse width	t_{WH}	0.6	-	-	μs
Clock low pulse width	t_{WL}	1.3	-	-	μs
Data setup time	t_{DS}	0.1	-	-	μs
Data hold time	t_{DH}	0.0	-	-	μs
START condition hold time	t_{SH}	0.6	-	-	μs
Time restart condition setup time	t_{RS}	0.6	-	-	μs
STOP condition setup time	t_{PS}	0.6	-	-	μs
Between STOP and START condition	t_{WS}	1.3	-	-	μs

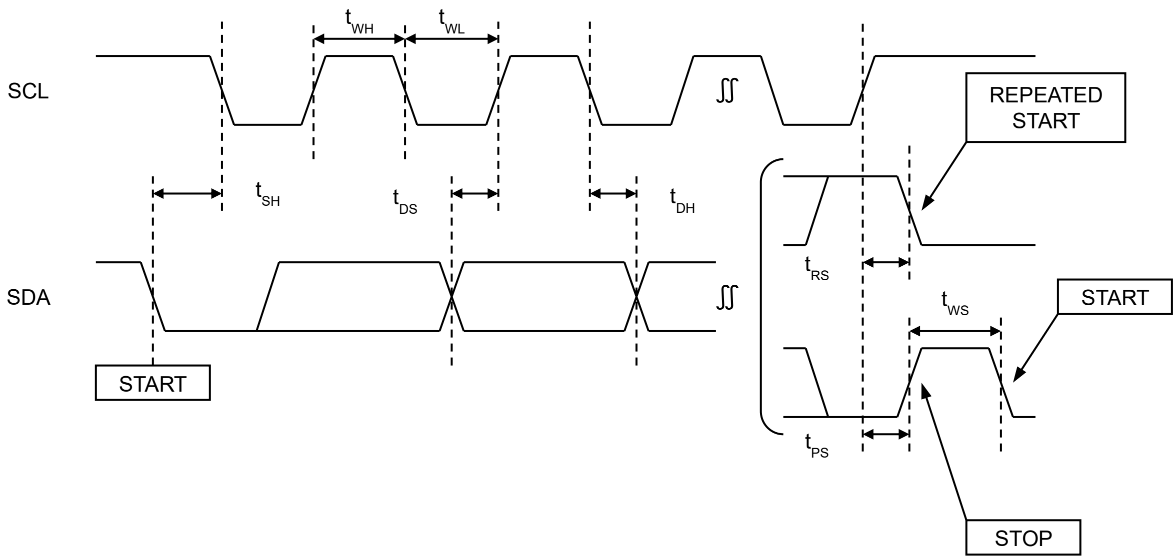


Figure 6.17. Timing Diagram for I²C

6.4. 4-Wire SPI with Multi-Slave Function

The multi-slave function is an extended function of 4-wire SPI mode that is available only through factory settings implemented by Epson. The multi-slave function allows you to reduce I/O ports and board circuitry by connecting multiple (maximum of 3) slave devices (Gyro) to a single master device (MPU). When the multi-slave function is enabled via factory settings, other serial communication (4-wire SPI, 3-wire SPI, and I^2C) cannot be used.

A connection example using 3 slave devices is shown in Figure 6.18. Three slave devices (Gyro) share a serial communications port connection on a single master device (MPU).

Each slave device (Gyro) is assigned the respective address shown in Table 6.4. Setting the address A [6:5] indicated in Section 6.1 enables serial communication with the desired slave device.

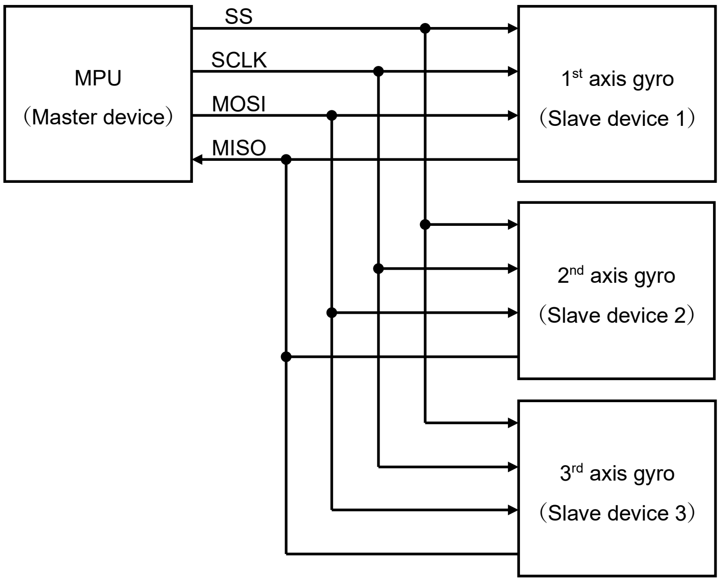


Figure 6.18. Connection Examples

Table 6.4. Slave Device Addresses and Product Name

A [6]	A [5]	Selected slave device	Product name
0	0	All slave devices	-
0	1	1st axis Gyro	XV7021BB 49.600kHz C
1	0	2nd axis Gyro	XV7021BB 51.000kHz D
1	1	3rd axis Gyro	XV7021BB 53.600kHz E

(Note) When the maximum 3 slave devices are connected.

Furthermore, when the address A [6:5] is set to "00", a register write command will write the same data to all slave devices, but register read commands are not common to all devices. Even if the read/write control bit (first bit of address: MSB) indicated in Section 6.1 is mistakenly set to "1" (read), the MISO value is "High-Z" (excluding global angular rate reads).

The register write sequence when using the multi-slave function is shown in Figure 6.19. Write data is transferred after the slave device address and register address. Maintain the SS at logic level "L" during the period between address and data transfer. During the write sequence, the MISO value is "High-Z". X is "1" or "0".

The register read sequence when using the multi-slave function is shown in Figure 6.20. After the slave device address and register address transfer is complete, data is simultaneously outputted with falling edge of SCLK and beginning from the 2nd byte. Similar to the write sequence, during data non-output, the MISO setting is "High-Z". X is "1" or "0". Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.11). After reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read (the same applies to read the temperature sensor data).

The sequence for only the address transfer (command) via the multi-slave function is shown in Figure 6.21. Maintain the SS at logic level "L" during address transfer. During the address transfer sequence, the MISO value is "High-Z". X is "1" or "0".

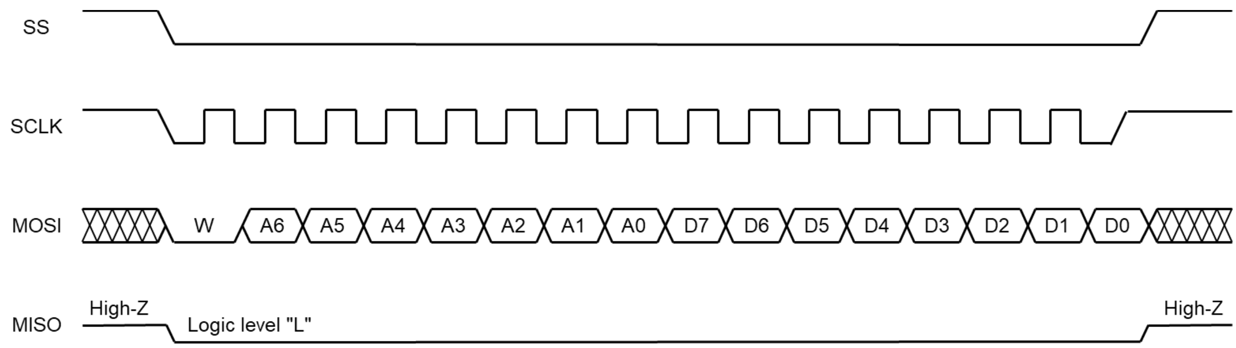


Figure 6.19. Write Sequence for 4-Wire SPI with Multi-Slave Function

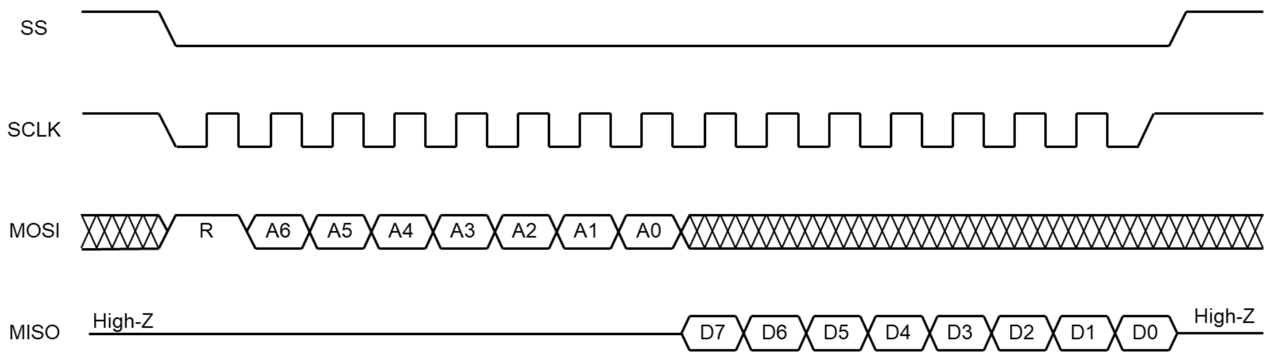


Figure 6.20. Read Sequence for 4-Wire SPI with Multi-Slave Function

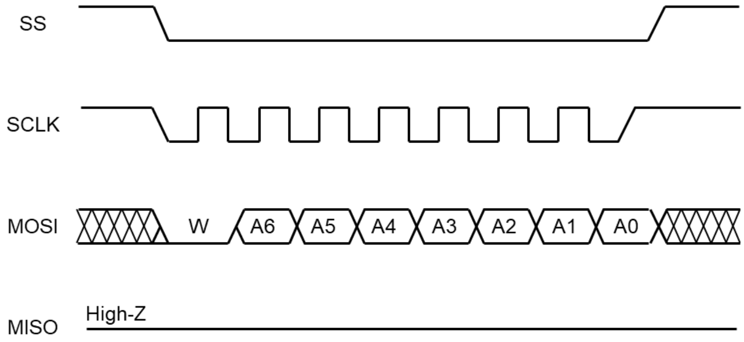


Figure 6.21. Address Setting Sequence for 4-Wire SPI with Multi-Slave function

The timing diagram for 4-wire SPI with multi slave function are indicated in Figure 6.22 and Figure 6.23.

Table 6.5. AC Characteristics for 4-Wire SPI with Multi-Slave Function

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Condition	$V_{DDI} \leq 2.4$ V			$V_{DDI} > 2.4$ V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SS setup time	t_{SSS}		15	-	-	15	-	-	ns
SS hold time	t_{SSH}		100	-	-	100	-	-	ns
SS high pulse width	t_{SSHW}		30	-	-	30	-	-	ns
Clock cycle	t_{SCYC}		200	-	-	100	-	-	ns
Clock high pulse width	t_{SHW}		90	-	-	40	-	-	ns
Clock low pulse width	t_{SLW}		90	-	-	40	-	-	ns
Data setup time	t_{SDS}		10	-	-	10	-	-	ns
Data hold time	t_{SDH}		10	-	-	10	-	-	ns
Read access time	t_{SACC}	Max. C_L = 30 pF	-	-	80	-	-	30	ns
Output disable time	t_{SOH}		-	-	30	-	-	30	ns

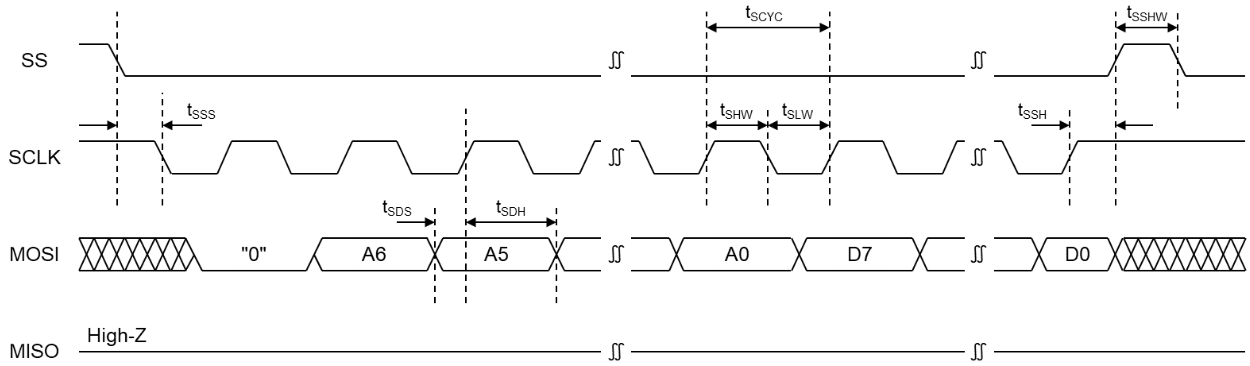


Figure 6.22. Timing Diagram of Writing for 4-Wire SPI with Multi-Slave Function

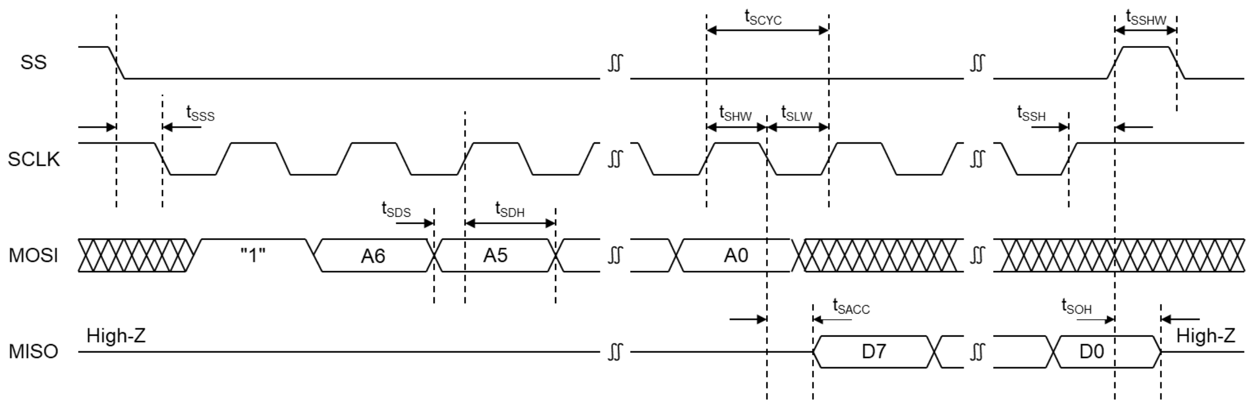


Figure 6.23. Timing Diagram of Reading for 4-Wire SPI with Multi-Slave Function

(Note) X is "1" or "0".

6.5. Angular Rate Data Read

6.5.1. 4-Wire SPI, 3-Wire SPI and I²C (Multi-Slave Function Disabled)

The angular rate read function is conducted using the DatAccOn indicated in Table 7.1. Angular rate data uses the 2's compliment expression and has a data width of 16 bits or 24 bits (switch using the DataFormat indicated in Table 7.6). During serial communication, after reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read.

When in 4-wire SPI or 3-wire SPI communication mode, after reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read.

When in I²C communication mode, after reading the angular rate data from the 1st byte, set the master to return an ACK (acknowledge) instead of a NACK (non-acknowledge) and then read the 2nd byte or the 3rd byte.

Table 6.6. Angular Rate Data Output Control

A [6:5]	DataFormat	Data output order		
		1st byte	2nd byte	3rd byte
00	0	D [15:8]	D [7:0]	
00	1	D [23:16]	D [15:8]	D [7:0]

(Note) DataFormat is the angular rate data format indicated in Table 7.6.

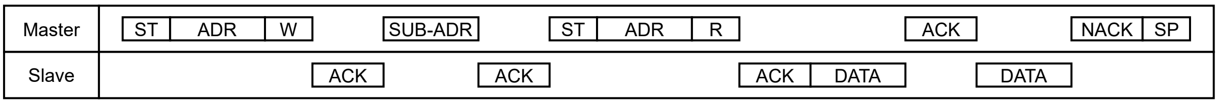


Figure 6.24. Angular Rate Data (16 Bits Output)

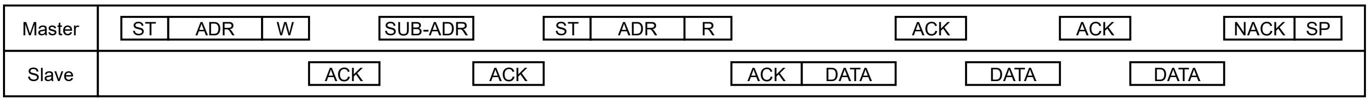


Figure 6.25. Angular Rate Data (24 Bits Output)

6.5.2. 4-Wire SPI with Multi-Slave Function

The angular rate read function is conducted using the DatAccOn indicated in Table 7.1. Angular rate data uses the 2's compliment expression and has a data width of 16 bits or 24 bits (switch using the DataFormat indicated in Table 7.6). There are two reading methods, Global angular rate read and Normal angular rate read.

Global angular rate read is shown in Figure 6.26. This reading method is available only when 3 slave devices are connected. To conduct a global angular rate read, set the slave device address A [6:5] to "00". After the angular rate data for the 1st axis gyro, the angular rates for the 2nd gyro and then the 3rd gyro are output. During serial communication, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read. If the logic level for the SS is changed from "L" to "H" before the desired bit is read, then no further angular rate data is outputted. Redo the angular rate data read command (DatAccOn). If the SCLK is stopped with the SS level maintained at level "L" before the desired bit is read, the angular rate data read can be outputted by restarting the SCLK input.

Global angular rate read operation method 1 is shown in Figure 6.27. After the angular rate data for the 1st axis gyro, the angular rates for the 2nd gyro and then the 3rd gyro are output. After the desired bit is read, raise the SS from logic level "L" to logic level "H." Run the angular rate data read command (DatAccOn) to read the angular rate data again.

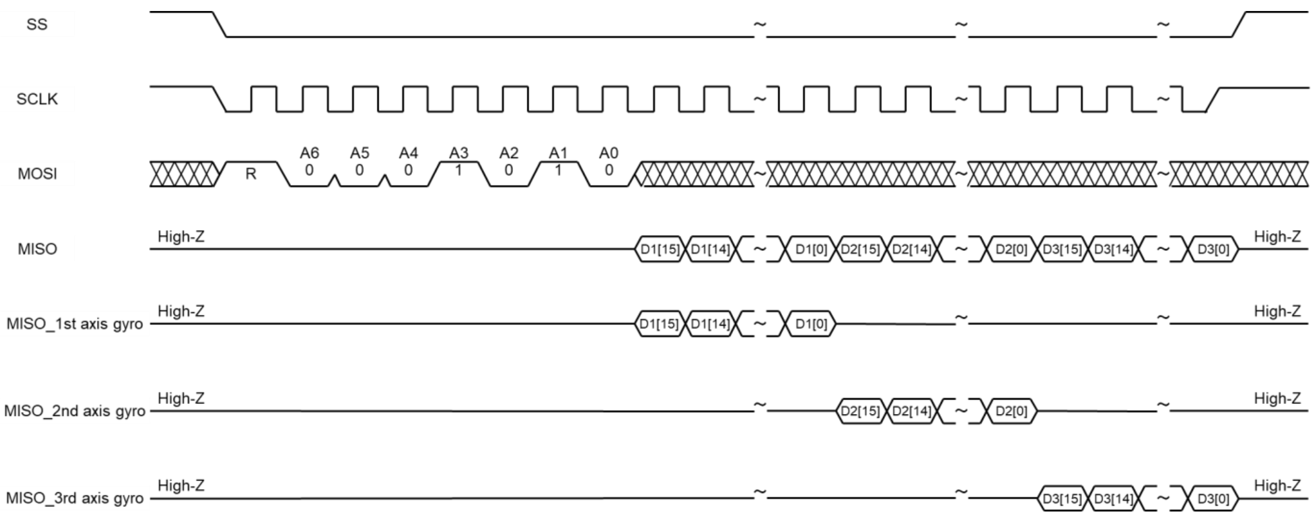


Figure 6.26. Global Angular Rate Read

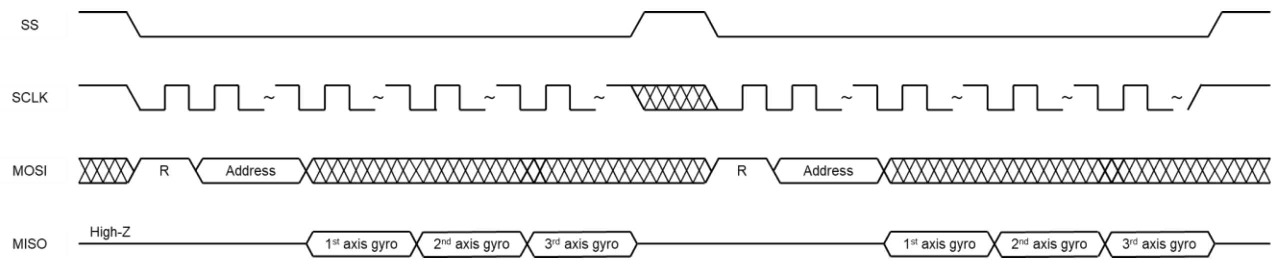


Figure 6.27. Global Angular Rate Read Operation Method 1

Global angular rate read operation method 2 is shown in Figure 6.28. The data output order is shown in Table 6.7. After the angular rate data for the 3rdaxis gyro is output, input the SCLK with the SS logic level at "L" to output the 2nd order angular rate data (1st – 3rdgyro). This angular rate data read can be repeated in the order of 3rd, 4th until the SS logic level is set to "H".

The read angular rate data update is conducted during the read period for the lower 8 bits of the angular rate data of the previous axis (ex: the angular rate data for 1st axis gyro of the 2nd order is updated during the read period for the lower 8 bits of angular rate data from the 3rd axis gyro of the 1st order).

Normal angular rate read is shown in Figure 6.29. For the slave device address A [6:5] used during normal angular rate read, set a desired slave device address (any of the Gyro addresses for the 1st through 3rd axes) from the addresses indicated in Table 6.4. During serial communication, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read. If the logic level for the SS is changed from "L" to "H" before the desired bit is read, then no further angular rate data is output. Redo the angular rate data read command (DatAccOn). If the SCLK is stopped with the SS logic level maintained at "L" before the desired bit is read, the angular rate data output can be continued by restarting the SCLK input.

After all angular rate data is provided, any angular rate data won't be provided even if the SCLK is sent with the SS logic level maintained at "L" (MISO keeps outputting at logic level "L"). To read angular rate data again, set the SS logic level to "H" (MISO is set to "High-Z") and execute the angular rate data read command (DatAccOn) again.

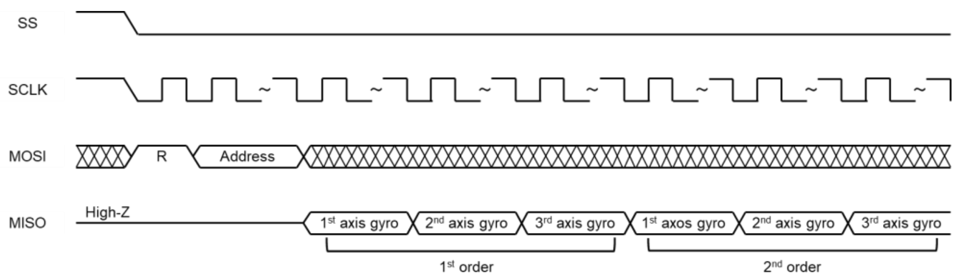


Figure 6.28. Global Angular Rate Read Operation Method 2

Table 6.7. Global Angular Rate Read Operation Method 2 – (Data Output Order)

Epson factory settings	Data output order					
Multi-slave function	1st order			2nd order		
	1st axis gyro	2nd axis gyro	3rd axis gyro	1st axis gyro	2nd axis gyro	3rd axis gyro

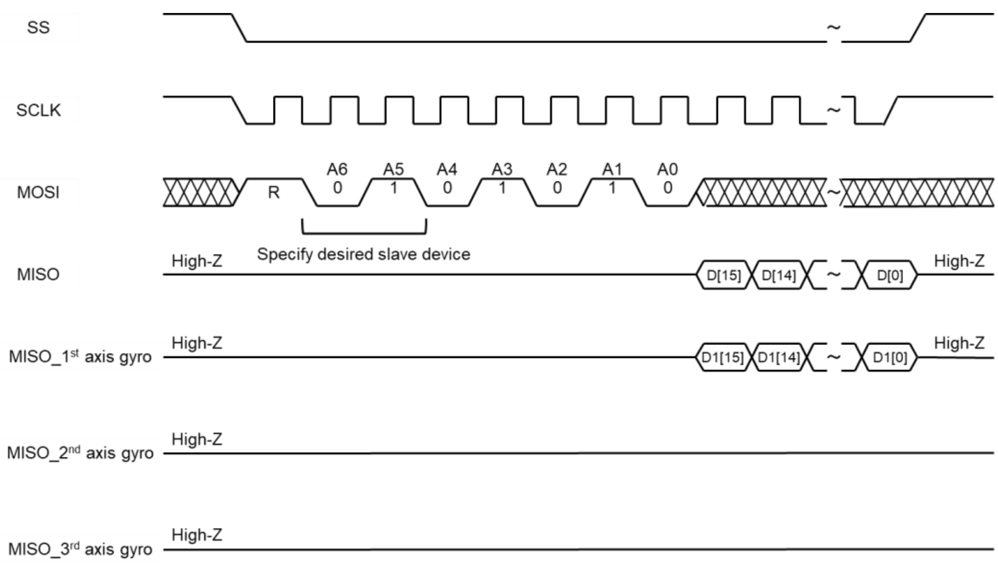


Figure 6.29. Normal Angular Rate Read

The angular rate data output control for both global angular rate read and normal angular rate read are indicated in Table 6.8.

Table 6.8. Angular Rate Data Output Control

Read method	A [6:5]	Data Format	Data output order								
			1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte	9th byte
Global angular rate read	00	0	D1 [15:8]	D1 [7:0]	D2 [15:8]	D2 [7:0]	D3 [15:8]	D3 [7:0]			
		1	D1 [23:16]	D1 [15:8]	D1 [7:0]	D2 [23:16]	D2 [15:8]	D2 [7:0]	D3 [23:16]	D3 [15:8]	D3 [7:0]
Normal angular rate read	Other than 00	0	D [15:8]	D [7:0]							
		1	D [23:16]	D [15:8]	D [7:0]						

(Note 1) The address A [6:5] is the slave device address indicated in Table 6.4.

(Note 2) DataFormat is the angular rate data format (DataFormat = 0: 16 bits output/1: 24 bits output) indicated in Table 7.6.

(Note 3) D1 is the angular rate data for the 1st axis gyro, D2 is the angular rate data for the 2nd axis gyro, and D3 is the angular rate data for the 3rd axis gyro.

(Note 4) D is the angular rate data for the slave device (any of the 1st through 3rd axis gyro) specified with the address A [6:5].

(Note 5) With global angular rate read, all slave devices are selected. After D1, the angular rate data for the 1st axis gyro, the angular rate data for D2 and D3 are output. Mistakenly specifying a separate angular rate data format (DataFormat = 0: 16 bits output/1: 24 bits output) for each slave device will result in a conflict in the output angular rate data. As such, make sure the angular rate data format setting is the same for each slave device.

Ex: In the case of 1st axis gyro DataFormat = 1 (24 bits output) and 2nd axis gyro DataFormat = 0 (16 bits output), the angular rate data output in the 3rd byte will result in a conflict.

(Note 6) Global angular rate read (address A [6:5] = "00") can be repeated in the order of 2nd, 3rd until the SS logic level is set to "H".

(Note 7) During the global angular rate read (address A [6:5] = "00"), if there is no slave device on a certain axis, then the angular rate data for that axis is set to "High-Z".

6.6. Angular Rate Data Read

The temperature sensor data read is conducted using the TempRd indicated in Table 7.1. Temperature sensor data uses the 2's compliment expression and has a data width of 8 bits, 10 bits or 12 bits (switch using the TsDataFormat indicated in Table 7.7, the default value is 12 bits). Similar to the angular rate data read function, continue the serial communication until the desired bit is read. Temperature sensor data is updated in intervals of approximately 2.4 ms.

Table 6.9. Temperature Sensor Data Output Control

TsDataFormat [1]	TsDataFormat [0]	Data output order	
		1st byte	2nd byte
0	0	D [7:0]	
0	1	D [9:2]	D [1:0] (Note 1)
1	0	D [11:4]	D [3:0] (Note 2)
1	1		

(Note 1) Logic level "L" is outputted at LSB-side 6 bits.

(Note 2) Logic level "L" is outputted at LSB-side 4 bits.

6.7. Control MISO/SA0

MISO/SA0 terminal status as indicated in Table 6.10 can be changed by rewriting SelMISO [1:0] indicated in Section 7.13.

Table 6.10. MISO/SA0 Terminal Control Method

Mode	**SPISel**	**I^2C_EN**	**SelMISO** [1]	**SelMISO** [0]	SS	MISO/SA0
Multi-slave	X	X	X	X	0	Output (Note 2)
	X	X	X	X	1	High-Z
4-wire SPI	0 (4-wire)	0 (I^2C Disable)	X	X	0	Output
	0	0	0	0	1	Output Level ”L”
	0	0	0	1	1	Output Level ”H”
	0	0	1	X	1	High-Z
3-wire SPI	1 (3-wire)	X	0	0	X	Output Level ”L”
	1	X	0	1	X	Output Level ”H”
	1	X	1	X	X	High-Z
I^2C	0	1 (I^2C Enable)	0	0	1	Input
	0	1	0	1	1	High-Z (Note 3)
	0	1	1	0	1	Input (pull-down)
	0	1	1	1	1	Input (pull-up)

(Note 1) The default value for SelMISO [1] is "1" and "0" for SelMISO [0].

(Note 2) The status is outputted during data read, “High-Z” during other times.

(Note 3) SA0 is fixed at "0" within the IC.

6.8. Command Validation Time

6.8.1. 4-Wire SPI, 3-Wire SPI and 4-Wire SPI with Multi-Slave Function

Table 6.11. Command Validation Time for SPIs

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Sleep-in wait time	t_{SLPIN}	10	-	-	μs
Sleep-out wait time (Note 1)	t_{SLPOUT}	10	-	-	μs
Standby wait time	t_{STBY}	10	-	-	μs
Software reset wait time	t_{SWRST}	10	-	-	μs

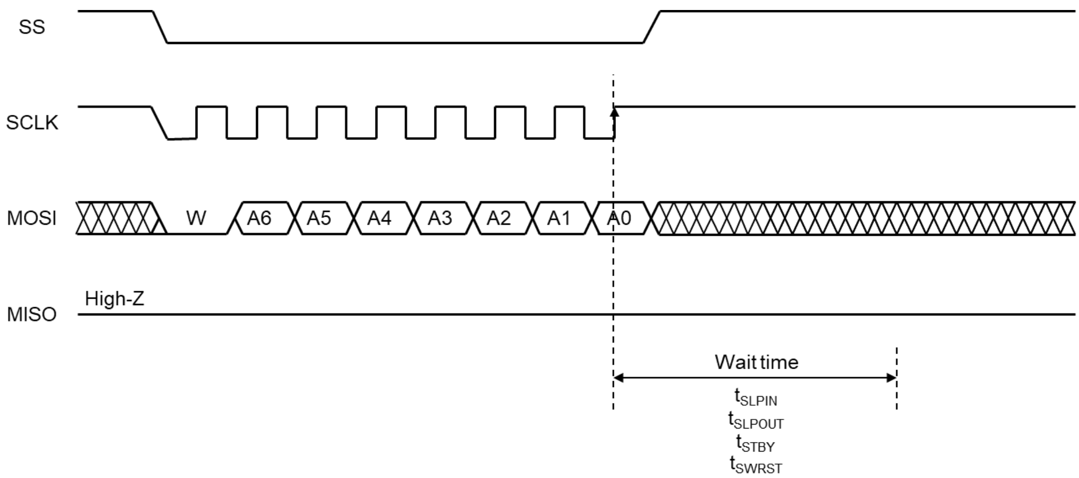


Figure 6.30. Command Validation Time for SPIs

(Note 1) Sleep-out command is validated after Sleep-in or Standby command issued and wait for t_{SLPOUT} or t_{STBY} to elapse.

(Note 2) X is "1" or "0".

6.8.2. I²C

Table 6.12. Command Validation Time for I²C

V_{DDM} = 2.7 to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Sleep-in wait time	t_{SLPIN}	10	-	-	μs
Sleep-out wait time (Note 1)	t_{SLPOUT}	10	-	-	μs
Standby wait time	t_{STBY}	10	-	-	μs
Software reset wait time	t_{SWRST}	10	-	-	μs

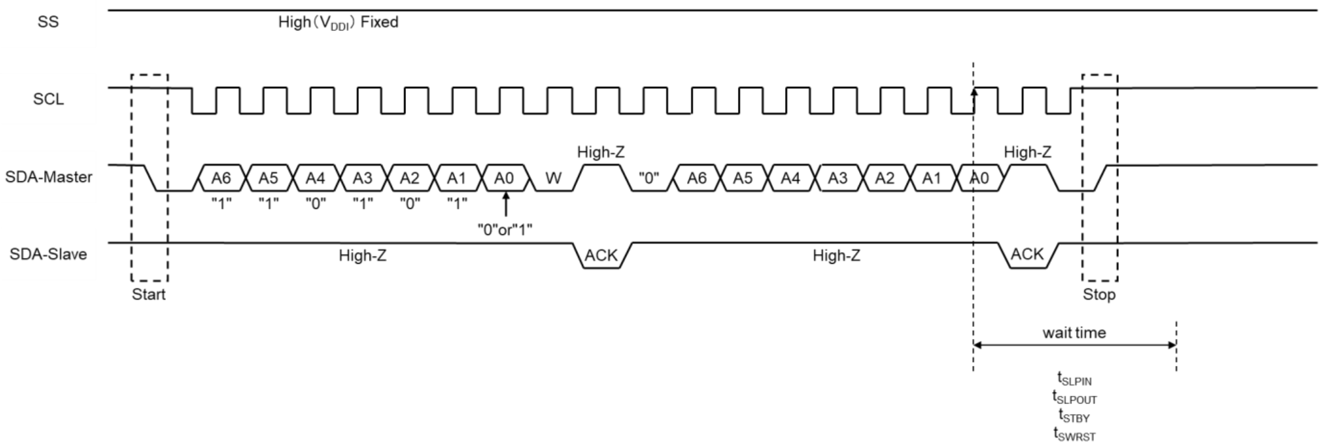


Figure 6.31. Command Validation Time for I²C

(Note 1) Sleep-out command is validated after Sleep-in or Standby command issued and wait for t_{SLPOUT} or t_{STBY} to elapse.

7. User Command Register

Table 7.1. User Command Register

Address	Register	R/W	Function
0x00	Reserved		
0x01	DspCtl1	R/W	DSP settings 1
0x02	DspCtl2	R/W	DSP settings 2
0x03	DspCtl3	R/W	DSP settings 3
0x04	StsRd	R	Status read
0x05	SlpIn	C	Sleep-in
0x06	SlpOut	C	Sleep-out
0x07	Stby	C	Standby
0x08	TempRd	R	Temperature sensor data read
0x09	SWRst	C	Software reset (user command register reset)
0x0a	DatAccOn	R	Angular rate data read
0x0b	OutCtl1	R/W	Angular rate data read control
0x0c	AutoC	C	Zero rate level calibration command
0x0d	Reserved		
0x0e	Reserved		
0x0f	Reserved		
0x10	Reserved		
0x11	Reserved		
0x12	Reserved		
0x13	Reserved		
0x14	Reserved		
0x15	Reserved		
0x16	Reserved		
0x17	Reserved		
0x18	Reserved		
0x19	Reserved		
0x1a	Reserved		
0x1b	Reserved		
0x1c	TsDataFormat	R/W	Temperature sensor data format
0x1d	Reserved		
0x1e	Reserved		
0x1f	IFCtl	R/W	Serial interface settings

R : Register read

R/W: Register read and register write

C : Specify address (command)

(Note) Reserved resister must not be changed. Writing to those registers may cause permanent damage to the device.

7.1. DSP Settings 1

Table 7.2. DSP Settings 1

Address	Bit	Register	Default	R/W	Function	Settings
0x01	7	Reserved	0	R	Reserved	Reserved
	6	HpfFc [2]	0	R/W	HPF (1st order) f_c select	HpfFc [2:0] 000: 0.01 Hz 001: 0.03 Hz 010: 0.1 Hz 011: 0.3 Hz 100: 1 Hz 101: 3 Hz 110: 10 Hz 111: Not-available
	5	HpfFc [1]	1	R/W		
	4	HpfFc [0]	0	R/W		
	3	Reserved	0	R/W	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	EnableHpf	0	R/W	HPF Enable	0: Disable 1: Enable
	0	Reserved	1	R/W	Reserved	Reserved

(Note) Reserved resister must not be changed. Use the default settings.

7.2. DSP Settings 2

Table 7.3. DSP Settings 2

Address	Bit	Register	Default	R/W	Function	Settings
0x02	7	Reserved	0	R	Reserved	Reserved
	6	EnDetFreq	0	R/W	Notch filter	0: Disable 1: Enable
	5	LpfOrder [1]	0	R/W	LPF order select	LpfOrder [1:0] 00: 2nd order 01: 3rd order 10: 4th order 11: Not Available
	4	LpfOrder [0]	0	R/W		
	3	LpfFc [3]	0	R/W	LPF f_c select	LpfFc [3:0] 0000: 10 Hz 0001: 35 Hz 0010: 45 Hz 0011: 50 Hz 0100: 70 Hz 0101: 85 Hz 0110: 100 Hz 0111: 140 Hz 1000: 175 Hz 1001: 200 Hz 1010: 285 Hz 1011: 345 Hz 1100: 400 Hz 1101: 500 Hz 1110: Not Available 1111: Not Available
	2	LpfFc [2]	1	R/W		
	1	LpfFc [1]	1	R/W		
	0	LpfFc [0]	0	R/W		

(Note) Reserved resister must not be changed. Use the default settings.

7.3. DSP Settings 3

Table 7.4. DSP Settings 3

Address	Bit	Register	Default	R/W	Function	Settings
0x03	7	Reserved	0	R	Reserved	Reserved
	6	EnCalibCmd	0	R/W	Zero rate level calibration	0 : Disable, 1 : Enable (Note 2)
	5	Reserved	0	R/W	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	SelFs [2]	0	R/W	Select angular rate output of the sampling frequency f_s	SelFs [2:0] (Note 3) 000: f_s 001: $f_s/2$ 010: $f_s/4$ 011: $f_s/8$ 100: $f_s/16$ 101: $f_s/32$ 110: $f_s/64$ 111: $f_s/128$
	1	SelFs [1]	0	R/W		
	0	SelFs [0]	0	R/W		

(Note 1) Reserved resister must not be changed. Use the default settings.

(Note 2) To carry out zero rate level calibration in Section 7.12, setting should be Enable.

(Note 3) The f_s is the AD converter sampling frequency. It carries out down sampling of the angular rate output.

7.4. Status Read

Table 7.5. Status Read

Address	Bit	Register	Default	R/W	Function	Settings
0x04	7	Reserved		R	Reserved	Reserved
	6	Reserved		R	Reserved	Reserved
	5	Reserved		R	Reserved	Reserved
	4	Reserved		R	Reserved	Reserved
	3	ProcOK		R	Temperature sensor data output flag	0: Data output not available 1: Data output available
	2	preStsPOR		R	Status flag	Bit [2:0] (Note 2) 100: After turning power ON 010: Standby 000: Sleep 001: Sleep out
	1	preStsStby		R		
	0	preStsSlpOut		R		

(Note 1) Reserved resister must not be changed. Use the default settings.

(Note 2) Only indicated combinations allowed.

7.5. Sleep-In

Specify address as "0x05". No data read or write. During sleep, only register access is possible. Status for angular rate data and temperature sensor data is "0". Conduct the sleep-out command in Section 7.6 to disable sleep mode.

7.6. Sleep-Out

Specify address as "0x06". No data read or write. Returns to normal operations from sleep mode or standby mode. This resets the DSP.

7.7. Standby

Specify address as "0x07". No data read or write. During standby, the detection circuit is set to disable. Status for angular rate data and temperature sensor data is "0". Conduct the sleep-out command in Section 7.6 to disable standby mode.

However, you cannot transition from sleep mode to standby mode.

7.8. Temperature Sensor Data Read

Specify address as "0x08". Only data read (no data write). Refer to Section 6.6 regarding the temperature sensor data read function.

7.9. Software Reset

Specify address as "0x09". No data read or write. The user command register indicated in Table 7.1 is reset (set to the default value).

7.10. Angular Rate Data Read

Specify address as "0x0a". Only data read (no data write). Refer to Section 6.5 regarding the angular rate data read function.

7.11. Angular Rate Data Read Control

Table 7.6. Angular Rate Data Read Control

Address	Bit	Register	Default	R/W	Function	Settings
0x0b	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R/W	Reserved	Reserved
	4	Reserved	0	R/W	Reserved	Reserved
	3	Reserved	0	R/W	Reserved	Reserved
	2	DataFormat	0	R/W	Angular rate data format	0: 16 bits output 1: 24 bits output
	1	Reserved	0	R/W	Reserved	Reserved
	0	Reserved	1	R/W	Reserved	Reserved

(Note) Reserved resister must not be changed. Use the default settings.

7.12. Zero rate level calibration command

Specify address as "0x0c". Data cannot be read or written. Zero rate level calibration is carried out at the moment command initiated. To issue this command, enable register EnCalibCmd indicated in Table 7.4. To disable the calibration value, disable register EnCalibCmd indicated in Table 7.4.

7.13. Temperature Sensor Data Format

Table 7.7. Temperature Sensor Data Format

Address	Bit	Register	Default	R/W	Function	Settings
0x1c	7	Reserved	0	R	Reserved	Reserved
	6	TsDataFormat [1]	1	R/W	Temperature sensor data format	TsDataFormat [1:0] 00: 8 bits output 01: 10 bits output 10: 12 bits output 11: Not Available
	5	TsDataFormat [0]	0	R/W		
	4	Reserved	0	R/W	Reserved	Reserved
	3	SelMISO [1]	1	R/W	MISO/SA0 terminal status selection	(Note 2)
	2	SelMISO [0]	0	R/W		
	1	Reserved	1	R/W	Reserved	Reserved
	0	Reserved	1	R/W	Reserved	Reserved

(Note 1) Reserved resister must not be changed. Use the default settings.

(Note 2) Refer to Section 6.7 indicated in Chapter 6 for details on settings.

7.14. Serial Interface Settings

Table 7.8. Serial Interface Settings

Address	Bit	Register	Default	R/W	Function	Settings
0x1f	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	SPISel (Note 1)	0	R/W	4-wire/3-wire SPI select	0: 4-wire SPI, 1: 3-wire SPI
	0	I^2C_EN (Note 1)	1	R/W	I^2C enable	0: Disable, 1: Enable

(Note 1) The mode indicated in Table 7.8 can be changed only by SPI communication.

(Note 2) Reserved resister must not be changed. Use the default settings.

(Note 3) Register settings are not set when the multi-slave function is enabled via factory settings.

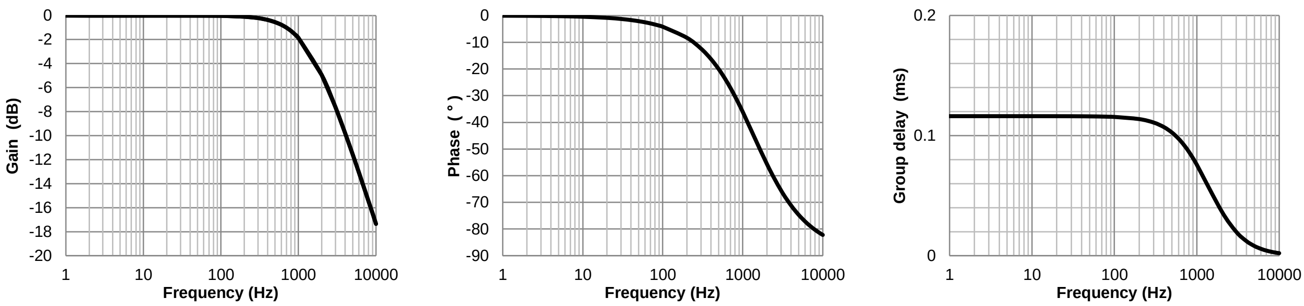
8. Filter Characteristics

8.1. Analog Filter

The analog low-pass filter (LPF) with 1st order characteristic indicated in Figure 1.2 is shown in Table 8.1.

Table 8.1. Analog LPF

Parameter	Condition	Min.	Typ.	Max.	Unit
Cut-off frequency	At phase delay 45 °	-	1370	-	Hz
Phase delay	Phase delay angle at 10 Hz	-	-0.42	-	°



(a) Gain (b) Phase (c) Group delay

Figure 8.1 Filter characteristics of the analog LPF

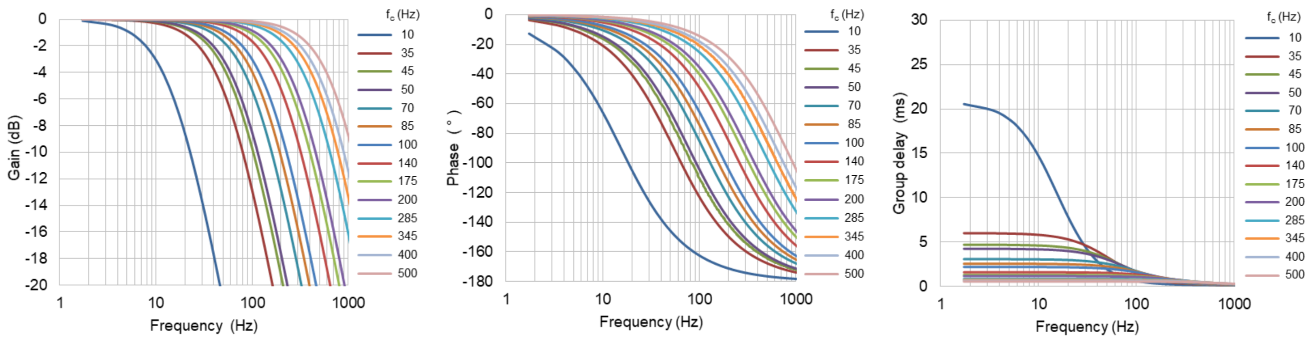
8.2. Digital Filter

8.2.1. Selectable Digital Low-Pass Filter (LPF)

The typical characteristic values of the selectable digital LPF are shown in Table 8.2, and the filter characteristics are shown in Figure 8.2 to Figure 8.4. The digital LPF has selectable filter orders (2nd, 3rd and 4th order) and cutoff frequencies (10 Hz to 500 Hz, 14 steps). See Section 7.2 for the setting instructions. For more details on the filter characteristics, please contact us.

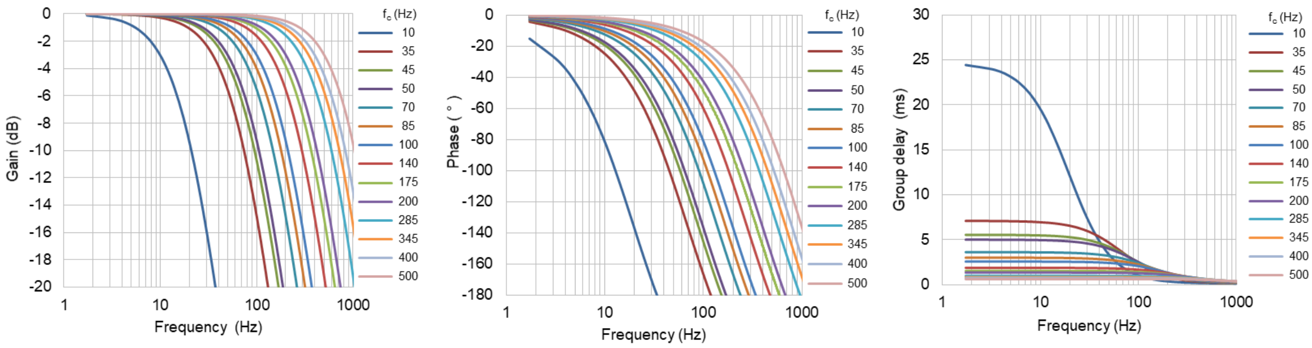
Table 8.2. Selectable Digital LPF

Parameter	Condition		Typ.			Unit
	LpfFc [3:0]	f_c	2nd order	3rd order	4th order	
Phase @ 10 Hz	0000	10 Hz	-67.3	-83.2	-96.6	°
	0001	35 Hz	-21.4	-25.5	-29.1	°
	0010	45 Hz	-16.7	-19.8	-22.6	°
	0011	50 Hz	-15.0	-17.9	-20.4	°
	0100	70 Hz	-10.8	-12.8	-14.5	°
	0101	85 Hz	-8.9	-10.5	-12.0	°
	0110	100 Hz	-7.6	-9.0	-10.2	°
	0111	140 Hz	-5.4	-6.4	-7.3	°
	1000	175 Hz	-4.3	-5.1	-5.8	°
	1001	200 Hz	-3.8	-4.5	-5.1	°
	1010	285 Hz	-2.6	-3.1	-3.6	°
	1011	345 Hz	-2.2	-2.6	-2.9	°
	1100	400 Hz	-1.9	-2.2	-2.5	°
	1101	500 Hz	-1.5	-1.8	-2.0	°
Group delay @ DC	0000	10 Hz	20.9	24.7	28.1	ms
	0001	35 Hz	6.0	7.1	8.1	ms
	0010	45 Hz	4.7	5.6	6.3	ms
	0011	50 Hz	4.2	5.0	5.7	ms
	0100	70 Hz	3.1	3.6	4.1	ms
	0101	85 Hz	2.6	3.0	3.4	ms
	0110	100 Hz	2.2	2.6	2.9	ms
	0111	140 Hz	1.6	1.9	2.1	ms
	1000	175 Hz	1.3	1.5	1.7	ms
	1001	200 Hz	1.2	1.4	1.5	ms
	1010	285 Hz	0.9	1.0	1.1	ms
	1011	345 Hz	0.7	0.8	0.9	ms
	1100	400 Hz	0.6	0.7	0.8	ms
	1101	500 Hz	0.5	0.6	0.7	ms



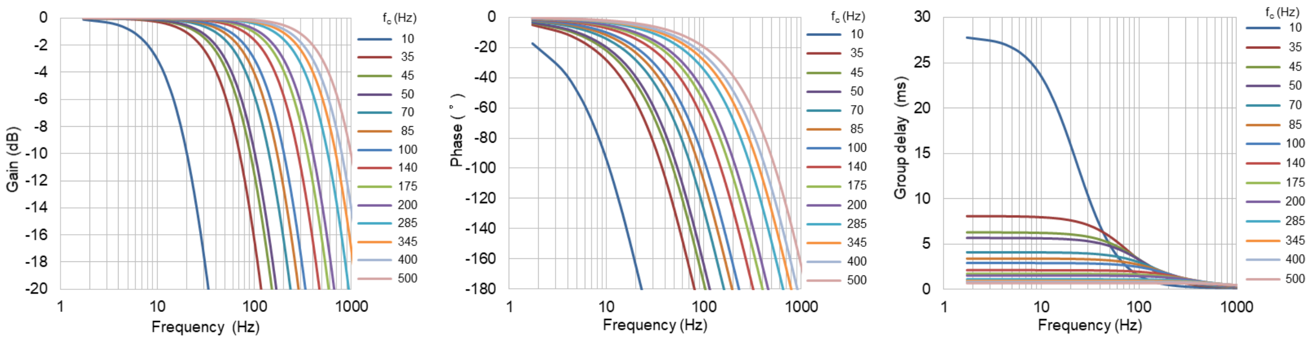
(a) Gain (b) Phase (c) Group delay

Figure 8.2 Filter characteristics of the selectable digital LPF (2nd order)



(a) Gain (b) Phase (c) Group delay

Figure 8.3 Filter characteristics of the selectable digital LPF (3rd order)



(a) Gain (b) Phase (c) Group delay

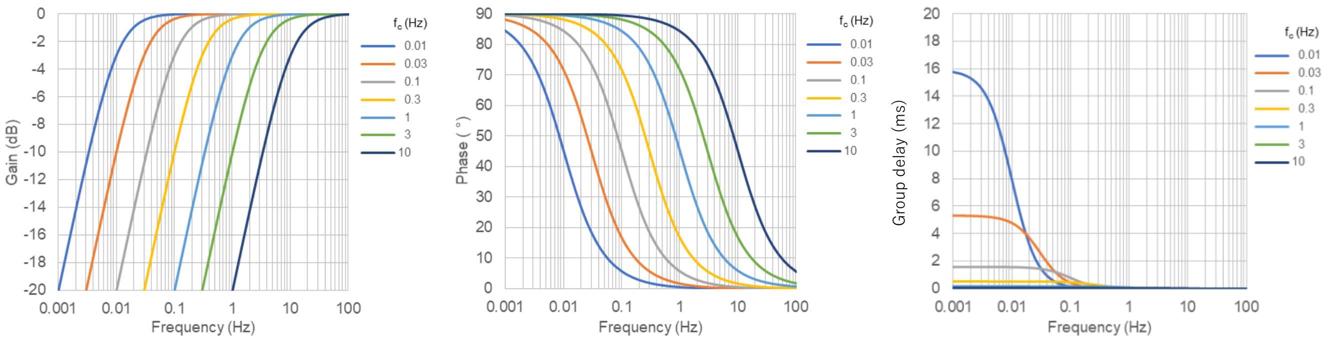
Figure 8.4 Filter characteristics of the selectable digital LPF (4th order)

8.2.2. Selectable Digital High-Pass Filter (HPF)

The typical characteristic values of the selectable digital HPF are shown in Table 8.3, and the filter characteristics are shown in Figure 8.5. The digital HPF has cutoff frequencies (0.01 Hz to 10 Hz, 7 steps). See Section 7.1 for the setting instructions. For more details on the filter characteristics, please contact us.

Table 8.3. Selectable Digital HPF

Parameter	Condition		Typ.	Unit
	HpfFc [2:0]	f_c	1st order	
Phase@ 10 Hz	000	0.01 Hz	0.1	°
	001	0.03 Hz	0.2	°
	010	0.1 Hz	0.6	°
	011	0.3 Hz	1.7	°
	100	1 Hz	5.7	°
	101	3 Hz	16.7	°
	110	10 Hz	45.0	°
Group delay @ 10 Hz	000	0.01 Hz	0.02	ms
	001	0.03 Hz	0.05	ms
	010	0.1 Hz	0.16	ms
	011	0.3 Hz	0.47	ms
	100	1 Hz	1.56	ms
	101	3 Hz	4.35	ms
	110	10 Hz	7.92	ms



(a) Gain **(b) Phase** **(c) Group delay**

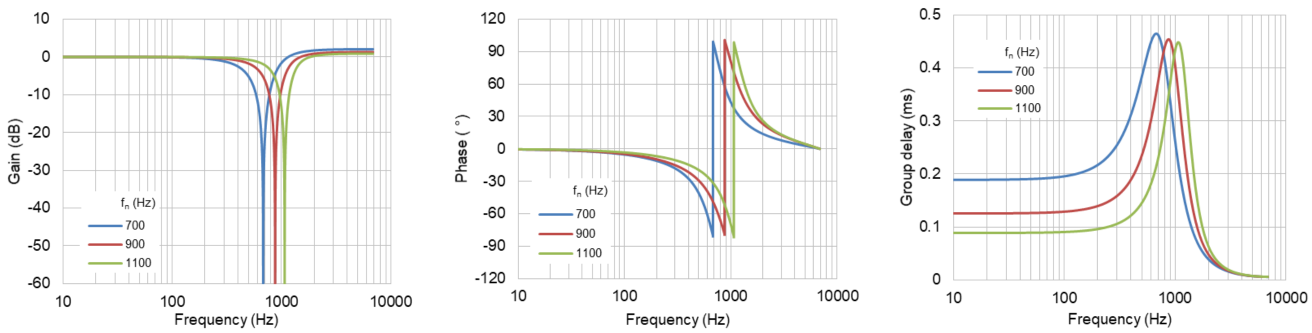
Figure 8.5 Filter characteristics of the selectable digital HPF (2nd order)

8.2.3. Notch Filter (NF)

The notch filter is used to remove the detuned frequency component (see section 12.3). The typical characteristic values of the filter are shown in Table 8.4, and the filter characteristics are shown in Figure 8.6. Please refer to Section 7.2 for the setting instructions. For more details on the filter characteristics, please contact us. The center frequency f_n (700 Hz to 1100 Hz) of the filter is set at the factory individually, and it cannot be changed. It is possible to select whether enable or disable the notch filter.

Table 8.4. Notch filter NF

Parameter	Condition f_n	Typ.	Unit
Phase @ 10 Hz	700 Hz	-0.52	°
	900 Hz	-0.47	°
	1100 Hz	-0.33	°
Group delay @ 10 Hz	700 Hz	0.19	ms
	900 Hz	0.13	ms
	1100 Hz	0.09	ms



(a) Gain (b) Phase (c) Group delay

Figure 8.6 Filter characteristics of the Notch filter

9. Connection Diagrams

If serial communications in each SPI cannot be used due to the characteristic impedance of the board, it may be possible to use it by connecting a damping resistor in series to the MOSI path and SCLK path.

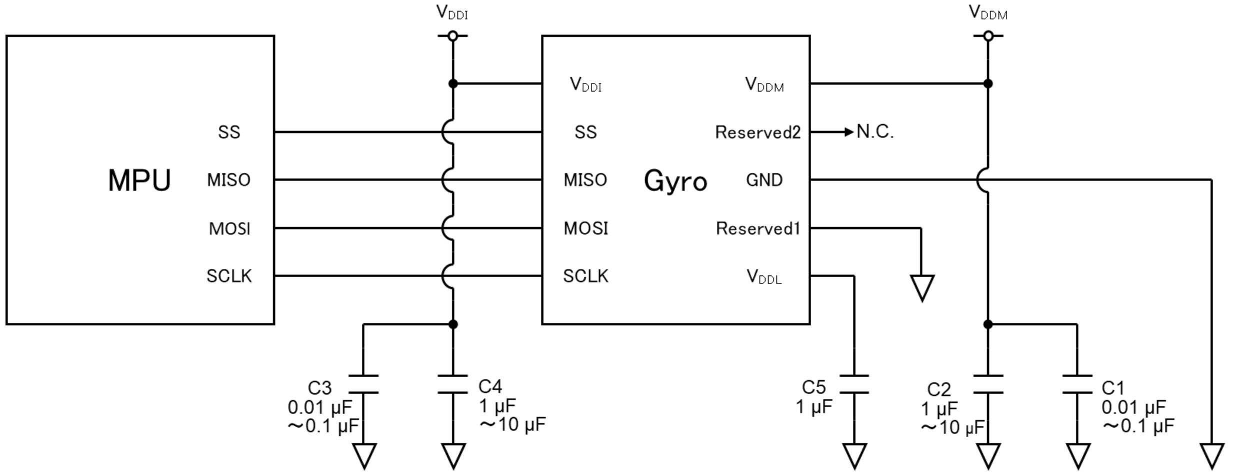


Figure 9.1. Example of 4-Wire SPI Connection

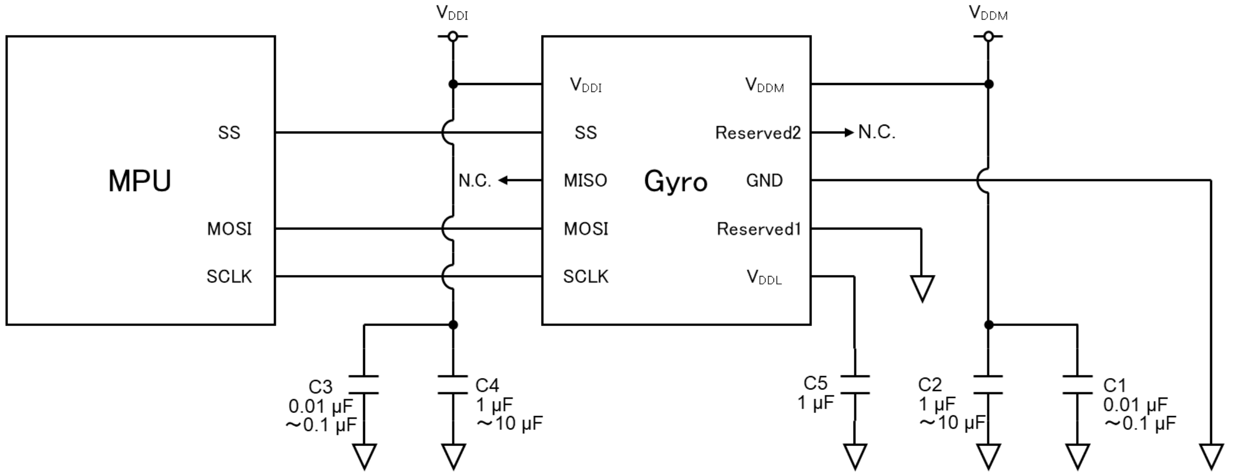


Figure 9.2. Example of 3-Wire SPI Connection

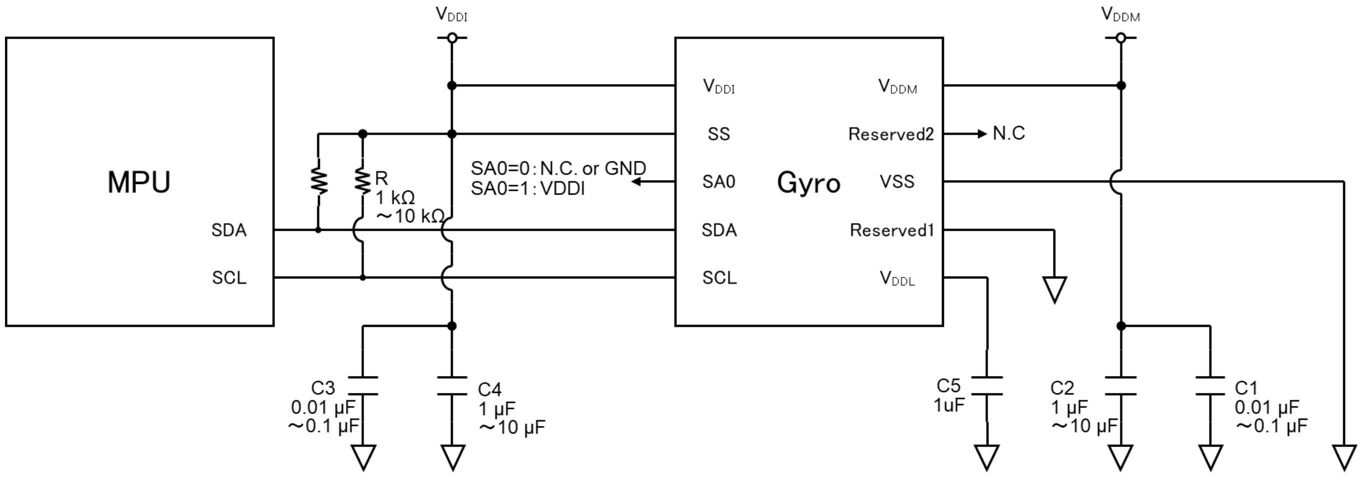


Figure 9.3. Example of I^2C Connection

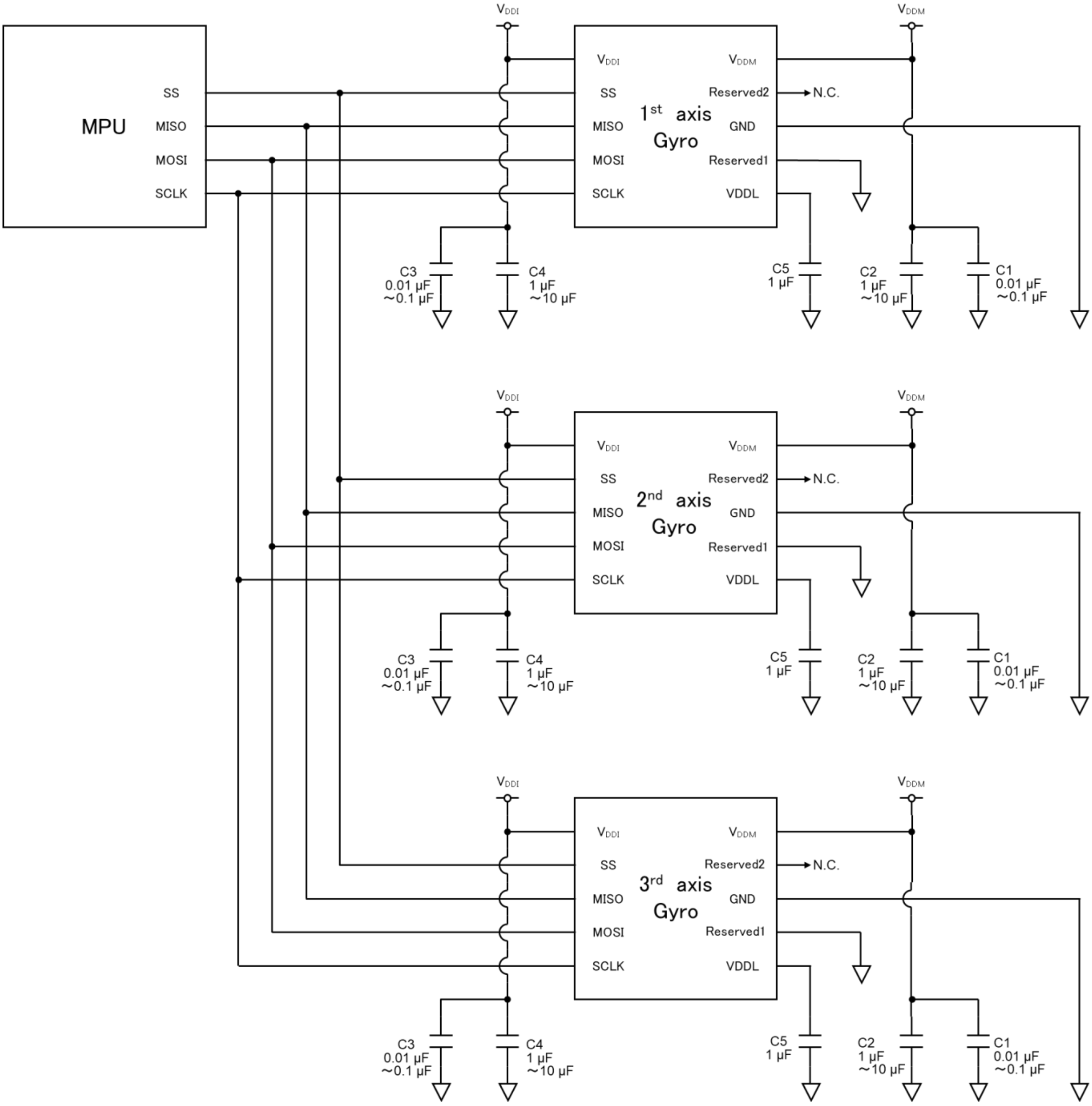


Figure 9.4. Example of 4-Wire SPI with Multi-Slave Connection

10. Other Information

10.1. Moisture Sensitivity Level (MSL)

Table 10.1. MSL

Parameter	Level	Standard
MSL	1	JEDEC J-SD-020D.01

10.2. Electro-Static Discharge (ESD)

Table 10.2. ESD

Model	Min.	Standard & Condition
HBM	2000 V	JESD22-A114, V_{DDM}, V_{DDI} and GND reference, 3 times
MM	200 V	JESD22-A115, V_{DDM}, V_{DDI} and GND reference, 1 time

10.3. Soldering Profile

A solder heat resistance of this product was verified under the air reflow soldering profile (JEDEC J-STD-020D.1) shown in Figure 10.1.

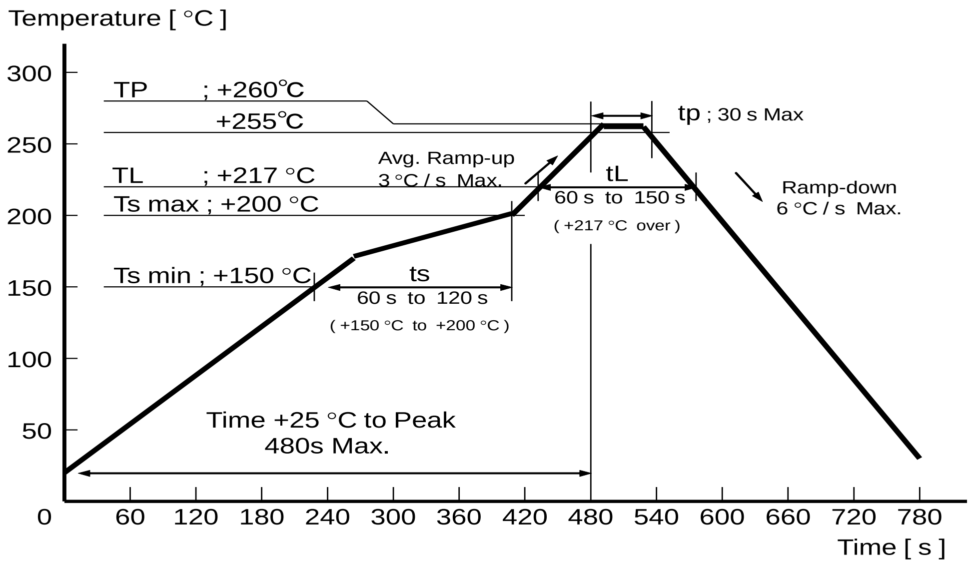


Figure 10.1. Soldering Profile

11. Taping Information

11.1. Taping Quantity

The standard quantity in a reel is 2000 pcs.

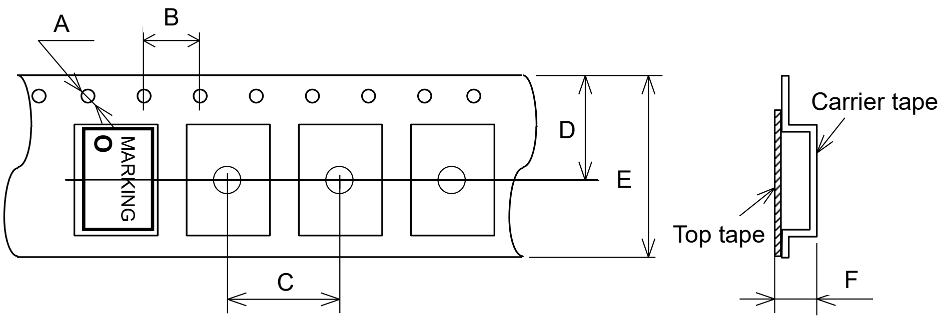
11.2. Taping Specification

Subject to EIA-481, IEC 60286, JIS C0806

Table 11.1. Tape and Reel Materials

Item	Material
Carrier tape	Black conductive PS (Polystyrene)
Top tape	Antistatic PET (Polyethylene terephthalate)
Reel	Black conductive PS

11.3. Taping Dimensions

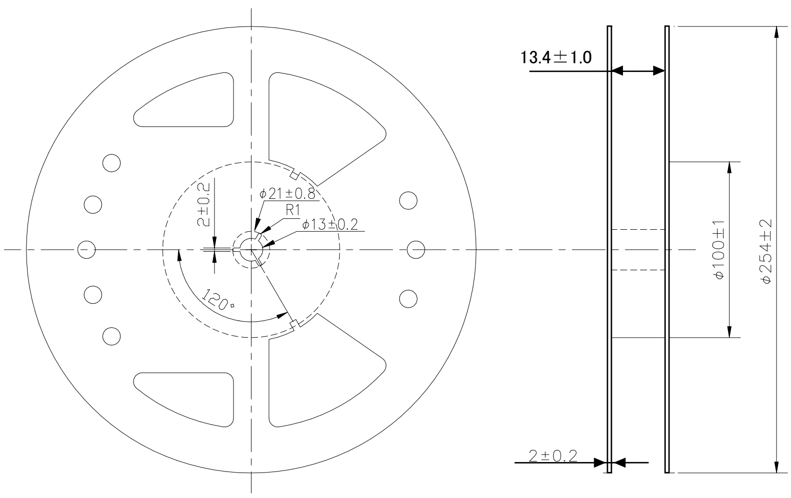


Unit: mm

Symbol	A	B	C	D	E	F
Value	φ1.5	4.0	8.0	7.25	12.0	2.1

Figure 11.1. Tape Dimensions

11.4. Reel Dimensions



Unit: mm

Figure 11.2. Reel Dimensions

12. Terminology

12.1. Cross Axis Sensitivity

The value is derived by dividing sensitivity around the X and Y axis by the sensitivity around the Z axis. The X, Y, and Z axis directions are as shown in Figure 12.1.

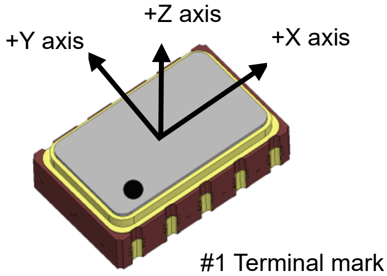


Figure 12.1. Each Axis Direction

12.2. Drive Frequency

The drive frequency is the resonance frequency (drive mode) of the sensor element continuously vibrated to gain the Coriolis force.

12.3. Detuning Frequency

The detuning frequency is the natural frequency used for the mechanical-electrical transduction of the Coriolis force. It is the difference from the drive frequency.

13. Handling Precaution

Crystal devices are high precision products. Use the following precautions during handling.

1. The detuning frequency for this product is 900 Hz ± 200 Hz. During board design, the customer must ensure that the board resonance frequency is not within the vicinity of this detuning frequency. When mounting on a board, align the sensor near a board loading component with low resonance variation.
2. Excessive shock from adsorption/chucking when mounting the sensor or excessive vibration or shock during board cutting or an impact wrench after mounting can result in damage to the sensor or the deterioration of sensor properties. Establish conditions that avoid vibration or shock to the sensor to ensure there is not loss in performance.
3. To detect angular rate, this product uses a drive frequency to drive the sensor element. External application of a signal with frequency components in the vicinity of the drive frequency or high-order harmonics can result in fluctuations in angular rate output by the sensor. Be sure to confirm internally in advance concerning power supply decoupling measures and serial interface communications frequency settings.
4. To prevent malfunctions caused by electromagnetic induction and static induction from other signal lines, during pattern design do not pass other signal lines near the sensor or along the back of the package. Also, use a pattern design that does not cross with other signal lines.
5. It may occur communication error with the device due to the signal pattern of board. In that case, please connect dumping resistor to reduce noise/overshoot/undershoot of the signal.
6. Confirm internally in advance concerning measures for vibration, shock, and noise.
7. This product design incorporates shock resistance but there is the risk of product damage due to drops and shock. **Do not use this product if it has been dropped as we cannot guarantee product performance.**
8. Applying ultrasonic vibration during ultrasonic washing can cause resonance damage to the crystal unit depending on usage conditions. As we cannot specify the usage conditions (washer type, power, time, tub position, etc.) at your company, we offer no guarantees concerning operability after the application of ultrasonic vibration. Confirm internally prior to use if the use of ultrasonic washing is required.
9. Prior to use, conduct mounting tests internally to confirm there is no impact on performance. Similarly, confirm prior to changing any conditions. During and after mounting, ensure that the sensor is not in contact with boards or structural elements.
10. The sensor includes a static electricity protection circuit, but application of significant static electricity can result in damage to the sensor's internal IC. Make sure to use conductive materials for packaging and transport containers as well. For the soldering iron, measurement circuit, etc., use products with no high-voltage leaks and during mounting make sure to employ static electricity measures such as the use of a ground wire.
11. Keep reflow to no more than three times. Use a soldering iron to correct any soldering mistakes. Here, the temperature of the iron type should be below +350 °C and less than 3 seconds. (Blower use not allowed)
12. We recommend using board production based on Epson pad dimensions.
13. This product has the same frequency noise as drive frequency. Remove using an appropriate filter circuit.
14. This product is designed to resist acoustic interference even when multiple sensors are operated in close proximity but impedance common to board resonance and power supply could result in mechanical or electrical interference. Confirm internally prior to use.
15. This product includes a POR circuit. To avoid the POR circuit malfunctions, power supply voltage rise should be conducted between 0.01 ms and 100 ms.
16. Do not use in high condensation or other environments prone to short circuits between terminals.
17. Using the drive frequency integral multiplier as communications clock may result in fluctuations in the angular rate output.
18. Acquiring angular rate data as a frequency that is a fraction of the integer for the drive frequency can result in fluctuations in the angular rate output.

14. Contact

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