

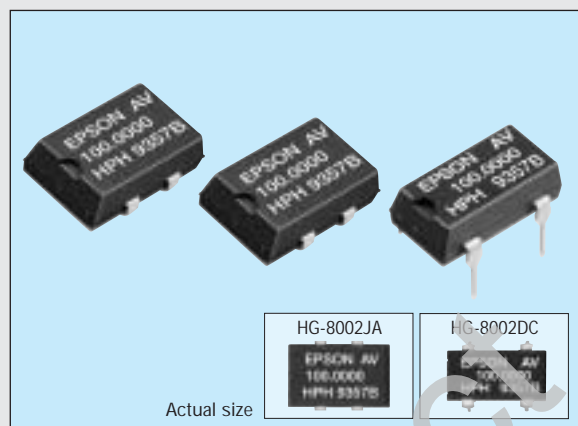
PROGRAMMABLE HIGH-STABILITY HIGH-FREQUENCY CRYSTAL OSCILLATOR

HG-8002JA/DC series

Product number (please refer to page 2)

Q3502JAxxxxxx00
Q3402DCxxxxxx00

- Wide frequency output by PLL technology.
- Low current consumption by output enable function (OE) or standby function (ST)
- Pin compatible with half-size oscillator SG-531.
- Package and pin compatible with SG-615.
- Low current consumption due to CMOS technology.
- Excellent environmental capability.



Specifications (characteristics)

Item	Symbol	Specifications *2			Remarks
		PT/ST	PH/SH	PC/SC	
Output frequency range	f_o	1.0000 MHz to 125.0000 MHz			Refer to page 33. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD-GND} -0.5 V to +7.0 V			
	Operating voltage	V_{DD}	$5.0 V \pm 0.25 V$	$3.3 V \pm 0.165 V$	
Temperature range	Storage temperature	T_{STG} -55 °C to +125 °C			Stored as bare product after unpacking
	Operating temperature	T_{OPR} -20 °C to +70 °C (-40 °C to +85 °C)			Refer to page 33. "Frequency range"
Frequency stability	$\Delta f/f_o$	AV: $\pm 20 \times 10^{-6}$ BV: $\pm 25 \times 10^{-6}$ CX: $\pm 30 \times 10^{-6}$			AV, BV: -20 °C to +70 °C, CX: -40 °C to +85 °C
Current consumption	I_{OP}	45 mA Max.		28 mA Max.	No load condition, Max. frequency range
Output disable current	I_{OE}	30 mA Max.		16 mA Max.	OE=GND(PT, PH, PC)
Standby current	I_{ST}	50 μ A Max.			\overline{ST} =GND(ST, SH, SC)
Duty *1	tw/t	—		40 % to 60 %	CMOS load: 1/2 V_{DD} level, Max. load condition
		40 % to 60 %		—	TTL load: 1.4 V level, Max. load condition
High output voltage	V_{OH}	$V_{DD} - 0.4 V$ Min.			$I_{OH} = -16 mA$ (PT/ST, PH/SH), $-8 mA$ (PC/SC)
Low output voltage	V_{OL}	0.4 V Max.			$I_{OL} = 16 mA$ (PT/ST, PH/SH), $8 mA$ (PC/SC)
Output load *1 condition (fan out)	TTL	N		2 TTL Max.	Max. frequency and Max. operating voltage range
	CMOS	CL		15 pF Max.	
Output enable/disable input voltage	V_{IH}	2.0 V Min.		0.7 x V_{DD} Min.	\overline{ST} , OE terminal
	V_{IL}	0.8 V Max.		0.2 x V_{DD} Max.	
Output rise time *1	CMOS level	t_{TLH}		3 ns Max.	CMOS load: 20 % \rightarrow 80 % V_{DD} level
	TTL level	4 ns Max.		—	TTL load: 0.4 V \rightarrow 2.4 V level
Output fall time *1	CMOS level	t_{THL}		3 ns Max.	CMOS load: 80 % \rightarrow 20 % V_{DD} level
	TTL level	4 ns Max.		—	TTL load: 2.4 V \rightarrow 0.4 V level
Oscillation start up time	t_{OSC}	10 ms Max.			Time at minimum operating voltage to be 0 s
Aging	f_a	$\pm 2 \times 10^{-9}$ /year Max.			$T_a = +25$ °C, $V_{DD} = 5.0 V/3.3 V$ (PC/SC)
Shock resistance	S.R.	$\pm 2 \times 10^{-6}$ Max.			Three drops on a hard board from 750 mm or excitation test with 29400 m/s ² x 0.3 ms x 1/2sine wave in 3 directions

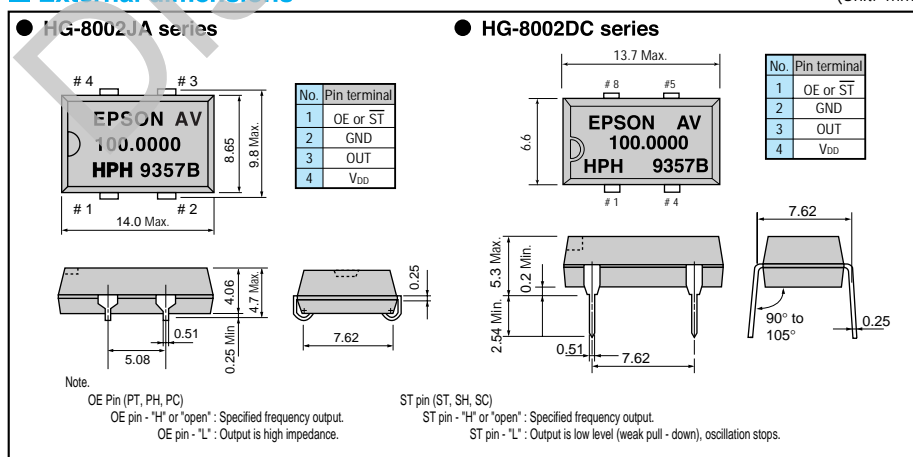
*1 Operating temperature(-40 °C to +85 °C), the available frequency, duty and output load conditions, please refer to page 33.

*2 PLL - PLL connection & Jitter specification, please refer to page 53, 54.

Checking possible by the Frequency Checking Program.

External dimensions

(Unit: mm)



Recommended soldering pattern (Unit: mm)

