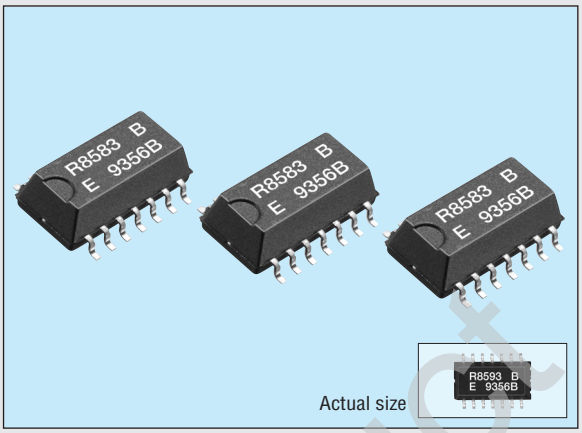
I² C-BUS COMPATIBLE REAL TIME CLOCK MODULE

RTC-8583/8593 series

- Built-in crystal unit. Adjustment free with 10 pF external capacitor.
- Small package (SOP 14-pin).
- Three mode operations: internal crystal oscillation, external 50 Hz clock and event counter.
- I²C-Bus interface compatible.
- Builtin 240 x 8 bit S-RAM available (RTC8583).
- Alarm and timer functions available.
- Wide operating voltage range 2.5 V to 6.0 V.
- Wide data hold voltage range 1.0 V to 6.0 V.
- Low current consumption (RTC8593, 1.0 µA typical).



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V_{DD}	V_{DD}-GND	-0.8	+7.0	V
Input voltage	V_{IN}			V_{DD}+0.8	
Input current	Ii			10	mA
Output current	Io				
Storage temperature	T_{STG}		-55	+125	°C

Operating range

Item	Symbol	Condition	Min.	Max.	Unit
Operating voltage	V_{DD}		2.5	6.0	V
Data holding voltage	V_{CLK}		1.0		
Operating temperature	T_{OPR}		-30	+70	°C
External capacitor	C_G		10±5 %		pF

Frequency characteristics

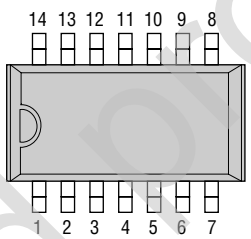
Item	Symbol	Condition	Max.	Unit
Frequency tolerance	Δf/fo	Ta=+25 °C, V_{DD}=5 V	A: 5±20 B: 5±50	x 10^{-6}
Frequency temperature characteristics	T_{op}	Ta=-10 °C to +70 °C, V_{DD}=5 V	+10 -120	
Frequency voltage characteristics	fv	Ta=+25 °C, V_{DD}=2.0 to 6.0 V	±3	
Oscillation start-up time	t_{OSC}	Ta=+25 °C, V_{DD}=5 V	3	s
Aging	fa	Ta=+25 °C, V_{DD}=5 V first year	±5	x 10^{-6}/year

DC characteristics

Item		Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage		SDA	V_{IH}	—	0.7V_{DD}		V_{DD}+0.8	V
"L" input voltage			V_{IL}		-0.8		0.3	
"L" output current			I_{OL}	V_{OL}=0.4 V	3			mA
Input leak current			I_L	V_{IN}=V_{DD} or GND			1	µA
Leak current		Ao RESET OSC1					250	nA
Output current		INT	I_{OL}	V_{OL}=0.4 V	1			mA
Leak current		INT SCL	I_L	V_{IN}=V_{DD} or GND			1	µA
Source current (access)			I_{DD0}	f_{SCL}=100 kHz			200	
Current Consumption (non access)	8583 1		I_{DD1}	V_{DD}=5 V, f_{SCL}=0 Hz		10	50	
	8583 2		I_{DD2}	V_{DD}=3 V, f_{SCL}=0 Hz		3.5	15	
	8583 3		I_{DD3}	V_{DD}=2 V, f_{SCL}=0 Hz		2.0	10	
	8593 1		I_{DD1}	V_{DD}=5 V, f_{SCL}=0 Hz		3.0	15	
	8593 2		I_{DD2}	V_{DD}=3 V, f_{SCL}=0 Hz		1.2	10	
	8593 3		I_{DD3}	V_{DD}=2 V, f_{SCL}=0 Hz		1.0	8	

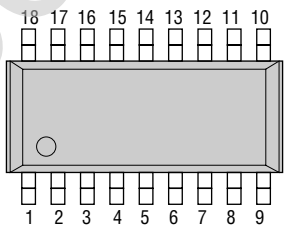
Terminal connection

● **RTC-8583/8593**



No.	8583	8593	8593SB
1	GND1	N.C	N.C
2	SCL	SCL	N.C
3	SDA	SDA	N.C
4	N.C	N.C	N.C
5	GND	GND	N.C
6	N.C	N.C	N.C
7	A0	RESET	N.C
8	OSC1	OSC1	RESET
9	N.C	N.C	GND
10	N.C	N.C	SDA
11	V_{DD}	V_{DD}	SCL
12	N.C	N.C	INT
13	N.C	N.C	V_{DD}
14	INT	INT	OSC1
15			N.C
16			N.C
17			N.C
18			N.C

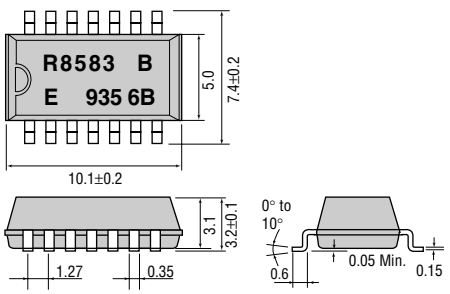
● **RTC-8593SB**



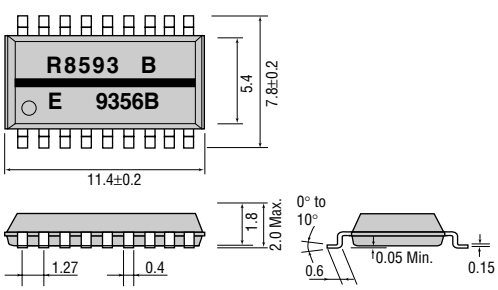
External dimensions

(Unit: mm)

● **RTC-8583/8593** (SOP 14-pin)



● **RTC-8593SB** (SOP 18-pin)



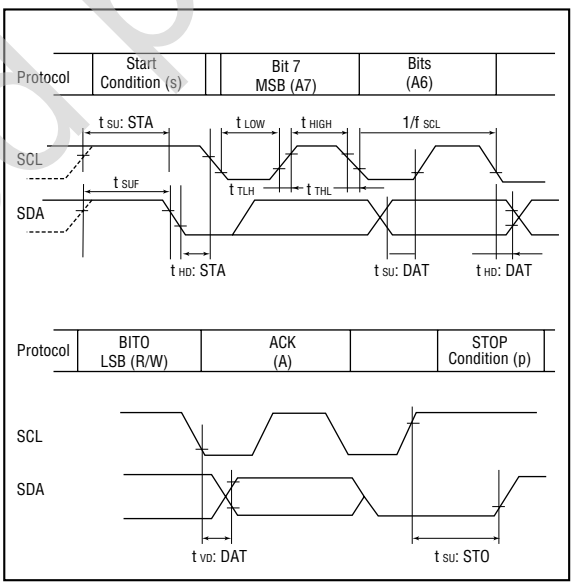
Register table

Address	Register name	count	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	CNT		STOP	HOLD	MODE1	MODE2	MASK	ALM	AF	TF
01	1/100SEC	0 to 99	8/10	4/10	2/10	1/10	8/100	4/100	2/100	1/100
02	SEC	0 to 59	10S8	10S4	10S2	10S1	S8	S4	S2	S1
03	MIN	0 to 59	10MIN8	10MIN4	10MIN2	10MIN1	MIN8	MIN4	MIN2	MIN1
04	HOUR	0 to 23	12/24	AM/PM	10HOUR2	10HOUR1	HOUR8	HOUR4	HOUR2	HOUR1
05	DAY	0 to 31	YEAR2	YEAR1	10DAY2	10DAY1	DAY8	DAY4	DAY2	DAY1
06	MONTH	0 to 12	W4	W2	W1	10MONTH1	MONTH8	MONTH4	MONTH2	MONTH1
07	TIMER	0 to 99	10TIMER8	10TIMER4	10TIMER2	10TIMER1	TIMER8	TIMER4	TIMER2	TIMER1
08	ALARM		AIE	TAIE	AS1	AS0	TIE	TCP2	TCP1	TCP0
09	A-1/100	0 to 99	A-8/10	A-4/10	A-2/10	A-1/10	A-8/100	A-4/100	A-2/100	A-1/100
0A	A-SEC	0 to 59	10A-SEC8	10A-SEC4	10A-SEC2	10A-SEC1	10A-SEC8	10A-SEC4	10A-SEC2	10A-SEC1
0B	A-MIN	0 to 59	10A-MIN8	10A-MIN4	10A-MIN2	10A-MIN1	10A-MIN8	10A-MIN4	10A-MIN2	10A-MIN1
0C	A-HR	0 to 23	A-12/24	A-AM/PM	10A-HR2	10A-HR1	A-HR8	A-HR4	A-HR2	A-HR1
0D	A-DAY	0 to 31	—		A-DAY2	A-DAY1	A-DAY8	A-DAY4	A-DAY2	A-DAY1
0E	A-MON	0 to 12	—			10A-MON1	10A-MON8	10A-MON4	10A-MON2	10A-MON1
0F	A-TIM	0 to 99	10A-TIM8	10A-TIM4	10A-TIM2	10A-TIM1	A-TIM8	A-TIM4	A-TIM2	A-TIM1
10 to FF		0 to FF	User's RAM (RTC-8583 is available)							

Switching characteristics

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	—	100	kHz
Spike tolerance on bus	t_{SW}			ns
Bus free time	t_{BUF}	4.7	—	μs
Start condition set-up time	$t_{SU;\ STA}$			
Hold time	$t_{HD;\ STA}$	4.0		
SCL "L" time	t_{LOW}	4.7		
SCL "H" time	t_{HIGH}	4.0		
SCL, SDA rise time	t_{TLH}	—	1.0	
SCL, SDA fall time	t_{THL}		0.3	
Date set-up time	$t_{SU;\ DAT}$	250	—	ns
Date hold time	$t_{HD;\ DAT}$	0		
SCL low to data out valid	$t_{VD;\ DAT}$	—	3.4	μs
Stop condition set-up time	$t_{SU;\ STO}$	4.0	—	
Event counter frequency	fi	—	1.0	MHz

Timing chart



Block diagram