

## **CRYSTAL OSCILLATOR (SPXO)**

**OUTPUT: HCSL** 





**Product Number** SG2016HGN:X1G006221xxxx15 SG2520HGN:X1G005891xxxx15

## **SG2016HGN / SG2520HGN**

25 MHz to 500 MHz •Frequency range Supply voltage 2.5 V Typ. / 3.3 V Typ. •Frequency tolerance  $\pm 25 \times 10^{-6}, \pm 50 \times 10^{-6}$ 

-40 °C to +85 °C, -40 °C to +105 °C •Operating temperature range Function Output enable (OE) or Standby (ST)

Phase jitter 90 fs Max.

 $(100 \text{ MHz} < \text{fo} \le 156 \text{ MHz}, V_{CC} = 2.5 \text{ V}, 3.3 \text{ V})$ 



SG2016HGN SG2520HGN

 $(2.0 \times 1.6 \times 0.63 \text{ mm})$ 

## $(2.5 \times 2.0 \times 0.74 \text{ mm})$

# PCle Gen5,6 Jitter specification compliant. Specifications (characteristics)

Item	Symbol	Specifications	Condition	s / Remarks
Output frequency range	frequency range fo 25 MHz to 500 MHz Please contact us for available frequenc		able frequencies.	
Supply voltage V <sub>CC</sub> D: 2.5 V ± 5 %, C: 3.3 V ± 5 %				
Storage temperature range				
Operating temperature range	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C		
Frequency tolerance	f_tol	D: ±25 × 10 <sup>-6</sup> Max. J: ±50 × 10 <sup>-6</sup> Max.	Includes initial frequency to temperature characteristics coefficient and 10 years ag	s, frequency / voltage
Current consumption	Icc	35 mA Max. 40 mA Max.	25 MHz ≤ fo < 212 MHz 212 MHz ≤ fo < 500 MHz	OE or $\overline{ST}$ = V <sub>CC</sub> , L_HCSL = 50 $\Omega$
Disable current	I dis	25 mA Max.	OE = GND	1
		30 μA Max.	ST = GND, T use Max. = +	-85 °C
Stand-by current	I_std	60 µA Max.	ST = GND, T use Max. = +	-105 °C
Symmetry	SYM	45 % to 55 %	At output crossing point	
		0.5 V to 0.7 V	25 MHz ≤ fo < 212 MHz	0
	.,	0.4 V to 0.65 V	212 MHz ≤ fo < 500 MHz	Output option: A
Output voltage	V <sub>OH</sub>	0.6 V to 0.8 V	25 MHz ≤ fo < 212 MHz	
	-	0.5 V to 0.75 V	212 MHz ≤ fo < 500 MHz	Output option: B
	VoL	-0.15 V to +0.15 V		1
D.W	Vsw	0.7 V to 1.4 V	Output option: A	
Differential swing		0.8 V to 1.6 V	Output option: B	
Crossing voltage	VcR	0.25 V to 0.55 V		
Rise time / Fall time	tr/tf	0.7 ns Max.	20 % - 80 % (V <sub>OH</sub> - V <sub>OL</sub> )	
Differential output rise slew rate / fall slew rate	Rr/Rf	2 V/ns to 10 V/ns	Between -0.15 V and 0.15 V of differential output	
Output load condition	L_HCSL	50 Ω		
Innut valtage	V <sub>IH</sub>	70 % V <sub>CC</sub> Min.	OE or ST terminal	
Input voltage	VIL	30 % V <sub>CC</sub> Max.	OE or ST terminal	
Output enable time	tsta_oe	500 ns Max.	t = 0 at OE = 70 % V <sub>CC</sub>	
Output enable time	tsta_st	10 ms Max.	t = 0 at <del>S</del> T = 70 % V <sub>CC</sub>	
Output dia abla tima	tstp_oe	100 ns Max.	t = 0 at OE = 30 % V <sub>CC</sub>	
Output disable time	tstp_st	100 ns Max.	t = 0 at <del>S</del> <del>T</del> = 30 % V <sub>CC</sub>	
Start-up time	t_str	10 ms Max.	t = 0 at 90 % V <sub>CC</sub>	
	t <sub>PJ</sub>	200 fs Max.	25 MHz ≤ fo < 100 MHz	Offset frequency
		90 fs Max.	100 MHz ≤ fo ≤ 156 MHz	fo < 50 MHz:
Phase jitter		70 fs Max.	156 MHz < fo ≤ 212 MHz	12 kHz to 5 MHz
		60 fs Max.	212 MHz < fo ≤ 391 MHz	fo ≥ 50 MHz:
		50 fs Max.	391 MHz < fo ≤ 500 MHz	12 kHz to 20 MHz
Jitter	t <sub>c-c</sub>	60 ps Max.	Cycle to cycle jitter (Peak to	o Peak)
PCIe jitter limits		0.1 ps Max.	For PCIe Gen5	
for CC architecture	-	0.06 ps Max.	For PCIe Gen6	

### Product name

**Product Name** (Standard form) a: Model b: Output (H: HCSL) c: Frequency d: Supply voltage e: Frequency tolerance

f: Operating temperature g: Function h: Output disable type (Z: High impedance) i: Output option

d: Supply voltage	
C 3.3 V Typ.	
D 2.5 V Typ.	

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Γ	e: Freq. tolerance		
Γ	D	±25 × 10 <sup>-6</sup>	
Γ	J	±50 × 10 <sup>-6</sup>	

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	f: Operating temp.			
	G	-40 °C to +85 °C		
	Ι	-40 °C to +105 °C		

g: F	unction
Р	OE
S	S₹

i: Output option		
Α	Vsw = 0.7 V to 1.4 V	
B	$V_{SW} = 0.8 \text{ V to } 1.6 \text{ V}$	

### (Unit:mm)

i: Output option	
Α	Vsw = 0.7 V to 1.4 V
В	Vsw = 0.8 V to 1.6 V

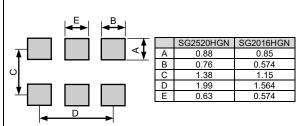
### External dimensions

### SG2520HGN SG2016HGN Pin Connection OE or ST N.C. (Open or V<sub>CC</sub>) GND 4 OUT 5 OUT 6

OE or ST pin = HIGH or "Open": Specified frequency output. OE or  $\overline{ST}$  pin = LOW: Output is high impedance

### Footprint (Recommended)

(Unit:mm)



In order to achieve optimum jitter performance, it is recommended that  $0.1\,\mu F$  and  $10\,\mu F$  bypass capacitors should be connected between  $V_{CC}$ and GND and placed as close to the  $V_{\text{CC}}$  pin as possible.

# PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

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All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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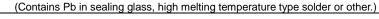
►Pb free.



► Complies with EU RoHS directive.

\*About the products without the Pb-free mark.

Contains Pb in products exempted by EU RoHS directive.





▶ Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.



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