

CRYSTAL OSCILLATOR (SPXO)

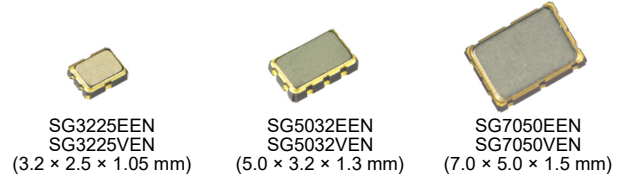
OUTPUT : LV-PECL, LVDS

SG3225EEN / VEN
SG5032EEN / VEN
SG7050EEN / VEN



Product Number
 SG3225EEN: X1G005221xxxx00 (fo ≤ 200 MHz)
 X1G005511xxxx00 (fo > 200 MHz)
 SG5032EEN: X1G005531xxxx00
 SG7050EEN: X1G005131xxxx00 (fo ≤ 200 MHz)
 X1G005551xxxx00 (fo > 200 MHz)
 SG3225VEN: X1G005351xxxx00 (fo ≤ 200 MHz)
 X1G005521xxxx00 (fo > 200 MHz)
 SG5032VEN: X1G005541xxxx00
 SG7050VEN: X1G005331xxxx00 (fo ≤ 200 MHz)
 X1G005561xxxx00 (fo > 200 MHz)

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 2.5 V Typ. / 3.3 V Typ.
- Output : LV-PECL or LVDS
- Function : Output enable (OE)
- Phase jitter : 50 fs Typ. (fo = 156.25 MHz, LV-PECL)
- Operating temperature : -40 °C to +105 °C



Specifications (characteristics)

Item	Symbol	Specifications		Conditions / Remarks	
		LV-PECL SG3225EEN / SG5032EEN / SG7050EEN	LVDS SG3225VEN / SG5032VEN / SG7050VEN		
Output frequency range	fo	25 MHz to 500 MHz 200.1 MHz to 500 MHz		Except for SG5032EEN / SG5032VEN	Please contact us for available frequencies.
Supply voltage	V _{CC}	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.165 V			
Storage temperature range	T _{stg}	-55 °C to +125 °C			
Operating temperature range	T _{use}	G: -40 °C to +85 °C, H: -40 °C to +105 °C			
Frequency tolerance	f _{tol}	D: ±25 × 10 ⁻⁶ Max. J: ±50 × 10 ⁻⁶ Max. L: ±100 × 10 ⁻⁶ Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 5 years aging (+25 °C) Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging (+25 °C)	
Current consumption	I _{CC}	60 mA Max.	25 mA Max.	OE = V _{CC} , L _{ECL} = 50 Ω or L _{LVDS} = 100 Ω	
Disable current	I _{dis}	25 mA Max.		OE = GND	
Symmetry	SYM	45 % to 55 %		At output crossing point	
Output voltage (LV-PECL)	V _{OH} V _{OL}	V _{CC} - 1.1 V Min. V _{CC} - 1.5 V Max.	-	DC characteristics	
Output voltage (LVDS)	V _{OD}	-	250 mV to 450 mV	Differential output voltage, V _{OD1} , V _{OD2}	
	dV _{OD}	-	50 mV Max.	dV _{OD} = V _{OD1} - V _{OD2}	
	V _{OS}	-	1.15 V to 1.35 V	Offset voltage, V _{OS1} , V _{OS2}	
	dV _{OS}	-	50 mV Max.	dV _{OS} = V _{OS1} - V _{OS2}	
Output load condition	L _{ECL}	50 Ω	-	Terminated to V _{CC} - 2.0 V	
	L _{LVDS}	-	100 Ω	Connected between OUT to OUT	
Input voltage	V _{IH}	70 % V _{CC} Min.		OE terminal	
	V _{IL}	30 % V _{CC} Max.			
Rise/Fall times	tr / tf	0.3 ns Max.	0.3 ns Max.	V _{CC} = 3.3 V, 25 MHz ≤ fo ≤ 200 MHz	LV-PECL: Between 20 % and 80 % of (V _{OH} - V _{OL}) LVDS: Between 20 % and 80 % of Differential Output peak to peak voltage
		0.35 ns Max.		All other	
Startup time	t _{str}	10 ms Max.		Time at minimum supply voltage to be 0 s	

Phase Jitter

Product Name	100 MHz	125 MHz	156.25 MHz	200 MHz	312.5 MHz	491.52 MHz	Conditions
SG3225EEN / SG5032EEN / SG7050EEN	75 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	20 fs Typ.	Offset frequency: 12 kHz to 20 MHz
SG3225VEN / SG5032VEN / SG7050VEN	90 fs Typ.	70 fs Typ.	60 fs Typ.	50 fs Typ.	40 fs Typ.	30 fs Typ.	

Product Name SG3225EEN 156.250000MHz C D G A (⑤⑥: Unavailable code DH, DG and JH at fo > 200 MHz, Refer to figure *1)

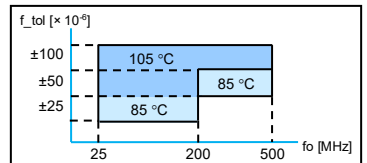
(Standard form) ① ② ③ ④⑤⑥⑦

① Model ② Output (E: LV-PECL, V: LVDS) ③ Frequency ④ Supply voltage

⑤ Frequency tolerance ⑥ Operating temperature ⑦ Internal identification code("A" is default)

*1 : Maximum T_{use} of operating range

④ Supply voltage		⑤ Frequency tolerance		⑥ Operating temperature	
C	3.3 V Typ.	D	±25 × 10 ⁻⁶	G	-40 to +85 °C
D	2.5 V Typ.	J	±50 × 10 ⁻⁶	H	-40 to +105 °C
		L	±100 × 10 ⁻⁶		



External dimensions

(Unit:mm)

SG7050EEN / SG7050VEN
 SG5032EEN / SG5032VEN
 SG3225EEN / SG3225VEN

Pin map

Pin	Connection
1	OE
2	N.C. (Open or V _{CC})
3	GND
4	OUT
5	OUT
6	V _{CC}

Note:
 OE pin = HIGH or "Open": Specified frequency output.
 OE pin = LOW: Output is high impedance

Footprint (Recommended)

(Unit:mm)

	SG3225EEN / SG3225VEN	SG5032EEN / SG5032VEN	SG7050EEN / SG7050VEN
A	1.05	1.60	2.00
B	0.92	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.80	0.89	1.80

In order to achieve optimum jitter performance, it is recommended that 0.1 μF and 10 μF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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IATF 16949 is the international standard that added the sector-specific supplemental requirements for automotive industry based on ISO9001.

► Explanation of the mark that are using it for the catalog

	► Pb free.
	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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