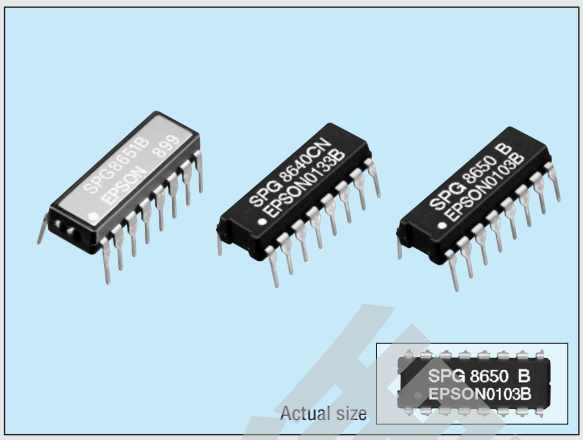
SELECTABLE-OUTPUT CRYSTAL OSCILLATOR

SPG series

- Capable of selecting 57 varieties of frequency output.
- Low current consumption.
- Easy to mount DIP 16-pin package.



Specifications (characteristics)

Item		Symbol	Specifications									Remarks
Model name			8640AN	8640BN	8640CN	8650A	8650B	8650C	8650E	8651A	8651B	8651E	
Oscillation source frequency		fo	600 kHz	1 MHz	768 kHz	60 kHz	100 kHz	96 kHz	32.768 kHz	60 kHz	100 kHz	32.768 kHz	For output frequency, refer to the table in the next page
Power source voltage	Max. supply voltage	VDD-GND	-0.3 V to +7.0 V										
	Operating voltage	VDD	5.0 V±0.5 V										
Temperature range	Storage temperature	TSTG	-55 °C to +125 °C							-30 °C to +80 °C			
	Operating temperature	TOPR	-10 °C to +70 °C							-10 °C to +60 °C			
Soldering condition (lead part)		TSOL	Under +260 °C within 10 s										Package should be less than +150 °C
Frequency tolerance		Δf/f0	±100 x 10-6			±50 x 10-6				±5 x 10-6 *1			VDD=5 V, Ta=+25 °C
Frequency temperature characteristics			+10/-120 x 10-6										VDD=5 V
Frequency voltage characteristics			±20 x 10-6	±10 x 10-6	±20 x 10-6	±10 x 10-6				±5 x 10-6			VDD=4.5 to 5.5 V
Aging		fa	±5 x 10-6/year Max.							±3 x 10-6/year Max.			VDD=5 V, Ta=+25 °C, first year
Current consumption		IOP	1.0 mA Max.	2.0 mA Max.	1.5 mA Max.	0.5 mA Max.							No load condition
Shock resistance		S.R.	±5 x 10-6 Max.(From 500 mm)			±5 x 10-6 Max.			±10 x 10-6 Max.				Three drops on a hard wooden board form 750 mm

*1 Frequency tolerance of 8651 system shows the value guaranteed at the time of shipment.

Electric characteristics

(VDD=5 V±0.5 V, Ta=-10 to +70 °C CL ≤ 15 pF)

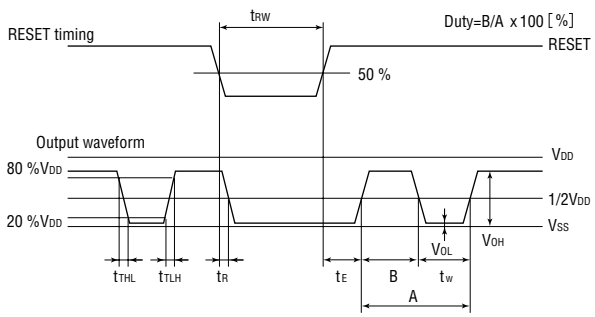
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
L. input voltage	VIL	0		0.8	V	
H. input voltage	VIH	VDD-1.0		VDD		
L. input current (Reset)	IRL	-30		-5	μA	Reset=GND
H input current (Reset)	IRH			0.5		Reset=VDD
L. input current (input terminal except for Reset)	IIL	-0.5				
H input current (input terminal except for Reset)	IIH	5		30		IOL=1.6 mA
L. output voltage	VOL			0.4	V	IOH= -40 μA
H. output voltage	VOH	VDD-1.0				VOL=0.4 V
L. output current	IOL	1.6			mA	VOH=VDD-1.0 V
H. output current	IOH			-40	μA	
Output rise time	tTLH		30	60	ns	
Output fall time	tTHL		25	50		
Duty		40		60	%	Except in the case of 1/3 and 1/5
Min. reset pulse width	tRW	1.0			μs	
Reset delay time	tR			1.0		
Reset release synchronous error	tE	tW-*1 1/2 to		tW *2		
External signal input frequency	FIN			1M	Hz	8640 N only
External signal input pulse width	tIN	0.5			μs	
Oscillation start up time	tOSC		0.2	1	s	*3

*1 to=oscillation source cycle. *2 tw=1/2 cycle of preset frequency.
*3 For more than 1 ms until VDD=0→4.5 V. Time at 4.5 V is to be 0.

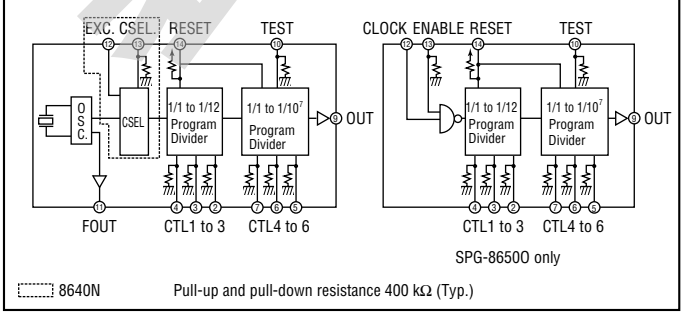
Divider IC (without quartz crystal)

Item	Symbol	Specifications	Remarks
Model name		8650 O	
Input clock frequency		1 MHz max.	
Current consumption	IOP	About 2 mA	No load condition

RESET timing

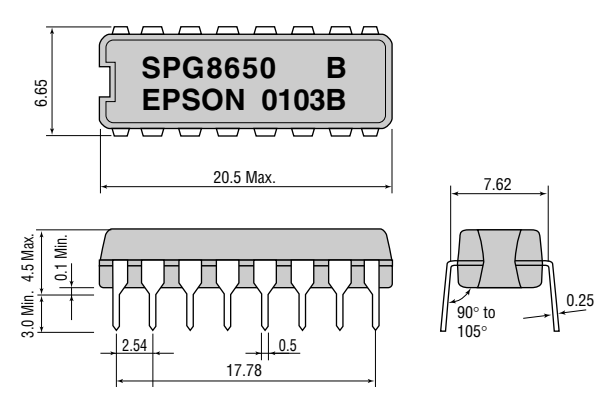


Block diagram

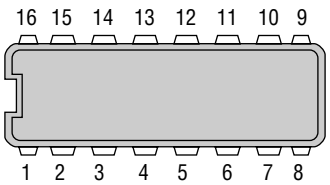


External dimensions

(Unit: mm)



Terminal connection



No.	Pin terminal	No.	Pin terminal
1	NC	16	V_{DD}
2	CTL 3	15	NC
3	CTL 2	14	RESET
4	CTL 1	13	NC (CSEL)
5	CTL 6	12	NC (EXC)
6	CTL 5	11	FOUT
7	CTL 4	10	TEST
8	GND	9	OUT

( ) shown 8640N only

NC: Do not connect to the external terminal.

For 8650 O
11. NC 12. CLOCK 13. ENABLE

Explanation of terminal

(a) CTL 1 to 6 : Programs dividing ratio. (pull-down resistor incorporated.)
(b) OUT : Output frequency preset by CTL1 to 6.
(refer to the procedure for setting output frequency.)
(c) FOUT : Constantly outputs the oscillation source frequency of builtin crystal unit.
(d) RESET : Stops output at RESET= "L".
(pull-up resistor incorporated.)
(e) TEST : Used for the input terminal for testing. When CTL4 is H, output will be 1000 times larger than the preset value at TEST= "H". (pull-down resistor incorporated.)
(f) EXC (8640N only) : Serves as input terminal when using an external clock by changing to the builtin oscillator.
Effective only when CSEL is H.
(g) CSEL (8640N only) : When this terminal is made H, the external clock is selected.
(pull-down resistor incorporated.)

(Note) Treatment of empty terminals. When RESET terminal is not used, this should be connected to V_{DD}, and when TEST terminal, CSEL terminal, and CTL 1 to 6 terminals are not used, to GND.

Explanation of terminal (8650 O)

(a) CLOCK: Clock input (Max. 1 MHz) (b) ENABLE: Be sure to connect to V_{DD}

Setting of divider output

CTL1	CTL2	CTL3	Dividing ratio
0	0	0	1/1
0	0	1	1/10
0	1	0	1/2
0	1	1	1/3
1	0	0	1/4
1	0	1	1/5
1	1	0	1/6
1	1	1	1/12

CTL4	CTL5	CTL6	Dividing ratio
0	0	0	1/1
0	0	1	1/10
0	1	0	$1/10^2$
0	1	1	$1/10^3$
1	0	0	$1/10^4$
1	0	1	$1/10^5$
1	1	0	$1/10^6$
1	1	1	$1/10^7$

0= "L" 1="H"

Setting of output frequency

8640AN

(Unit: Hz)

Set terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL3 \ CTL6	0	1	0	1	0	1	0	1
0	0	0	600k	60k	6k	600	60	6.0	0.6	0.06
0	0	1	60k	6k	600	60	6	0.6	0.06	0.006
0	1	0	300k	30k	3k	300	30	3.0	0.3	0.03
0	1	1	200k	20k	2k	200	20	2.0	0.2	0.02
1	0	0	150k	15k	1.5k	150	15	1.5	0.15	0.015
1	0	1	120k	12k	1.2k	120	12	1.2	0.12	0.012
1	1	0	100k	10k	1k	100	10	1.0	0.1	0.01
1	1	1	50k	5k	500	50	5	0.5	0.05	0.005

8640BN

Set terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL3 \ CTL6	0	1	0	1	0	1	0	1
0	0	0	1M	100k	10k	1k	100	10	1	1/10
0	0	1	100k	10k	1k	100	10	1	1/10	1/100
0	1	0	500k	50k	5k	500	50	5	1/2	1/20
0	1	1	333.3k	33.3k	3.3k	333.3	33.3	3.33	1/3	1/30
1	0	0	250k	25k	2.5k	250	25	2.5	1/4	1/40
1	0	1	200k	20k	2k	200	20	2	1/5	1/50
1	1	0	166.6k	16.6k	1.6k	166.6	16.6	1.6	1/6	1/60
1	1	1	83.3k	8.3k	833.3	83.3	8.3	0.83	1/12	1/120

8650A 8651A

Set terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL3 \ CTL6	0	1	0	1	0	1	0	1
0	0	0	60k	6.0k	600	60	6.0	0.6	0.06	0.006
0	0	1	6k	600	60	6	0.6	0.06	0.006	0.0006
0	1	0	30k	3.0k	300	30	3.0	0.3	0.03	0.003
0	1	1	20k	2.0k	200	20	2.0	0.2	0.02	0.002
1	0	0	15k	1.5k	150	15	1.5	0.15	0.015	0.0015
1	0	1	12k	1.2k	120	12	1.2	0.12	0.012	0.0012
1	1	0	10k	1.0k	100	10	1.0	0.1	0.01	0.001
1	1	1	5k	500	50	5	0.5	0.05	0.005	0.0005

8650B 8651B

Set terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL3 \ CTL6	0	1	0	1	0	1	0	1
0	0	0	100k	10k	1k	100	10	1	1/10	1/100
0	0	1	10k	1k	100	10	1	1/10	1/100	1/1000
0	1	0	50k	5k	500	50	5	1/2	1/20	1/200
0	1	1	33.3k	3.3k	333.3	33.3	3.33	1/3	1/30	1/300
1	0	0	25k	2.5k	250	25	2.5	1/4	1/40	1/400
1	0	1	20k	2k	200	20	2	1/5	1/50	1/500
1	1	0	16.6k	1.6k	166.6	16.6	1.6	1/6	1/60	1/600
1	1	1	8.3k	833.3	83.3	8.3	0.83	1/12	1/120	1/1200

8650E 8651E

Set terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL3 \ CTL6	0	1	0	1	0	1	0	1
0	0	0	32768	3276.8	327.68	32.768	3.276	0.3276	0.03276	0.00327
0	0	1	3276.8	327.68	32.768	3.276	0.327	0.0327	0.00327	0.00032
0	1	0	16384	1638.4	163.84	16.384	1.638	0.1638	0.01638	0.00163
0	1	1	10922.6	1092.26	109.226	10.922	1.092	0.1092	0.01092	0.00109
1	0	0	8192	819.2	81.92	8.192	0.819	0.0819	0.00819	0.00081
1	0	1	6553.6	655.36	65.536	6.553	0.655	0.0655	0.00655	0.00065
1	1	0	5461.3	546.13	54.613	5.461	0.546	0.0546	0.00546	0.00054
1	1	1	2730.6	273.06	27.306	2.730	0.273	0.0273	0.00273	0.00027

Note: Lower digits are omitted.

Baud rate generator

8640CN

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Output frequency	Baud rate output example (fo/16)
0	0	0	0	0	0	768 kHz	48000 bits/s
1	0	1	0	0	0	153.6	9600
0	0	1	0	0	0	76.8	4800
0	1	0	0	0	1	38.4	2400
1	0	0	0	0	1	19.2	1200

8650C

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Output frequency	Baud rate output example (fo/16)
0	0	0	0	0	0	96.0 kHz	6000 bits/s
1	0	1	0	0	0	19.2	1200
0	0	1	0	0	0	9.6	600
0	1	0	0	0	1	4.8	300
0	1	1	0	0	1	3.2	200
1	0	0	0	0	1	2.4	150
1	1	0	0	0	1	1.6	100
1	1	1	0	0	1	0.8	50