

## **Programmable Voltage Controlled Oscillator (VCXO)**

**Output: LV-PECL** 

# VG7050EAN / ECN

• Frequency range : 50 MHz to 800 MHz

(Tuning resolution: 2.2 to 2.8 ×10-9)

 Supply voltage : 2.5 V / 3.3 V

• External dimensions : EAN : 7.0 × 5.0 × 1.5 mm (8 pins) ECN : 7.0 × 5.0 × 1.5 mm (10 pins)

• Absolute Pull Range :  $\pm 0 \times 10^{-6}$  to  $\pm 180 \times 10^{-6}$  (12 steps selectable)

• EAN: User-specified one startup frequency, APR and 7-bit I2C address • ECN: User-specified four startup frequency, APR and 7-bit I2C address

• User Programming : I<sup>2</sup>C Interface

Low jitter PLL technology

Applications

SONET/SDH, OTN, GbE, Fibre Channel







EAN: X1G004541xxxx00 ECN: X1G004561xxxx00





#### Specifications (characteristics)

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Symbol	Specifications	Conditions / Remarks	
fo	50 MHz to 800 MHz	It can be changed by I <sup>2</sup> C	
V <sub>CC</sub>	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.33 V		
T_stg	-55 °C to +125 °C	Store as bare product after packing	
T_use	-40 °C to +85 °C		
f_tol	±50 × 10 <sup>-6</sup>	Includes frequency aging (10 years)	
I <sub>CC</sub>	90 mA Max.	OE Active, L_ECL=50 Ω	
	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode	
I_dis	70 mA Max.	OE Inactive, Output Standby: Fix mode	
ADD	±0 × 10 <sup>-6</sup> to ±180 × 10 <sup>-6</sup> Min.	Vc = 1.65 V ± 1.35 V (Vcc = 3.3 V)	
AFK	$\pm 0 \times 10^{-6}$ to $\pm 180 \times 10^{-6}$ Min.	Vc = 1.25 V ± 1.00 V (Vcc = 2.5 V)	
Vc	0 V to Vcc		
-	Positive slope		
SYM	45 % to 55 %	At outputs crossing point	
V <sub>OH</sub>	Vcc - 1.025 V Min.	DC characteristics	
V <sub>OL</sub>	Vcc - 1.62 V Max.		
L_ECL	50 Ω	Termination to Vcc - 2.0 V	
V <sub>IH</sub>	70 % Vcc Min.	EAN : OE, SDA and SCL ECN : OE, FSEL0, FSEK1, SDA and SCL	
V <sub>IL</sub>	30 % Vcc Max.		
tr / tf	400 ps Max.	Between 20 % and 80 % of (VoH - VoL)	
t_str	10 ms Max.	Time at minimum supply voltage to be 0 s	
	fo	fo 50 MHz to 800 MHz  V <sub>CC</sub> D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.33 V  T_stg -55 °C to +125 °C  T_use -40 °C to +85 °C  f_tol ±50 × 10-6  I <sub>CC</sub> 90 mA Max.  I_dis 70 mA Max.  APR ±0 × 10-6 to ±180 × 10-6 Min.  VC 0 V to VCC  - Positive slope  SYM 45 % to 55 %  V <sub>OH</sub> VCC -1.025 V Min,  VoL VC -1.62 V Max.  L_ECL 50 Ω  V <sub>IH</sub> 70 % VCC Min.  V <sub>IL</sub> 30 % VCC Max.  tr / tf 40 °C to +125 °C  1-40 °C to +125 °C  1-4	

<sup>\*1</sup> Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product name VG7050 EAN SM18xxxx CJ GHPZ (Standard form)

456789 1

①Model

2 Output (E: LV-PECL)

③Parameter Designator (EAN: SM18xxxx, ECN: SM20xxxx )

(4) Supply voltage (C: 3.3 V Typ., D: 2.5 V Typ.)

5 Frequency tolerance (J: ±50 × 10<sup>-6</sup>)

6Operating temperature (G: -40 °C to +85 °C)

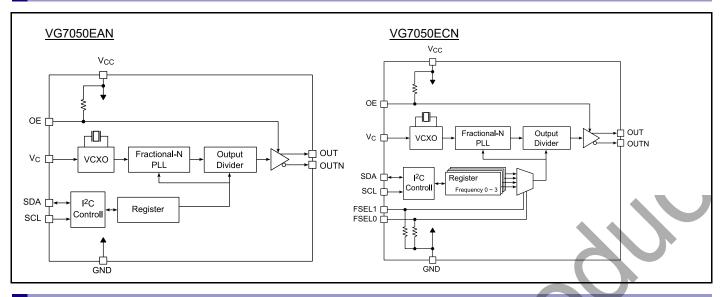
OE Function (H: Active High, L: Active Low)

#### **Phase Jitter**

	Offset Frequency	125.00 MHz	156.25 MHz	250.00 MHz	425.00 MHz	622.08 MHz	669.33 MHz	794.73 MHz
Phase jitter*2 - Typ.	12 kHz to 20 MHz	0.30 ps	0.26 ps	0.26 ps	0.25 ps	0.26 ps	0.26 ps	0.26 ps
	20 kHz to 50 MHz	0.30 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps
	50 kHz to 80 MHz	0.29 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps

<sup>\*2</sup> In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μF + 10 μF) between Vcc and GND pin should be placed as close to the Vcc pin as possible.

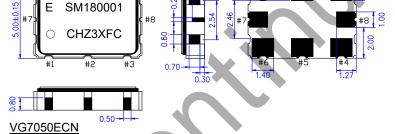
#### Block diagram

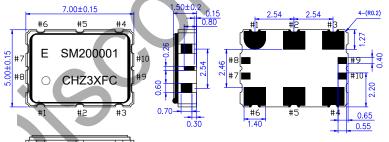


### OE Function / OE Standby Type

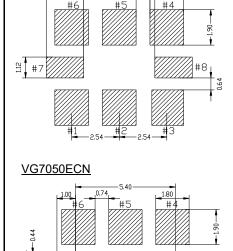
OE Function	OE Standby Type	Output Enable	Output Disable		
OL I dilction	OL Standby Type	OE pin	OE pin	OUT, OUTN pin	
H: High Active	7. High 7	"H" or "OPEN"	"L"	Lligh Issnadance	
L: Low Active	Z: High-Z	"L" or "OPEN"	"H"	High Impedance	
H: High Active	F: Fix	"H" or "OPEN"	"L"	OUT = "L", OUTN = "H"	
L: Low Active	r. FIX	"L" or "OPEN"	"H"	001 = L,001N = 11	

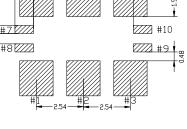
# External dimensions (Unit: mm) Footprint (Recommended) (Unit: mm) VG7050EAN VG7050EAN





0.50	Din	Connection		Din	Connection		
0.50 -   -	Pin	EAN	ECN	Pin	EAN	ECN	
	1	Vc	Vc	6	Vcc	Vcc	
	2	OE	OE	7	SDA	SDA	
	3	GND	GND	8	SCL	SCL	
	4	OUT	OUT	9	-	FSEL0	
	5	OUTN	OUTN	10	•	FSEL1	





In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1  $\mu F$  + 10  $\mu F)$  between VCC and GND pin should be placed as close to the VCC pin as possible.

# PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

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►Pb free.



► Complies with EU RoHS directive.

\*About the products without the Pb-free mark.

Contains Pb in products exempted by EU RoHS directive.

(Contains Pb in sealing glass, high melting temperature type solder or other.)



▶ Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.



▶ Designed for automotive applications related to driving safety (Engine Control Unit, Air Bag, ESC etc.).

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