

VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO)  
OUTPUT : LV-PECL, LVDS



Product Number  
 VG3225EFN X1G005361xxxx00  
 VG5032EFN X1G005471xxxx00  
 VG7050EFN X1G005491xxxx00  
 VG3225VFN X1G005461xxxx00  
 VG5032VFN X1G005481xxxx00  
 VG7050VFN X1G005501xxxx00

**VG3225EFN / VFN**  
**VG5032EFN / VFN**  
**VG7050EFN / VFN**

- Frequency range : 25 MHz to 500 MHz (VG3225EFN / VFN)  
25 MHz to 250 MHz (All other)
- Supply voltage : 3.3 V Typ.
- Output : LV-PECL or LVDS
- Function : Output enable (OE)



Specifications (characteristics)

Item	Symbol	Specifications		Conditions / Remarks
		LV-PECL VG3225EFN / VG5032EFN / VG7050EFN	LVDS VG3225VFN / VG5032VFN / VG7050VFN	
Output frequency range	fo	25 MHz to 500 MHz	25 MHz to 250 MHz	VG3225EFN / VG3225VFN All other
Supply voltage	V <sub>CC</sub>	C: 3.3 V ± 0.165 V		Please contact us for available frequencies.
Control voltage	V <sub>C</sub>	1.65 V ± 1.65 V		
Storage temperature range	T <sub>stg</sub>	-55 °C to +125 °C		
Operating temperature range	T <sub>use</sub>	G: -40 °C to +85 °C, H: -40 °C to +105 °C		
Frequency tolerance	f <sub>tol</sub>	J: ±50 × 10 <sup>-6</sup> Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging (+25 °C) at V <sub>C</sub> = 1.65 V
Absolute Pull range *1	APR	B: ±50 × 10 <sup>-6</sup> Min.		25 MHz ≤ fo ≤ 42.5 MHz, 50 MHz ≤ fo ≤ 85 MHz, 100 MHz ≤ fo ≤ 170 MHz
		M: ±20 × 10 <sup>-6</sup> Min.		25 MHz ≤ fo ≤ 250 MHz
		S: ±10 × 10 <sup>-6</sup> Min.		25 MHz ≤ fo ≤ 250 MHz
				250 MHz < fo ≤ 500 MHz, T <sub>use</sub> : G (-40 °C to +85 °C)
Current consumption	I <sub>CC</sub>	60 mA Max.	25 mA Max.	OE = V <sub>CC</sub> , L ECL = 50 Ω or L LVDS = 100 Ω
Disable current	I <sub>dis</sub>	25 mA Max.	15 mA Max.	OE = GND
Input impedance	Z <sub>in</sub>	10 MΩ Min.		DC level
Frequency change polarity	-	Positive slope		V <sub>C</sub> = 0 V to 3.3 V
Symmetry	SYM	45 % to 55 %		At output crossing point
Output voltage (LV-PECL)	V <sub>OH</sub>	V <sub>CC</sub> - 1.1 V Min.	-	DC characteristics
	V <sub>OL</sub>	V <sub>CC</sub> - 1.5 V Max.	-	
Output voltage (LVDS)	V <sub>OD</sub>	-	250 mV to 450 mV	Differential output voltage, V <sub>OD1</sub> , V <sub>OD2</sub>
	V <sub>OS</sub>	-	1.15 V to 1.35 V	
ECL load condition	L <sub>ECL</sub>	50 Ω	-	Offset voltage, V <sub>OS1</sub> , V <sub>OS2</sub>
LVDS load condition	L <sub>LVDS</sub>	-	100 Ω	Terminated to V <sub>CC</sub> - 2.0 V
Input voltage	V <sub>IH</sub>	70 % V <sub>CC</sub> Min.		OE terminal
	V <sub>IL</sub>	30 % V <sub>CC</sub> Max.		
Rise/Fall times	tr / tf	0.5 ns Max.	0.3 ns Max.	LV-PECL: Between 20 % and 80 % of (V <sub>OH</sub> - V <sub>OL</sub> ) LVDS: Between 20 % and 80 % of Differential Output peak to peak voltage
Startup time	t <sub>str</sub>	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t <sub>PJ</sub>	120 fs Max.	160 fs Max.	fo = 122.88 MHz
		80 fs Max.	80 fs Max.	fo = 245.76 MHz
		70 fs Max.	80 fs Max.	fo = 491.52 MHz

\*1 Absolute pull range = Frequency control range - Frequency tolerance  
 \* Please keep V<sub>C</sub> pin open or ground while powering up V<sub>CC</sub>.

Product Name **VG3225 EFN 122.88000MHz C J G H B A**

(Standard form)

- ① Model ② Output (E: LV-PECL, V: LVDS) ③ Frequency  
 ④ Supply voltage (C: 3.3 V Typ.) ⑤ Frequency tolerance ⑥ Operating temperature  
 ⑦ OE Function ⑧ Absolute Pull Range ⑨ Output Standby Type (A: High-Z)

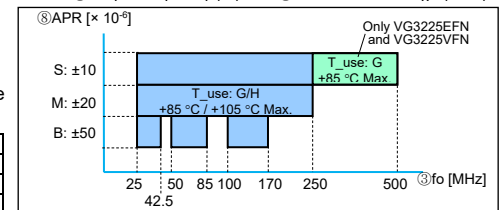
⑤ Frequency tolerance	J	±50 × 10 <sup>-6</sup>
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⑥ Operating temperature	G	-40 to +85 °C
	H	-40 to +105 °C

⑦ OE Function	H	Active High
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⑧ Absolute Pull Range	B	±50 × 10 <sup>-6</sup>
	M	±20 × 10 <sup>-6</sup>
	S	±10 × 10 <sup>-6</sup>

Figure 1 Available combination of  
 ③ Output frequency (fo) and ⑧ Absolute Pull Range (APR)





External dimensions

(Unit:mm)

VG7050EFN  
VG7050VFN

VG5032EFN  
VG5032VFN

VG3225EFN  
VG3225VFN

Pin map

Pin	Connection
1	V <sub>c</sub>
2	OE
3	GND
4	OUT
5	OUT
6	V <sub>CC</sub>

Note:  
OE pin = HIGH or "Open": Specified frequency output.  
OE pin = LOW: Output is high impedance

Footprint (Recommended)

(Unit:mm)

	VG3225EFN VG3225VFN	VG5032EFN VG5032VFN	VG7050EFN VG7050VFN
A	1.05	1.60	2.00
B	0.92	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.80	0.89	1.80

In order to achieve optimum jitter performance, it is recommended that 0.1 μF and 10 μF bypass capacitors should be connected between V<sub>CC</sub> and GND and placed as close to the V<sub>CC</sub> pin as possible.

## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

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	► Pb free.
	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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